The mild objection I have to L. Fein's letter is this: He has presented some problems and proposed a solution. The problems, as defined, are somewhat exaggerated, and he takes no cognizance of the conscientious attempts which are being made to solve them. Many aspects of his prescription have been used, and since the objections he voices still exist, there must be more to be done. His letter is a good start towards initiating a discussion which, I am sure, will result in no unavailability of opinion, but which should provide valuable guides for the planning of future meetings.

RICHARD I. TANAKA
Chairman, Conference Committee
IEEE—PTGEC

Ultimate-Speed Adders*

Lehman and Burla [1] in their TRANSACTIONS paper describe the "skip-carry" binary adders, by which an attractive compromise between speed and diode expenditure is achieved. They include a comparison of the speed and diode expenditure for several competing types of binary adders. They conclude that, except for the possible implications of accounting for the systems in which the adders are imbedded, a properly designed skip-carry adder is the fastest for a given expenditure of diodes, as well as the most economical in diode for a given computational speed. In particular the conditional-sum adder appears in their paper to have lost the speed superiority it had in an earlier analysis [2], [3].

In this correspondence we present a point of view by which "conditional logic" and its related technique "distant-carry logic" achieve addition speeds that in principle cannot be exceeded by skip techniques. We shall explain why we feel this point of view is both meaningful and useful for a certain type of hardware technology. Upper bounds on the realizable addition speeds are derived. The speeds of conditional adders and distant-carry adders turn out to approach these bounds surprisingly closely.

I. WHICH ADDER IS THE FASTEST?

The extent to which the "speed" of an adder contributes to the over-all value or effectiveness of a computer depends, of course, on quite a thing as function of the costs of engineering, fabrication, operation and maintenance of the entire computer [2]. Hence when one evaluates the utility of an entire computer the speed of the adder is likely to be drowned in a complicated sea of economic and engineering considerations.

Consequently the question "Which adder is the fastest?" is an impossibly difficult question if we define adder speed as the contribution of an adder to over-all computational effectiveness. On the other hand it is possible to obtain a meaningful answer if we constrain the class of adders to those adders that produce in a parallel fashion a binary sum from two binary summands. We call these the "binary parallel adders."

At this point we find that we still cannot answer the proposed question, for the following reason: we have not yet defined a unit of addition time. The natural unit to adopt is the delay of a single AND gate or OR gate. In practice, however, the speeds of these gates are dependent on several factors, of which gate delay is only one. Among these factors are the fan-in and fan-out capacities of the individual gates. In fact, when certain high-speed hardware has been used, the fan-in/fan-out capacities are critical parameters forming bounds on the logic speed. More will be said about this in Section II.

In the communication we answer the question, "Which adder is the fastest?" we shall really be answering the following more restricted question. "Which binary parallel adder consumes the fewest gate delays in adding two summands, under the constraint that the fan-in and fan-out capacities of the individual gates do not exceed certain specified values?"

Now we ask ourselves, "How useful is the answer to the above relatively constrained question?" i.e., "Is the class of adders under consideration so narrow that the answer is neither interesting nor useful?"

It turns out that practically all of the "fast" adders used in practice fall into two classes: the binary parallel adders and two-bit number-system adders. (The latter class includes the separate-carry-storage adders.) We expect that under certain design specifications that binary parallel adders will be preferable. For these conditions a quantitative description of the speeds of binary parallel adders and of fan-in/fan-out capacities, summed lengthiously, diode count should be useful. Under other conditions, the redundant number system offers an attractive approach [6].

A quantitative description of the speeds of binary parallel adders for the case of a fan-in capacity of two appears in an earlier paper [2], and is extended here to more general fan-ins and fan-outs. From this evidence we note the following: If the maximum permissible fan-in per gate is two, and if the admissible fan-out per gate is unrestricted, then the conditional-sum adder is the fastest known adder. (In Section II we discuss why a fan-in of two is realistic when certain high-speed hardware is used.)

Empirical evidence also indicates that if in addition to the fan-in constraint—fan-out is constrained to lie below or at a specified constant, then the conditional-sum adder is still the fastest adder. Why, then, does the conditional-sum adder appear slower than the carry-skip adder in the second example of Lehman and Burla's paper? (Hereafter we shall refer to the latter adder as the "Lehman-Burla example."

The reason is that the Lehman-Burla example is built of gates having fan-ins as large as eight, and that the delay of their multiple-input gates is equal to that of any other of their gates independently of the individual fan-ins. These multiple-input gates are practical when ordinary diodes are used; however, if high-speed devices such as...
Correspondence

This results in a conditional sum adder in which binary-coded conditional sums and carries are generated for each r-ray digit. The number of gates becomes larger than that in the Lehman-Burla example, but the computational time—or, more accurately, the effective carry-production time—is reduced to \( t = \log_2(n + 1) \), where \( n \) is the length of the summand register, \( t \) is the carry-production time defined by Lehman-Burla, and the circumflex indicates that \( \log_2 n \) is the smallest integer greater than \( \log_2 n \). When \( p > 2 \), the resulting conditional-sum adder requires a maximum fan-in of \( \gamma \geq n \). On the other hand, a conditional-carry adder based on the same basic concept will require a maximum fan-in of \( \gamma = p \). Furthermore, the conditional-carry adder uses significantly less gates than the conditional-sum adder when \( p > 2 \).

It turns out that the conditional-carry adder can be simplified further by the use of "auxiliary carries" in place of conditional carries. When this is done, \( t \) and \( p \) remain the same, but we have the "simultaneous carry" adder described by Weinberger and Smith [4]. Simultaneous carries are of the form \( \gamma = p \) and have been known as "look-ahead carry" and "distance-carry" logic. We shall use the term "distant carry." To compare the conditional-carry and the distant-carry logic, examine Figs. 1 and 2. Fig. 1 shows the basic conditional-carry logic for a span of 5; Fig. 2 shows the basic distant-carry adder for a span of 5. The next hierarchical level of distant-carry logic is illustrated in Fig. 3. (In Figs. 1–3, \( e \) and \( f \) are auxiliary carries, while \( e' \) and \( f' \) are conditional carries.)

Hence, it seems appropriate to compare the Lehman-Burla example with a fully layered distant-carry adder for spans of 3 or 4 to 8. The results of such a comparison show that one may, by the distant carry technique, achieve a carry-production time of

\[
t = 1 + \log_2(n + 1)
\]

where \( n \) is the summand length.\(^1\) For example, if \( p = 8 \), then \( n = (n + 1) = \log_2(55) = 5.13 \). Consequently \( t = 2.5 \). This value of \( t \) is five-eighths of the carry-production time in the Lehman-Burla example, achieved at a cost of an approximate doubling in the diode expenditure.

In the event \( p = 2 \) and \( 2 \leq n \leq 4 \), the conditional-carry adder will be faster than a distant-carry adder by the time \( \Delta = 1 \), because there is no need to assimilate carries in the conditional-sum adder.

IV. NUMERICAL COMPARISON

Table 1 displays the results of a comparison of three fully layered 54-bit distant-carry adders with the Lehman-Burla example. Undoubtedly further simplifications of the distant-carry adders could be made (as, for example, was done by Weinberger and Smith [4]) in such a way as to reduce the diode expenditure without incurring a loss in addition time. No attempt at such simplifications was made in this comparison.

Our version of the distant-carry adder with a span of 6 is shown in Fig. 4. The carry-production time and diode expenditure of this adder, as well as two other similarly structured adders with spans of 4 and 8, were computed and the results tabulated in Table 1 in the rows labeled \( DCA_p \), \( DCA_4 \), and \( DCA_8 \). The last column of Table 1 shows the number of extra diodes \( \Delta D \) required to reduce the maximum fan-out, \( f \), to 7 and \( f' \). The value of \( f' \) was chosen because this is the value of \( f \) in the Lehman-Burla example. In all cases the extra diodes required for fan-out reduction are less than the number of the original number of diodes, \( D \), and hence are not significant considerations.

We note in Table 1 that addition time must be bought at a disproportionate cost in diodes. However, it may be worthwhile in some instances to pay a 100 per cent increase in hardware for a 37 per cent reduction in addition time, since a time saving accumulates over the life of the computer. Therefore, \( Q \) is not necessarily the best figure of merit of the adders. Other figures of merit, such as \((f/n) \log_2 D \) might result in more realistic relative standings [2].

The following tentative conclusion is also observed in Table 1: For a given addition time, the number of diodes is minimized by using the smallest possible span for the required summand length \( n \). (This corroborates Lehman-Burla's design principle b.) Another tentative conclusion is that \( \Delta D \) increases as \( p \) increases if \( n \) is constant.

The following questions are stimulated by the remarks of Lehman-Burla in the last paragraph of their paper: 1) For a given addition speed, which adder expends the most diodes? 2) For a given diode expenditure which adder is fastest? Unfortunately, Table 1 cannot answer either of these questions. We believe, however, that skip-carry cannot achieve the speeds of fully layered distant-carry or conditional sum at any expenditure of diodes, because the latter two techniques give us adders whose addition times seem to approach the shortest that can be physically realized. In the interstaging category, there is the evidence supporting this belief.

VI. WHAT IS THE EVIDENCE SUPPORTING THE THESIS THAT CONDITIONAL-LOGIC AND DISTANT-CARRY TECHNIQUES YIELD NEAR-ULTIMATE-SPEED ADDERS?

Basically, addition speed is limited by gate delay and by fan-in and fan-out capacities of the individual gates. Fig. 5 (p. 146) illustrates the interdependence of the sums and output carries of a six-bit adder on the summand bits in the preceding columns. Note that the maximum fan-in and fan-out indicated in the illustration are both equal to the summand length, namely 6. If the available fan-in and fan-out per gate are both less than 6, then clearly the addition time or carry-production time will necessarily be greater than a single-gate delay.

To determine a lower bound on the addition time or carry-production time, note from Fig. 6 (p. 146) how tree networks can implement large fan-ins and fan-outs with low-gain gates. Each of these tree networks is minimal both in its gate expenditure and...

\(^{1}\) We refer here to our version of the distant-carry adder, illustrated in Fig. 4.

The enclosed numbers in Fig. 4 indicate fan-out requirements of certain sections of the adder.
Fig. 1—Conditional carry selector for a span of 5 at level 1 (denoted as $K_0$).

Fig. 2—Auxiliary carry selector for a span of 5 at level 1 (denoted as $\overline{K}_1$).
TABLE I

<table>
<thead>
<tr>
<th></th>
<th>$t$</th>
<th>$100 t/u_s$</th>
<th>$D$</th>
<th>$D/m$</th>
<th>$Q$</th>
<th>$r$</th>
<th>$d$</th>
<th>$\Delta D$</th>
<th>$\delta = \gamma$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lehman-Futura</td>
<td>4</td>
<td>7.4</td>
<td>1014</td>
<td>18.8</td>
<td>17</td>
<td>8</td>
<td>7</td>
<td>0</td>
<td>0.0</td>
</tr>
<tr>
<td>DCA1</td>
<td>3.5</td>
<td>6.48</td>
<td>1376</td>
<td>24.6</td>
<td>19.9</td>
<td>4</td>
<td>40</td>
<td>31</td>
<td>75.0</td>
</tr>
<tr>
<td>DCA3</td>
<td>3.5</td>
<td>6.48</td>
<td>1010</td>
<td>28.7</td>
<td>23.2</td>
<td>6</td>
<td>30</td>
<td>34</td>
<td>42.0</td>
</tr>
<tr>
<td>DCA4</td>
<td>2.5</td>
<td>4.63</td>
<td>2127</td>
<td>38.1</td>
<td>22.1</td>
<td>8</td>
<td>70</td>
<td>64</td>
<td>53.0</td>
</tr>
</tbody>
</table>

$\Delta D$ carry-production time.
$\delta$ carry-production time of a pure ripple-carry adder.
$D$ number of diodes.
$\gamma$ summand length.
$\delta = 100 D/(u_4 D_s)$, where $D_s$ number of diodes in a pure ripple-carry adder.
$\gamma$ maximum permissible fan-in per gate.
$\delta$ maximum permissible fan-out per gate.
$\Delta D$ additional diodes needed for fan-out reduction.

Fig. 3—Auxiliary carry selector for a span of 5 at level 2 (denoted as $V_i$). Dotted lines indicate how fan-out of one of the auxiliary carries may be increased.

Fig. 4—An n-looked distant-carry adder with a span of 6.
its overall delay provided the available gates have maximum permissible fan-ins (or fan-outs) equal to the number of converging (or diverging) branches at each node of the tree.

Returning to Fig. 5, note that information on the column 0 summand bits must reach column 5 as part of a fan-out of 6 emanating from column 0. Implementing this fan-out by a tree network contributes \(\lg n\) gate delays to the addition time. (We define \(\log x\) as the smallest integer not less than \(\log x\).) Note also that the sum and output-carry bits of column 5 are dependent upon 2 summand bits; hence the generation of the sum and output-carry bits at column 5 requires an effective fan-in of 2. Implementing this fan-in by a tree network contributes \(\lg 2\) gate delays. Since the tree networks impose minimal overall delays for given \(n\) and \(k\), the overall addition time or carry-production time cannot be less than \(\max(\log 2, 2n, \log n)\) gate delays. Note that Lehman-Burla's definition of \(k\) is one half the number of gate delays. Hence,

\[
4 \geq \frac{1}{2} \max(\log 2, 2n, \log n),
\]

where \(4\) is defined as the shortest realizable addition time or carry production time.

An analysis of the so-called carry-adder shows that the carry-production time of this adder is

\[
\begin{align*}
\text{cadd} &= \log_2 (2n + 2) + \frac{1}{2} \log_2 \left( \frac{n + 1}{2} \right) \\
&= \log_2 (2n + 2) + \frac{1}{2} \log_2 (n + 1 - \frac{n + 1}{2})
\end{align*}
\]

An analysis of the 2-span conditional-sum adder gives the following addition time:

\[
\text{csadd} = \log_2 (2n + 2) + \frac{1}{2} \log_2 \left( \frac{n + 1}{2} \right).
\]

When \(k = \gamma = 1\) and \(n\) is large, the addition/carry-processing times of both the direct-carry adder and the conditional-sum adder are approximately three times the lower bound indicated in the right member of (1). On the other hand, when \(k < \gamma < 2\) and \(n = 1/2\), the conditional-sum adder is almost equal to the right member of (1). Hence in the fan-out-limited case the conditional-sum adder and direct-carry adder seem to approach the ultimate in speed. For the cases where \(k = \gamma = 1\) and \(\gamma > 2\) then the CS adder and DCA are not necessarily ultimate-speed, but analysis under the fan-in/fan-out constraint indicates that they are the fastest known adders. In particular, when \(k = 2\) the conditional-sum adder is faster than the direct-carry adder; for \(\gamma > 2\) both the CS adder and DCA are out of the running altogether, because their fan-in requirements seem to be proportional to \(P^2\).

When \(\gamma < 1\), the sum/carry processing times of the conditional-sum adder and direct-carry adder are about twice the right-hand member of (1). At first sight this factor of two might appear large. Upon reflection, however, we see that it is, in fact, surprisingly small. The normal-form realization of a general Boolean function of 2\(n\) variables requires as many as \(2^n - 1\) AND gates or OR gates feeding an OR gate (or AND gate). Imposing the fan-in constraint, we must replace the \(2^n\)-input AND gate and the \(2^n\)-input OR gate by tree networks of the form of Fig. 6(a); furthermore, internal fan-outs as large as \(2^n - 1\) in the normal-form network may have to be implemented by tree networks of the form of Fig. 6(b). Hence we expect that implementing a \(2^n\)-variable Boolean function will generally require many more gates and will consume much more delay than that of a single-tree network.

In fact we would expect from these considerations that the ratio \(\log 2, 2n + 1\) increase rapidly as \(n\) increases. Hence it is surprising (and gratifying) that \(\text{cadd}\) remains approximately constant at its value 2 independently of the size \(n\) when \(\gamma < 1\). (The factor of two can be explained by the fact that each AND gate must be followed by an OR gate when \(\gamma < 1\)).

We suspect, therefore, that this factor two represents very nearly the ratio between ultimate realizable speeds and the upper bound implied by (1) when \(\gamma < 1\).

VII. A FEW MISCELLANEOUS ITEMS

1) The carry-skipping or "look-ahead" technique is a combination of distant-carry logic [4] and ripple-carry logic [5]. It is possible to have a pure ripple-carry logic, and it is possible to have a pure distant-carry logic, but it is not possible to have pure carry-skipping logic.

2) Fig. 4 of the Lehman-Burla paper [6] is a hybrid of a fully layered distant-carry adder and a ripple-carry adder. Hence certain parts of the ripple-carry logic are superfluous. In particular, the lower right-hand AND gate in each ripple-carry feed lines for columns 2 to 5 may be deleted. The resulting circuit has the form of our Fig. 2, if we delete from Fig. 2 the gate forming the auxiliary carry \(f_3\) of.

3) The effective carry-processing time of the \(S\)-bit conditional-sum adder is \(t = 6\) rather than the \(S\) listed in Lehman-Burla's Table II. Apparently Lehman and Burla noted that the conditional carries in the \(S\) modules of Fig. 2 of Sklansky [3] are produced in \(2n = 2\). However, the conditional-sum bits in these modules are produced in \(3n = 3\). Because the columns covered by the last layer of conditional logic, the final-sum bits cannot be produced until the conditional-sum bits is the earlier layers are transmitted downward. Hence the sum-bit-propagation time, rather than the carry-propagation time, determines the speed of this adder.

4) Lehman-Burla's computation of the addition time for the "simultaneous-carry" adder is \(t = 4\), while we compute \(t = 3.5\) for our version of the same type of adder. An analysis of Weinberger and Smith's 3-bit adder (Fig. 10 of [4]) also yields \(t = 3.5\).

VIII. SUMMARY AND CONCLUSIONS

1) The following inequality describes a lower bound on the physically realizable addition or carry production time of an \(n\)-bit binary adder:

\[
4 \geq (1/2) \max(\log 2, 2n, \log n).
\]

2) Conditional logic and distant-carry logic are strongly related.

3) Conditional-sum adders are the fastest known adders when the maximum permissible fan-in, \(\gamma\), is two. (This low fan-in is realistic for certain types of high-speed hardware being developed today.) When \(\gamma > 2\), distant-carry adders are both faster and require fewer gates than conditional-sum...
Correspondence

Dr. Sklansky's Reply

I am very grateful to Dr. Lehman for his comments. They are perhaps representative of the point of view of the logical designer strongly motivated toward overall machine effectiveness and economy.

My overall reaction to his comments is that they seem to originate from a misunderstanding of the principal theme of my correspondence. That theme is not, "What is the fastest adder?" It is, rather, a continuation of a discussion, begun by Lehman and Burla in their paper [1], on the question, "What are the relative logical speeds of parallel binary adders—in particular, skip-carry adders—and at what cost in diode expenditure are these logical speeds achieved?" The correspondence was an attempt to show 1) that fan-in/fan-out considerations will change the relative standings of the papers considered in the Lehman and Burla paper, in particular the conditional-sum and distant-carry (or "simultaneous-carry") adders, and 2) that as a hybrid between ripple-carry and distant-carry, there is little hope that a skip-carry adder can achieve the logical speeds of distant-carry logic under any diode expenditure, for a given fan-in/fan-out constraint. My discussion of upper bounds on addition speeds was intended to lend a certain plausibility to 2), although admittedly these bounds are not tight enough to constitute anything more than an argument. The discussion of these bounds was not based on the assumption of low fan-ins—as Dr. Lehman seems to imply—although the case $< \leq 2$ did receive special attention for mathematical reasons, not for its practical interest.

I agree with Dr. Lehman in his contention that devices with fan-ins and fan-outs of order five to ten will remain practical for a long time, in spite of the fact that the advent of nanosecond circuitry points to low fan-in/fan-out as a problem to live with at very high operating frequencies. The correspondence, however, does not address itself only to low fan-in circuitry—it emphasizes that no matter what the fan-in/fan-out of the available hardware may be, the fan-in/fan-out size should be a significant parameter in any comparison of logical speeds. Thus in Table I of the correspondence, adders with relatively high fan-in/fan-out are compared with a nanosecond circuitry—Dr. Lehman questions the utility of considering circuits having a low fan-in (in particular, a fan-in of two) and a large fan-out. My answer to this is at the logical design level rather than at the component-design level: A component having a fan-in of two and a fan-out of five is as valuable in a tree of similar components in which the fan-out per component is as low as desired. In many distant-carry and conditional-sum adders of practical interest, such a replacement will not incur a reduction in the overall logical speed. This is the case for the adders discussed in Section IV of the correspondence. The number of diodes consumed in such a replacement are given in the last two columns of Table I.

Dr. Lehman brings forth the embarrassing question of the utility of this entire discussion—including, by implication, the Lehman-Burla adder comparison—because he doubts on the value of an adder comparison that excludes the class of redundant-number-system circuits. The correspondence was a response to the Lehman-Burla comparison, and retained the same framework of discussion, including the implied assumption on the utility of such an analysis. My feelings on Dr. Lehman's doubt-casting are: 1) that parallel binary adders have not yet been made obsolete by any means (where by "parallel binary adders" we exclude redundant-number-system adders), and 2) that parallel binary adders are relatively easy to compare and that the means we can obtain certain interesting and useful design information at relatively little effort.

Dr. Lehman goes on to object that even within the class of parallel binary adders, the correspondence is not sufficiently comprehensive, apparently because it does not bring to the same question and intensity of discussion to such circuits as the skip-carry and the pyramid adders as it does to the distant-carry and the conditional-sum adders. Again this reflects a certain amount of misunderstanding of the principal aim of the correspondence, which was to show that the importance of the fan-in/fan-out constraint and to comment on Lehman and Burla's contention that skip-carry adders are
superior with respect to diode expenditure per unit of logical speed. With this aim in mind, I felt a discussion of adders other than distant-carry, conditional-sum, and skip-carry was unnecessary. Because the skip-carry adder is a hybrid of a ripple-carry adder and a distant-carry adder, because ripple-carry adders and the related carry-detection adders are slower on the average than distant-carry adders [2], and because distant-carry and conditional-sum adders seem to approach the ultimate in speed, I felt that a detailed general analysis of skip-carry adders was unnecessary, and that a single numerical example (Table I) would suffice to demonstrate my point.

The correspondence, by the way, should not be taken as a criticism of the skip-carry concept. It is, rather, a criticism of the evaluation of that concept.

REFERENCES


The Fabrication of Low Resistances at Liquid Helium Temperatures*

The operation of linear cryogenic amplifiers, as well as other cryotron devices, often requires resistances that are extremely small, but nonzero. One means of obtaining such a resistance is to construct it of a short length of copper wire. It is then necessary to know the value of the resistivity of copper at liquid helium temperatures. This resistivity is considerably lower than the room temperature value, and it will vary with the impurity levels, and somewhat with the temperature. A range of values for resistivity, which has been obtained experimentally, will be given here. This range should not be considered to represent the upper and lower limits of resistivity available, but just to represent a small sample of values. These values are presented as a first approximation to the actual resistivity and should be used as such.

$$1.2 \times 10^{-4} \text{ohm-cm} \leq \rho \leq 1.8 \times 10^{-4} \text{ohm-cm}$$

The copper wire used in these measurements was of "thermocouple grade."

When making soldered connections to these resistances care must be taken since the contact resistance resulting from improperly soldered connections may be many times the value of the desired load resistance. (There may be applications where load resistance in the order of $10^{-4}$ ohms or smaller is desired.) Contact resistances that are usually negligible become important in such cases. If clean oxidized leads, which are carefully tinned, are used, these contact effects can be greatly reduced.

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