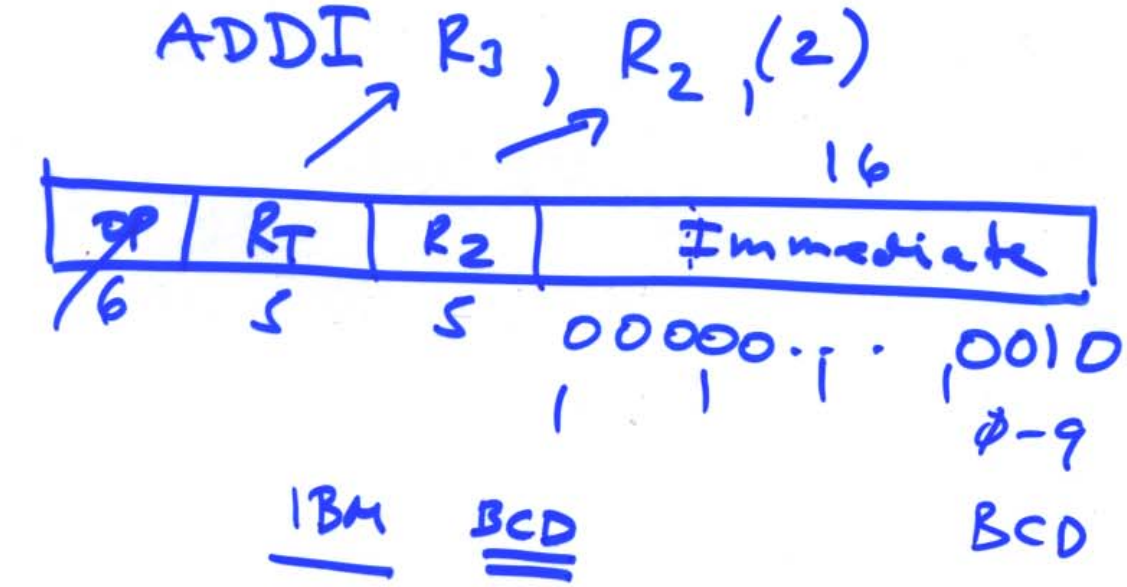
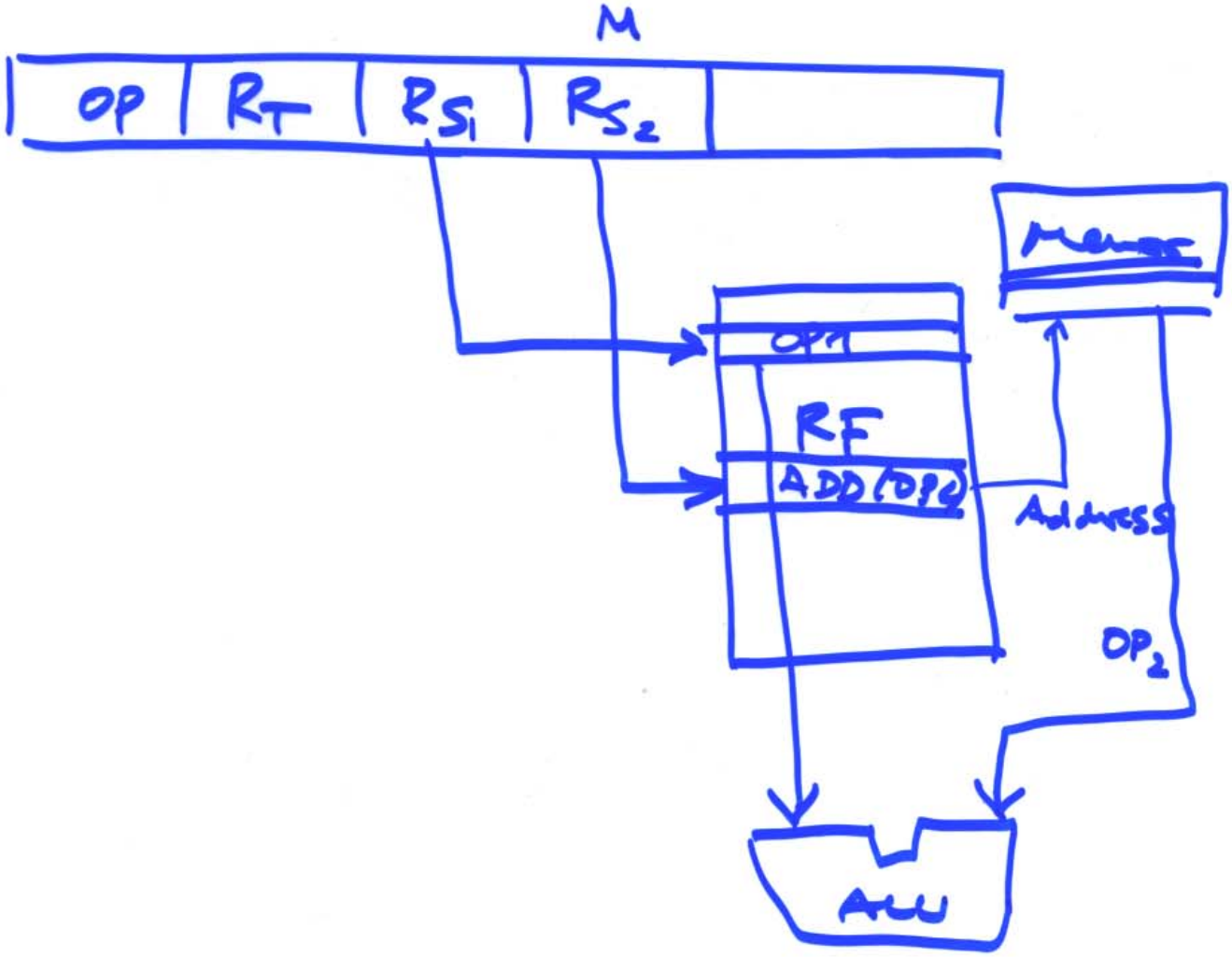

ADDI R3, R2, (2)
16
OP
RT
R2
Immediate
6
5
5
00000 . . . 0010
Ø-9
IBM
BCD
BCD


M
OP
RT
RS1
RS2
Memory
OP
RF
ADD(OP2)
Address
OP2
ALU

- No of Ops ?
  3, 2, 1, 0

- Where are the opd's

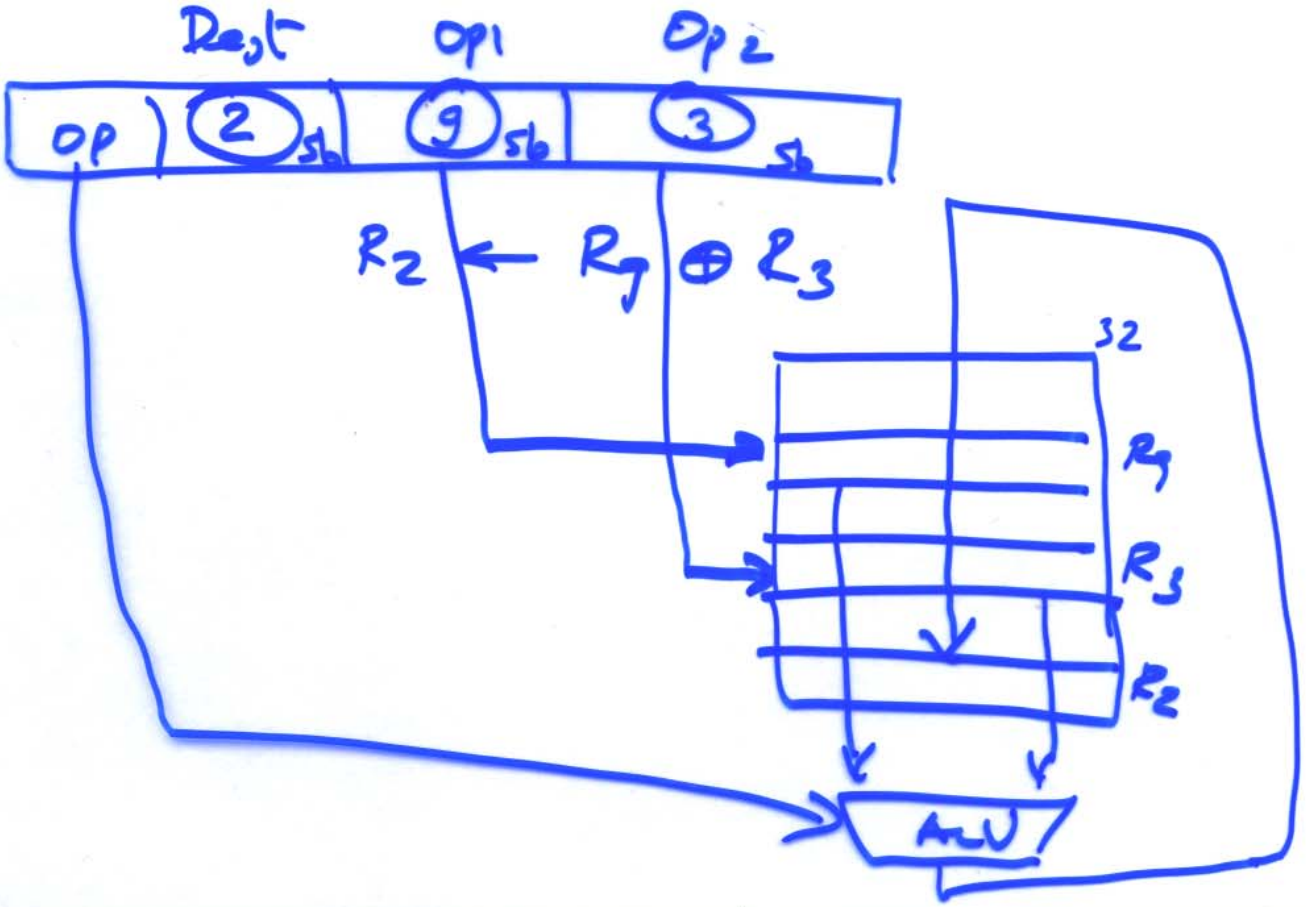
$R \leftarrow R \circ R$

$R \leftarrow R \circ M$

$R \leftarrow R \circ M$

$M \leftarrow M \circ M$

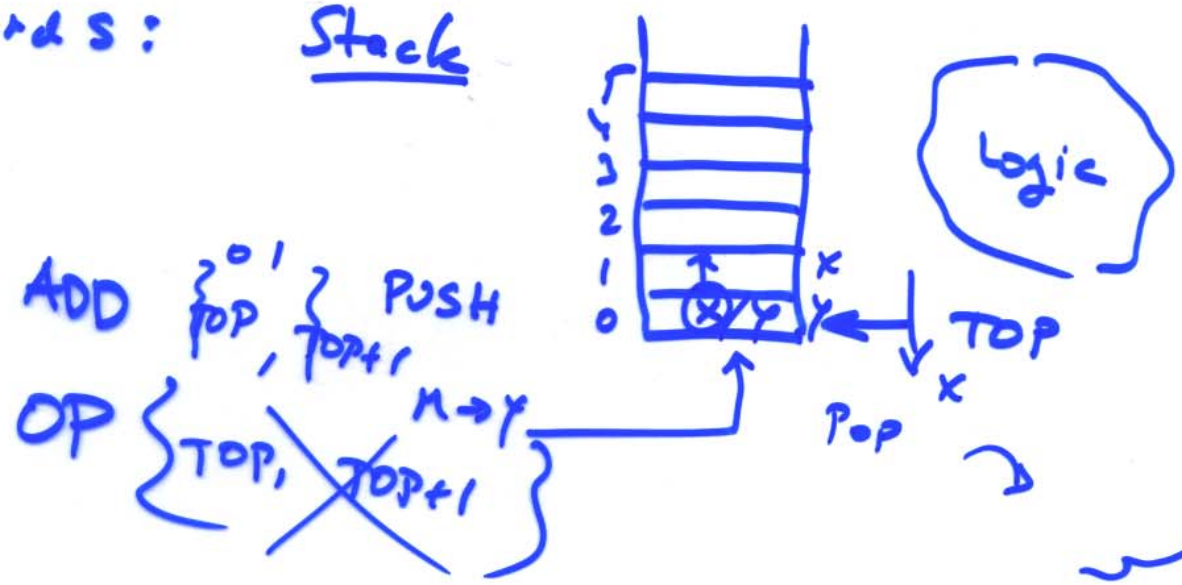
$M \leftarrow R \circ R$



Instructions

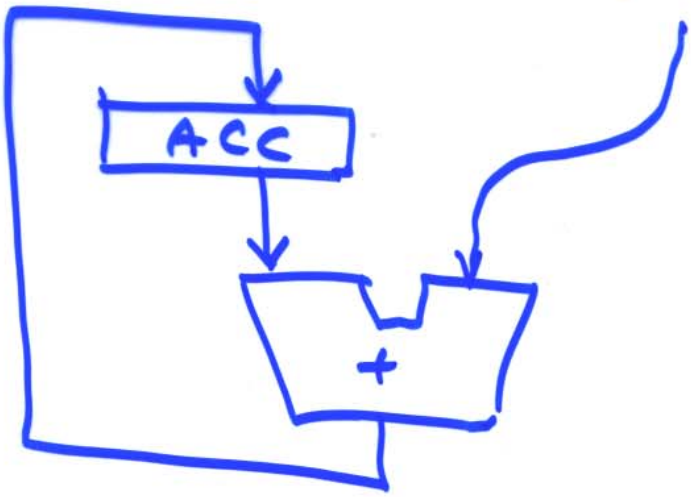
Classification of machines:

0 opnds: Stack



1 - Operand

$Acc \leftarrow Acc + \begin{Bmatrix} R \\ M \end{Bmatrix}$



2 - opnds

$R_1 \leftarrow R_1 \oplus \begin{Bmatrix} R \\ M \end{Bmatrix}$

3 - opnds:

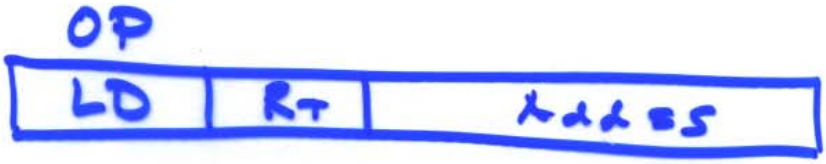
$\begin{Bmatrix} M \\ R_3 \end{Bmatrix} \leftarrow \begin{Bmatrix} M \\ R_2 \end{Bmatrix} \oplus \begin{Bmatrix} M \\ R_1 \end{Bmatrix}$

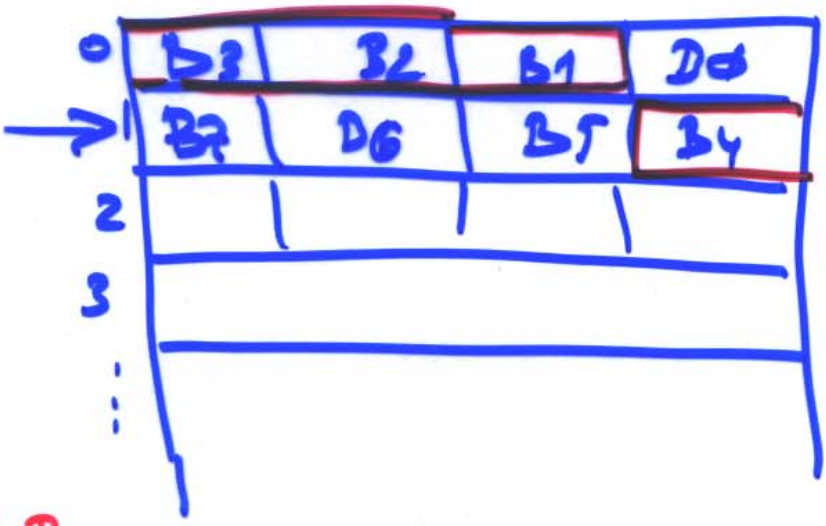
Types of Instructions

(A) Movement of Data

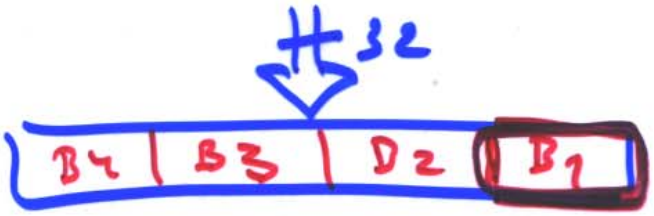
LD, ST

R ← M M ← R

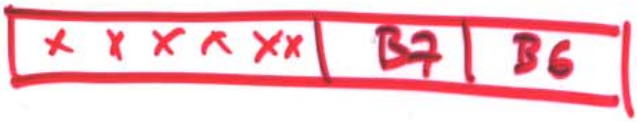


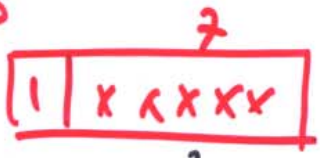


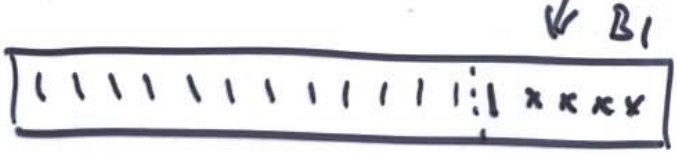
LB



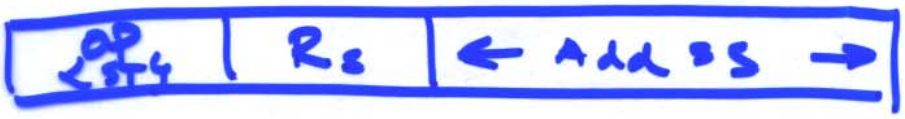
LHW







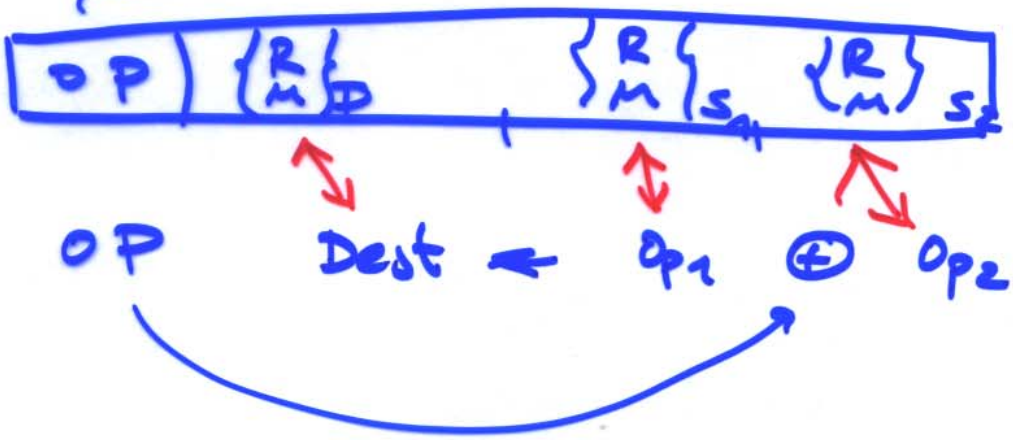
STORE ST R_x & M.. }



$R_s \rightarrow$ M & Address }

(b) OPERATIONS: Arith / Logical

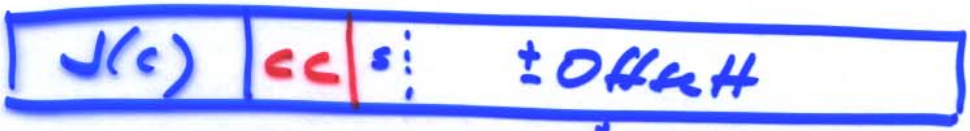
{ ADD, SUB, INC, DEC, MLT, DIV ...
OR, XOR, AND, NOT ... }



(c) Change Sequence of the Program

JMP < J Unconditional

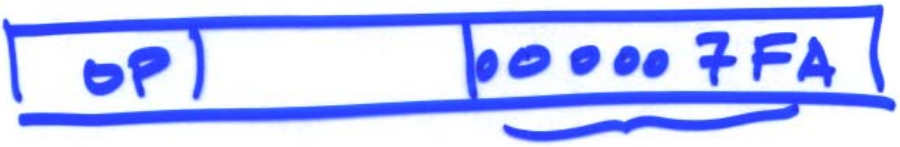
JC Conditional



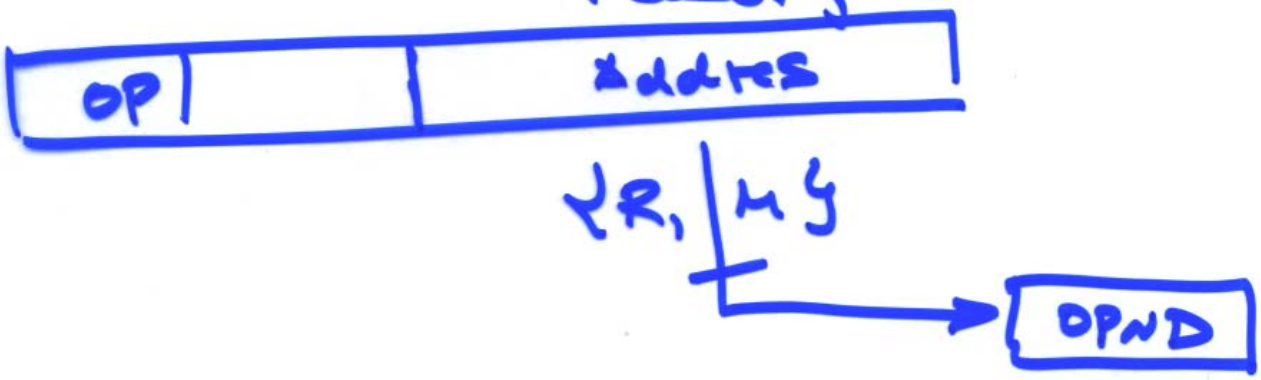
(D) Control / System

Addressing modes :

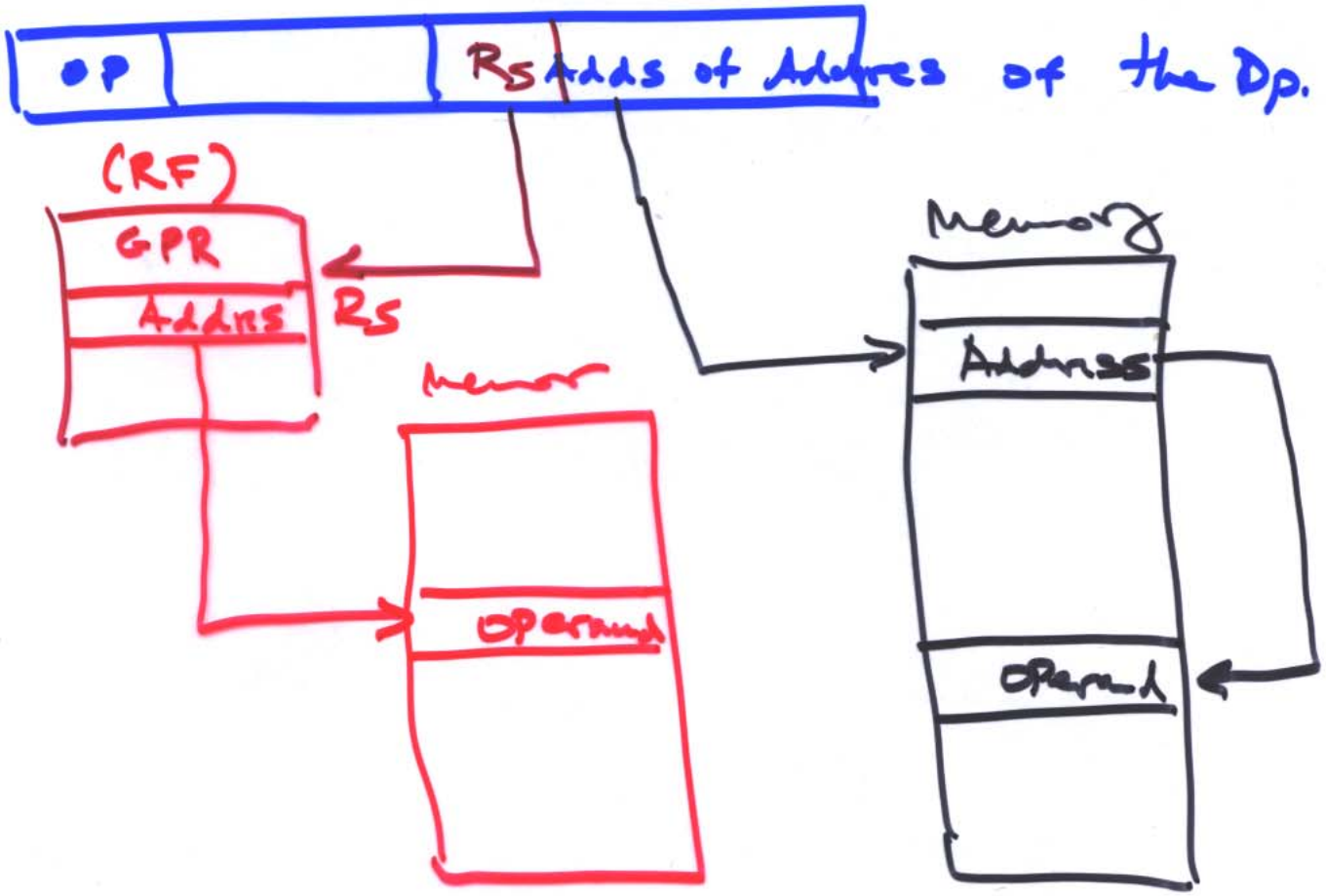
(1) Absolute / Immediate



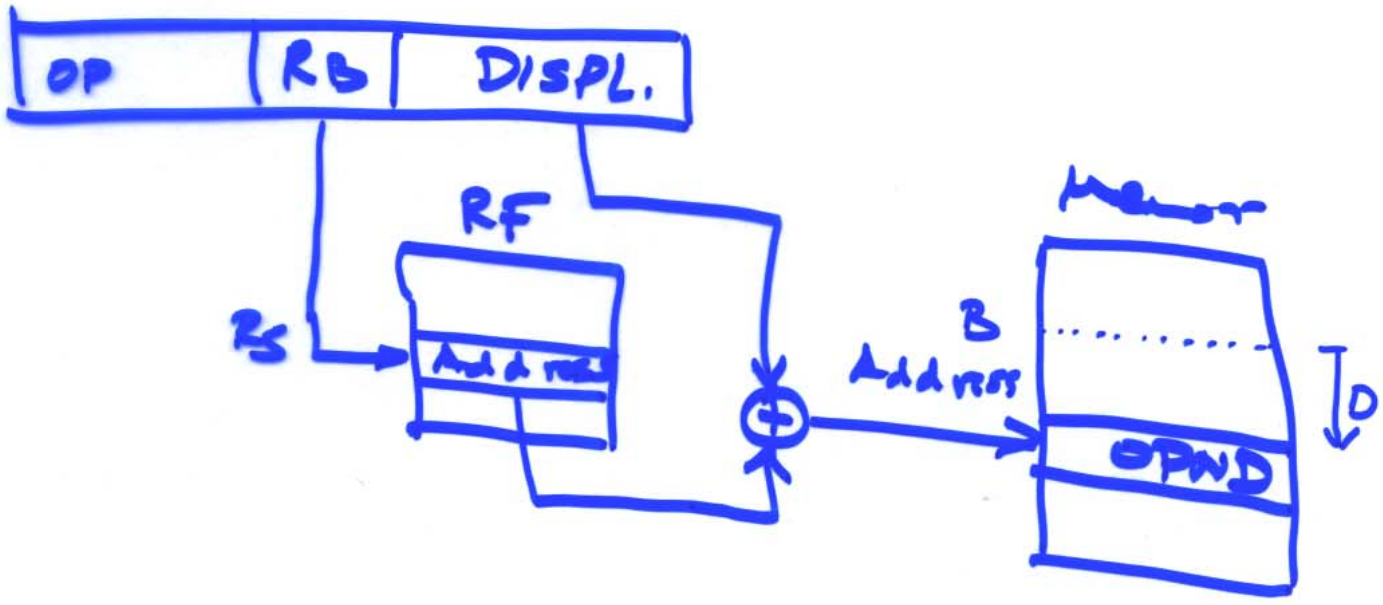
(2) Direct < Register / Memory



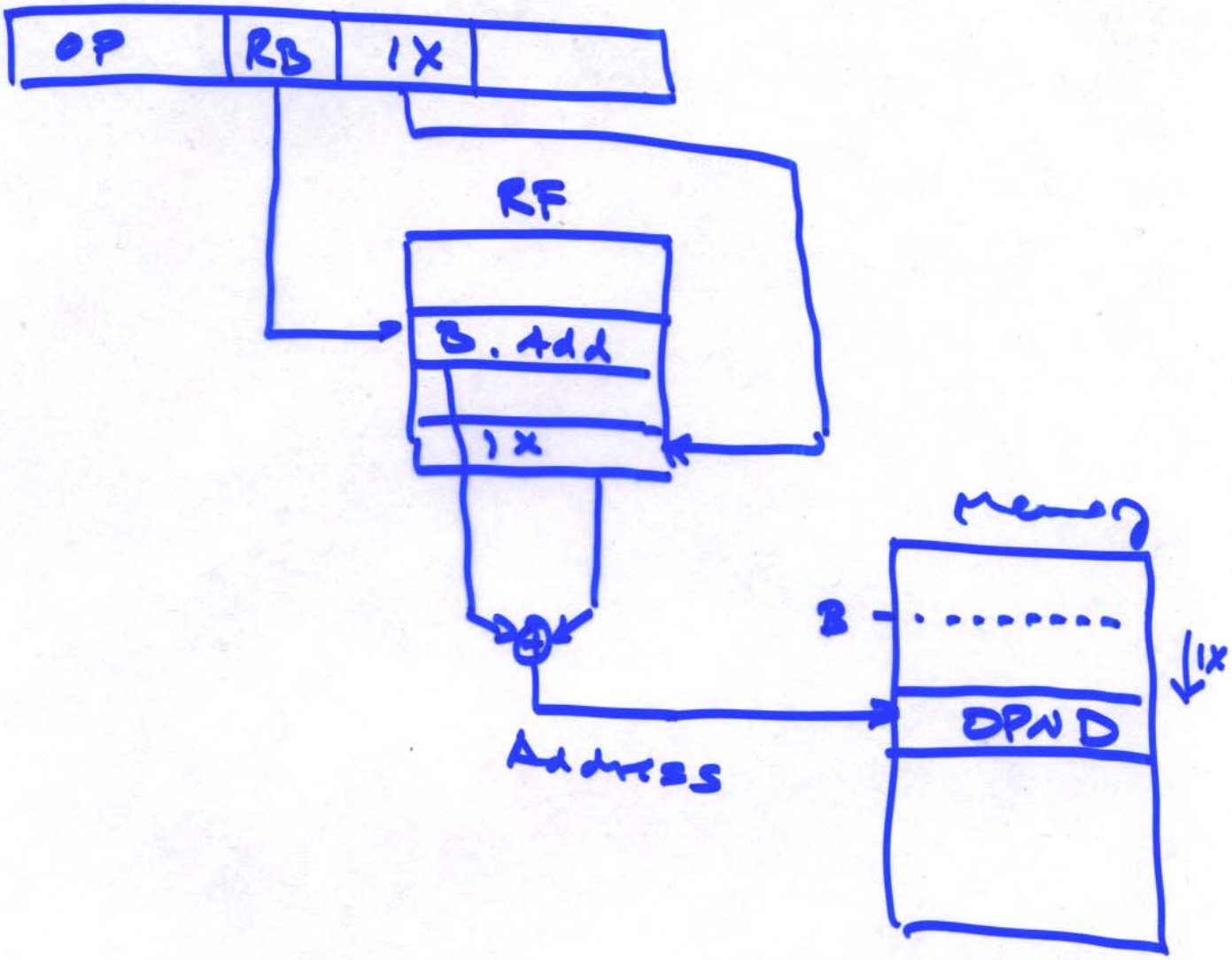
(3) Indirect Addressing < R Indir
M Indirect

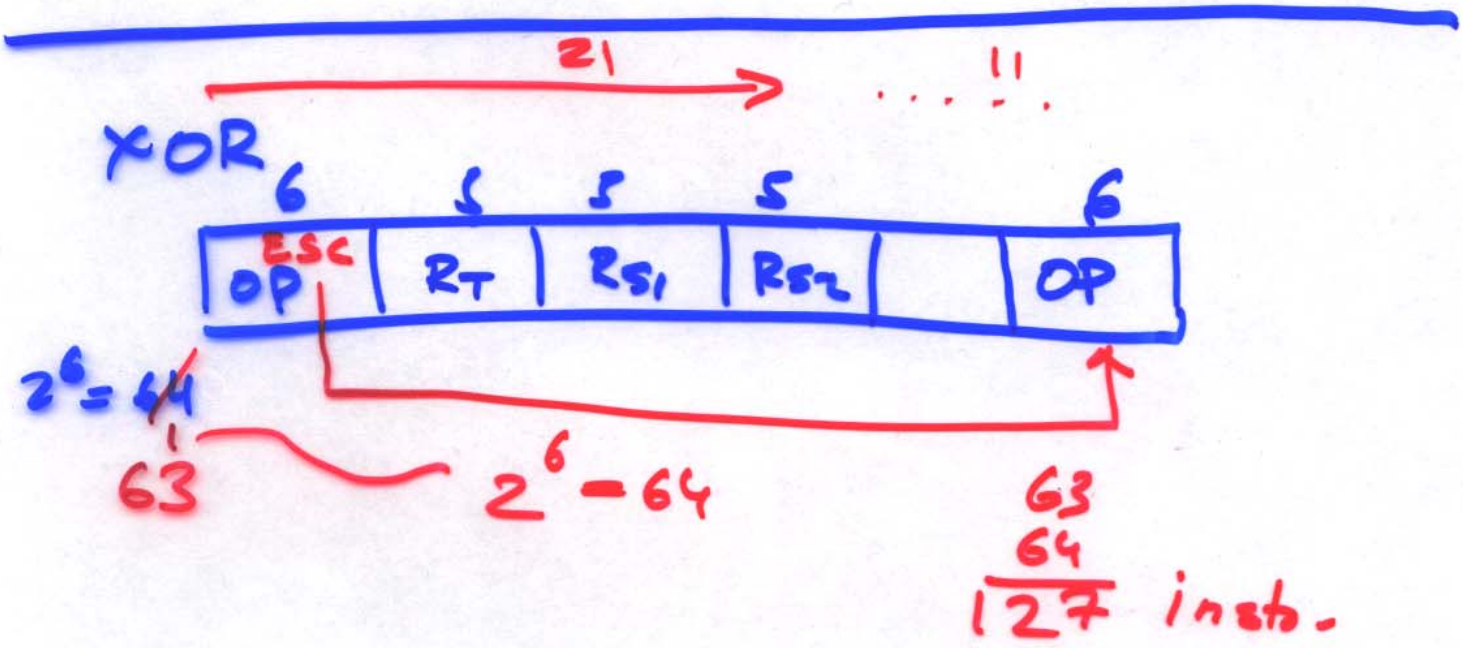


(4) Base + Disp



(5) Base + Index


OP
RB
IX
RF
B. Add
IX
Memory
B
IX
OPND
Address


21
11
XOR
6
5
5
5
6
OP
Esc
RT
RS1
RS2
OP
$2^6 = 64$
63
$2^6 - 64$
63
64
127 instr.