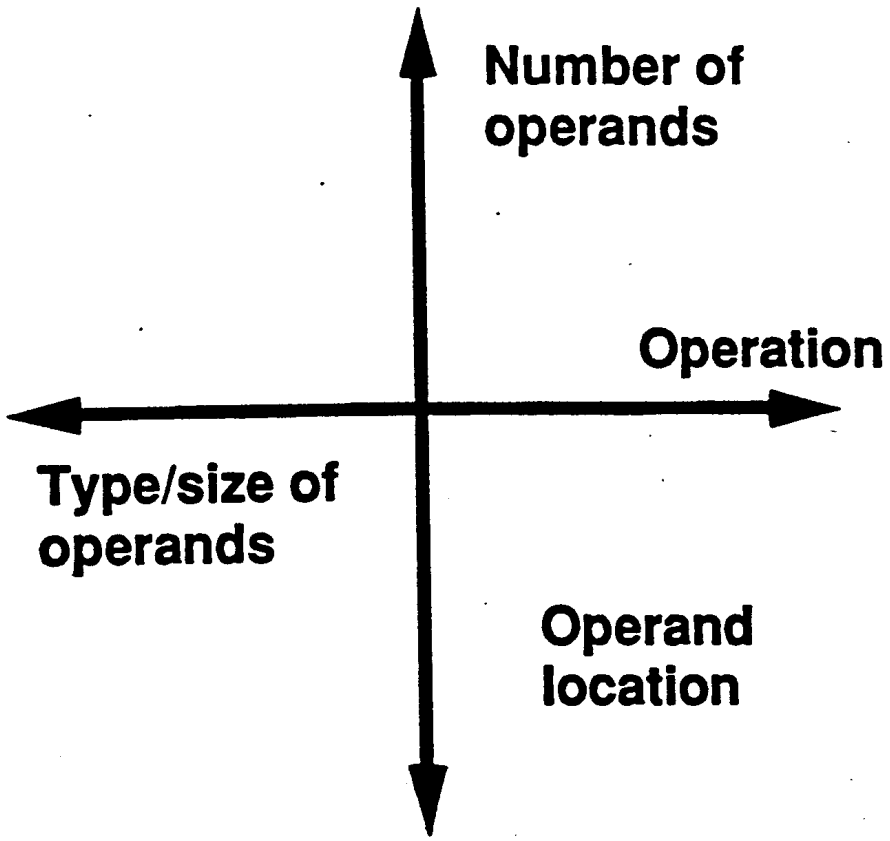
Instruction Design (Architecture) ISA

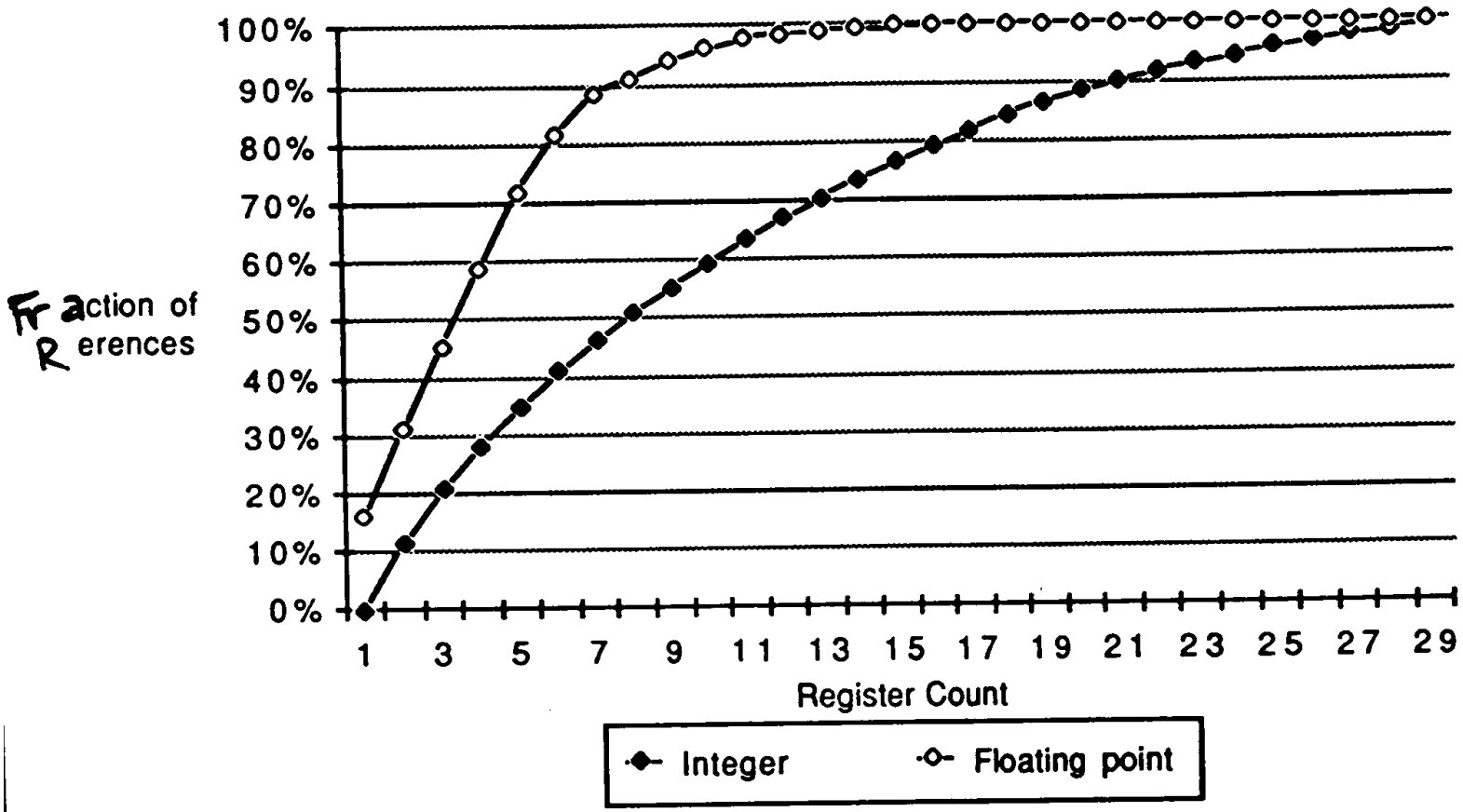
to the detailed specifics of a machine. Any use of the word architecture will be generic and cover all three aspects.

Key Structural Concepts

Typical instruction format:

We can classify each instruction in a three-dimensional space as shown below:




100%
90%
80%
70%
60%
50%
40%
30%
20%
10%
0%
Fraction of References
1 3 5 7 9 11 13 15 17 19 21 23 25 27 29
Register Count
Integer
Floating point

Typical Instruction Operations

Data Movement	Load (from memory) Store (to memory) memory-to-memory move register-to-register move input (from I/O device) output (to I/O device) push, pop (to/from stack)
Arithmetic	integer (binary + decimal) or FP Add, Subtract, Multiply, Divide
Logical	not, and, or, set, clear
Shift	shift left/right, rotate left/right
Branch	unconditional, conditional
Subroutine Linkage	call, return
Interrupt	trap, return
Synchronization	test & set (atomic r-m-w)
String	search, translate

MIPS: Instruction Classes

- Load and Store
- Arithmetic/Logic/Shift (including register-register moves)
- Control Transfers (branches, subroutines)
- R/W Control Registers (privileged)
- FP operate
- Coprocessor operate

Separated Load/Store and Reg/Reg Architecture Critical Ingredient of RISC architectures

All instructions exactly 32-bits long

Exactly two formats:
three register operands OR one register & one memory operand

Clasification by the number of Operands

- 0 - Operand Machines - Stack Machines (HP3000)
- 1 - Operand MAchines - Accumulator machines (one operand is always implicitely assumed to be in the accumulator ACC)
- 2 - Operand Machies R1 <- R1 * R2 (One of the source registers is also a destination register - Target)
- 3 - Operand Machines : R1 <- R2 * R3 (Destination / Target Register is explicitely specified - easyer on the Compiler)

Clasification by the Location of the Operands

- R - M : Register to Memory Instructions
  most of the machines: IBM 360/370 Architecture

- M - M : Memroy to Memory Instructions (Architectures)
  VAX - 11 Instructions etc. (some S/360)

- R - R register to Register Machines (Load/Store)
  (RISC Machines)

IF ID

OAG: Difference between R-R instructions

M-R Instructions

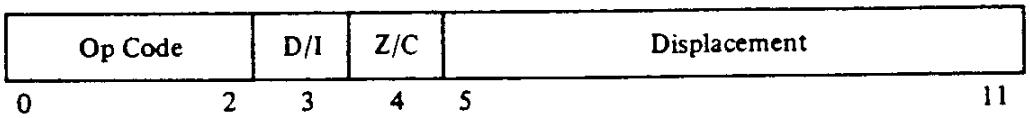
M-M Instructions

R - R :

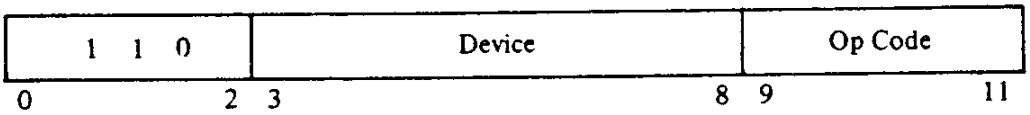
R - M :

M - M :

Memory Reference Instructions

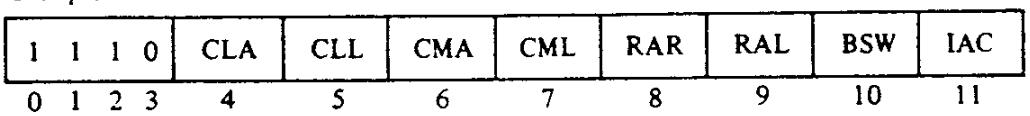


Input/Output Instructions

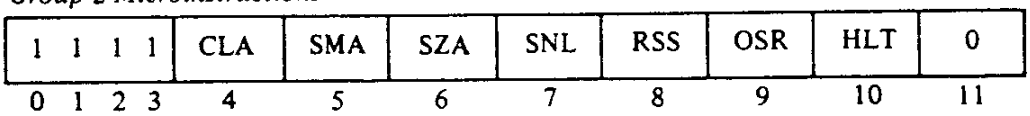


Register Reference Instructions

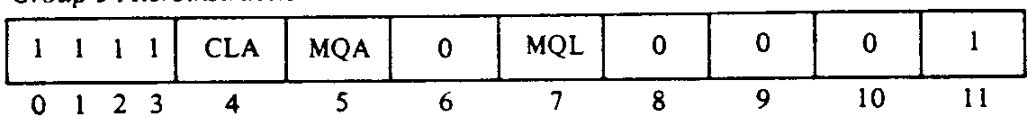
Group 1 Microinstructions



Group 2 Microinstructions



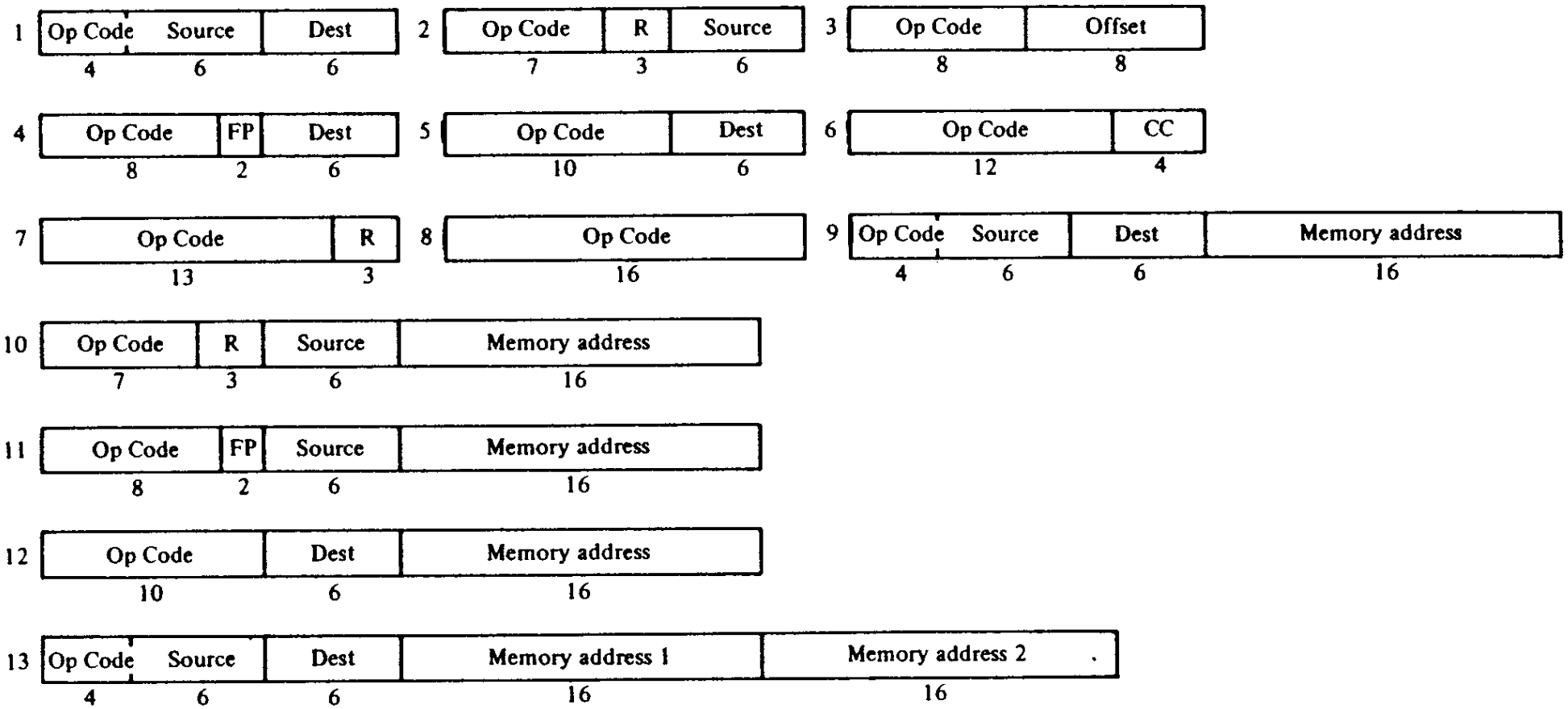
Group 3 Microinstructions



Mnemonics

CLA = CLear Accumulator
CLL = CLear Link
CMA = CoMplement Accumulator
CML = CoMplement Link
RAR = Rotate Accumulator Right
RAL = Rotate Accumulator Left
BSW = Byte SWap
IAC = Increment ACcumulator
SMA = Skip on Minus Accumulator
SZA = Skip on Zero Accumulator
SNL = Skip on Nonzero Link
RSS = Reverse Skip Sense
OSR = Or with Switch Register
HLT = HaLT
MQA = Multiplier Quotient into Accumulator
MQL = Multiplier Quotient Load

FIGURE 9-2. PDP-8 instruction formats.



Source and dest each contain a 3-bit addressing mode field and a 3-bit register number;
FP is 1 of the floating point registers 0, 1, 2, or 3;
R is 1 of the general registers;
CC is the condition code field

FIGURE 9-4. Instruction formats used on the PDP-11. The numbers indicate the field lengths.

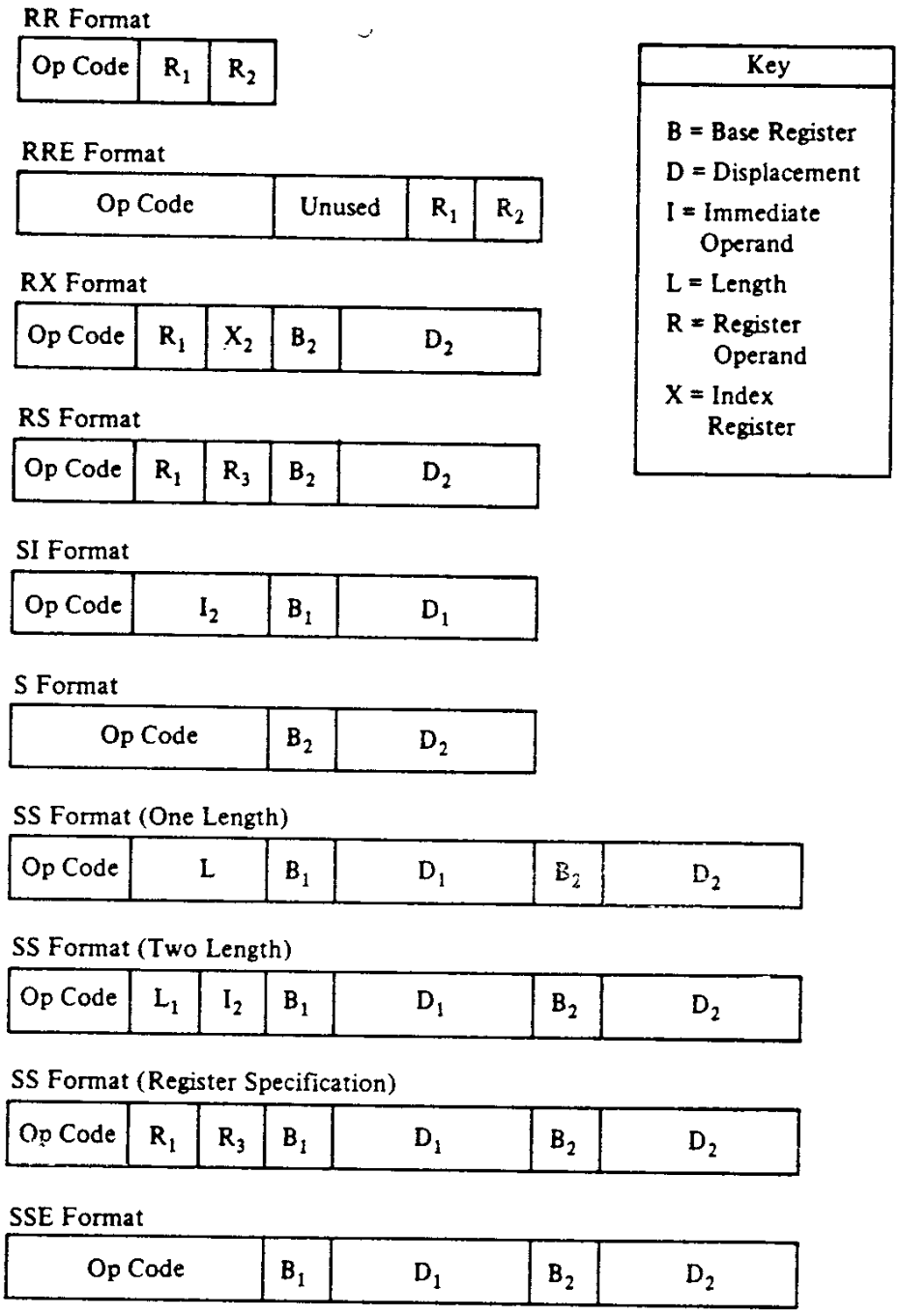


FIGURE 9-5. IBM S/370 instruction formats.