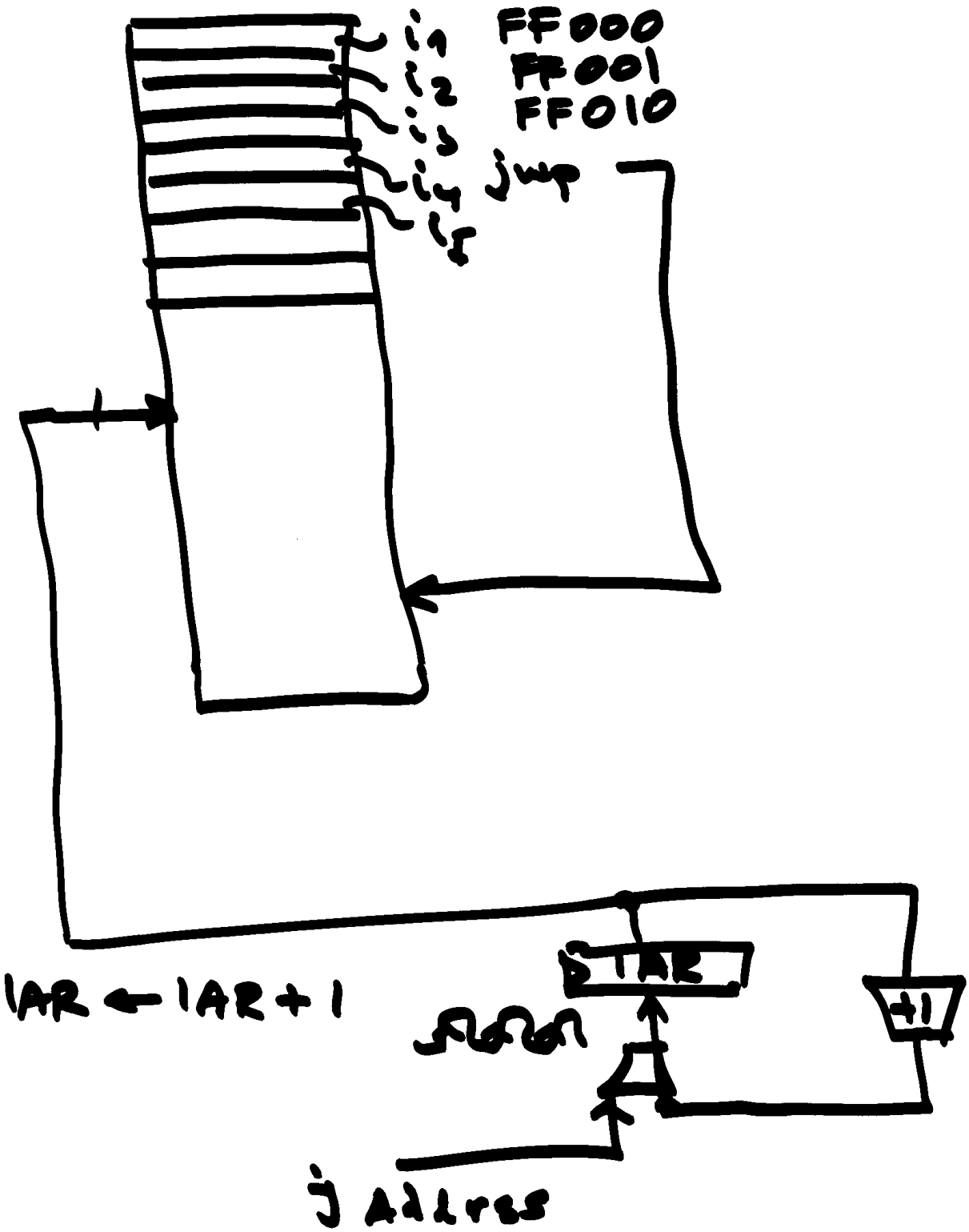
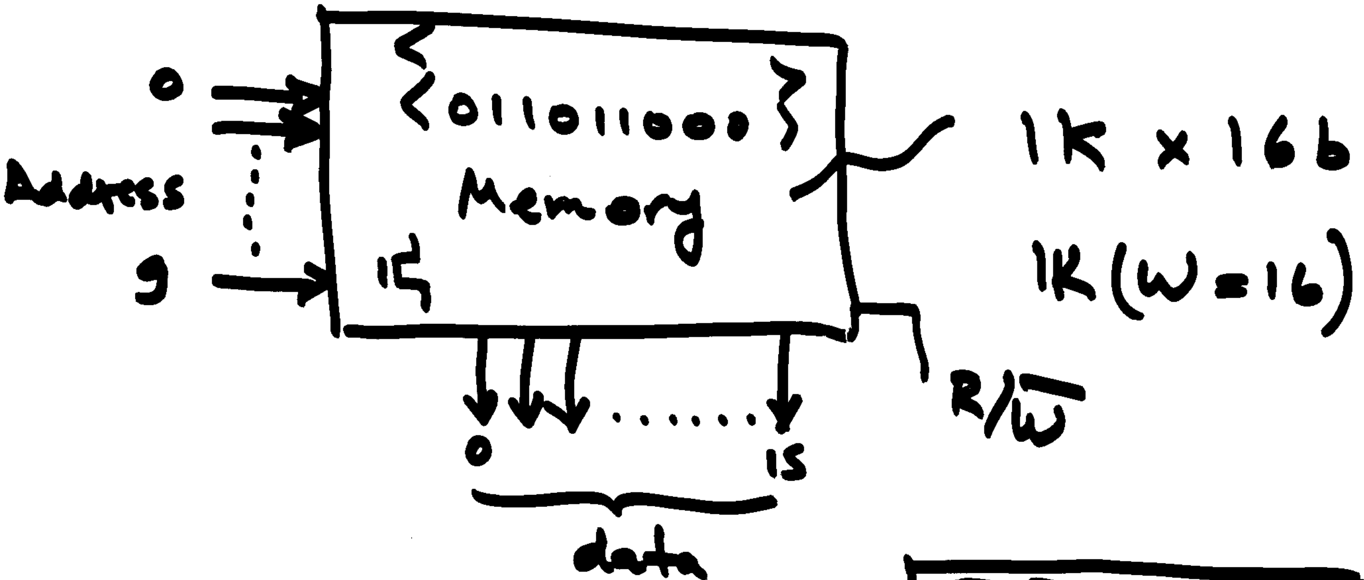
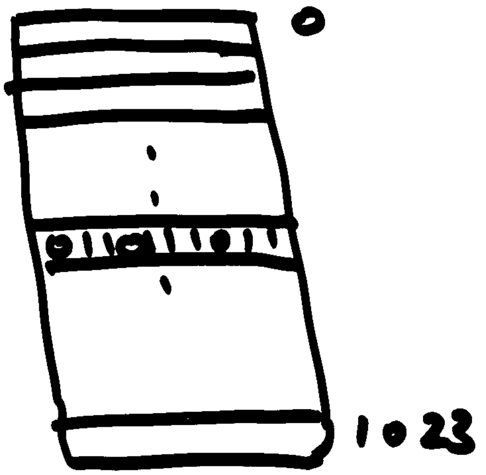
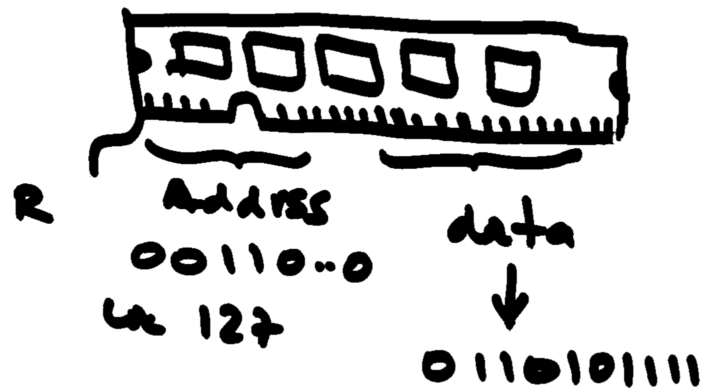
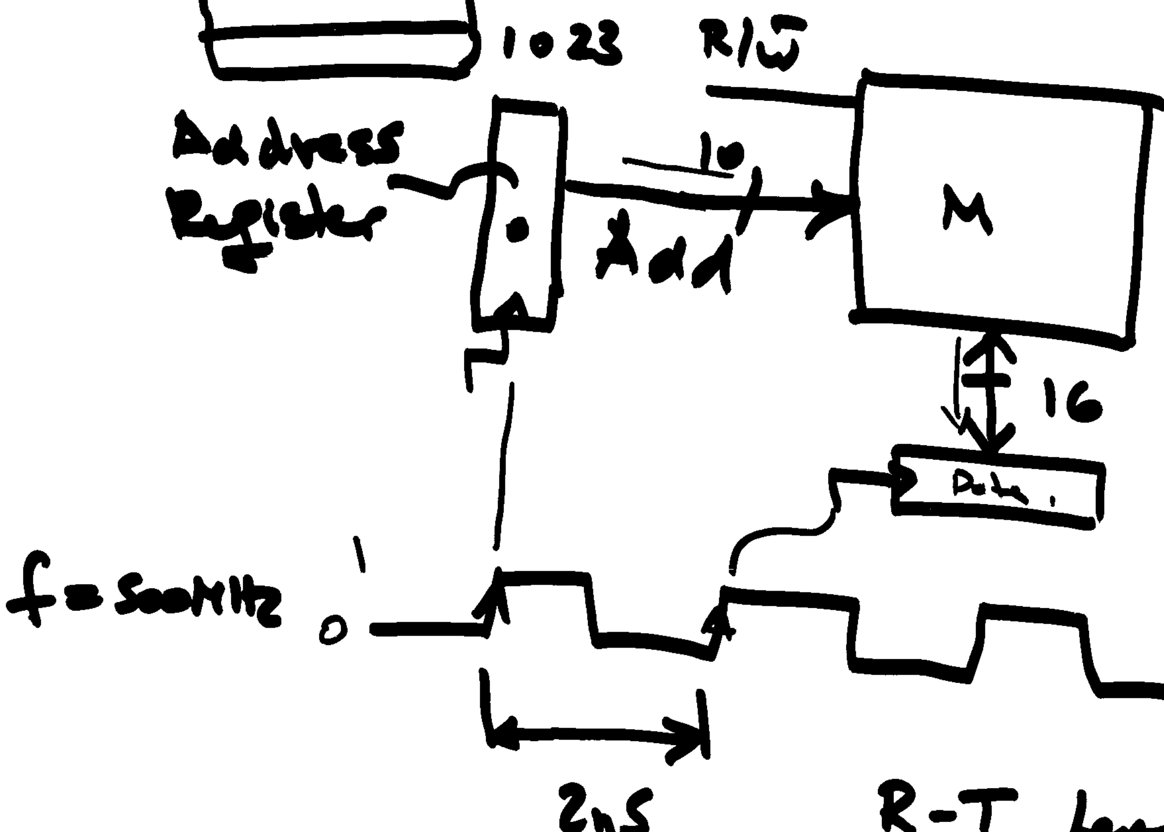

i1
i2
i3
i4
i5
FF000
FF001
FF010
jump
IAR ← IAR + 1
STAR
+1
j address


0
Address
9
{011011000}
Memory
1K x 16b
1K(W=16)
R/$\overline{W}$
0
15
data


0
0110110111
1023


R
Address
00110..0
127
data
0110101111


R/$\overline{W}$
Address Register
10
Add
M
16
Data
f = 500MHz
0
2nS

R-T Level

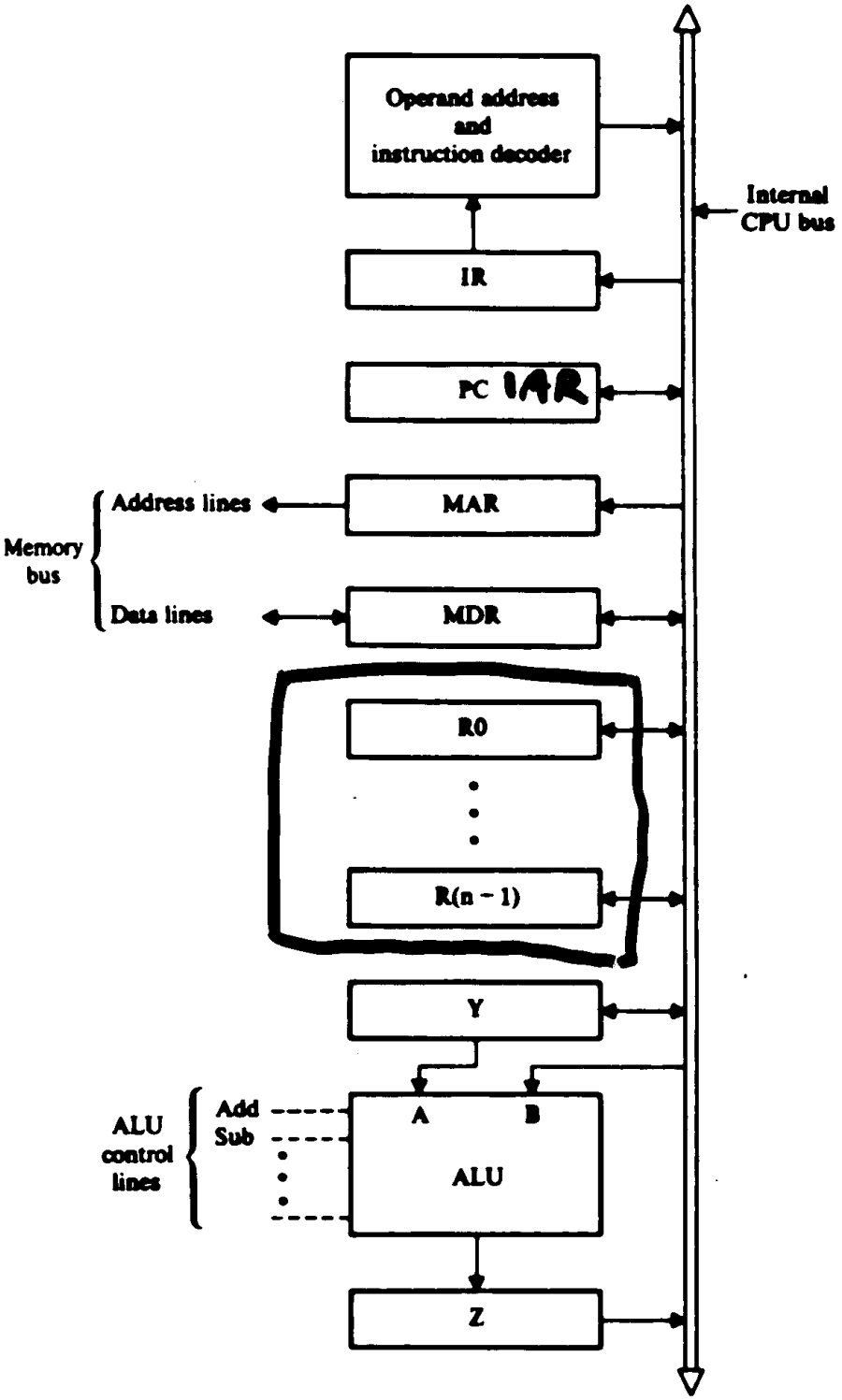


Figure 4.1 Single-bus organization of the data paths inside the CPU.

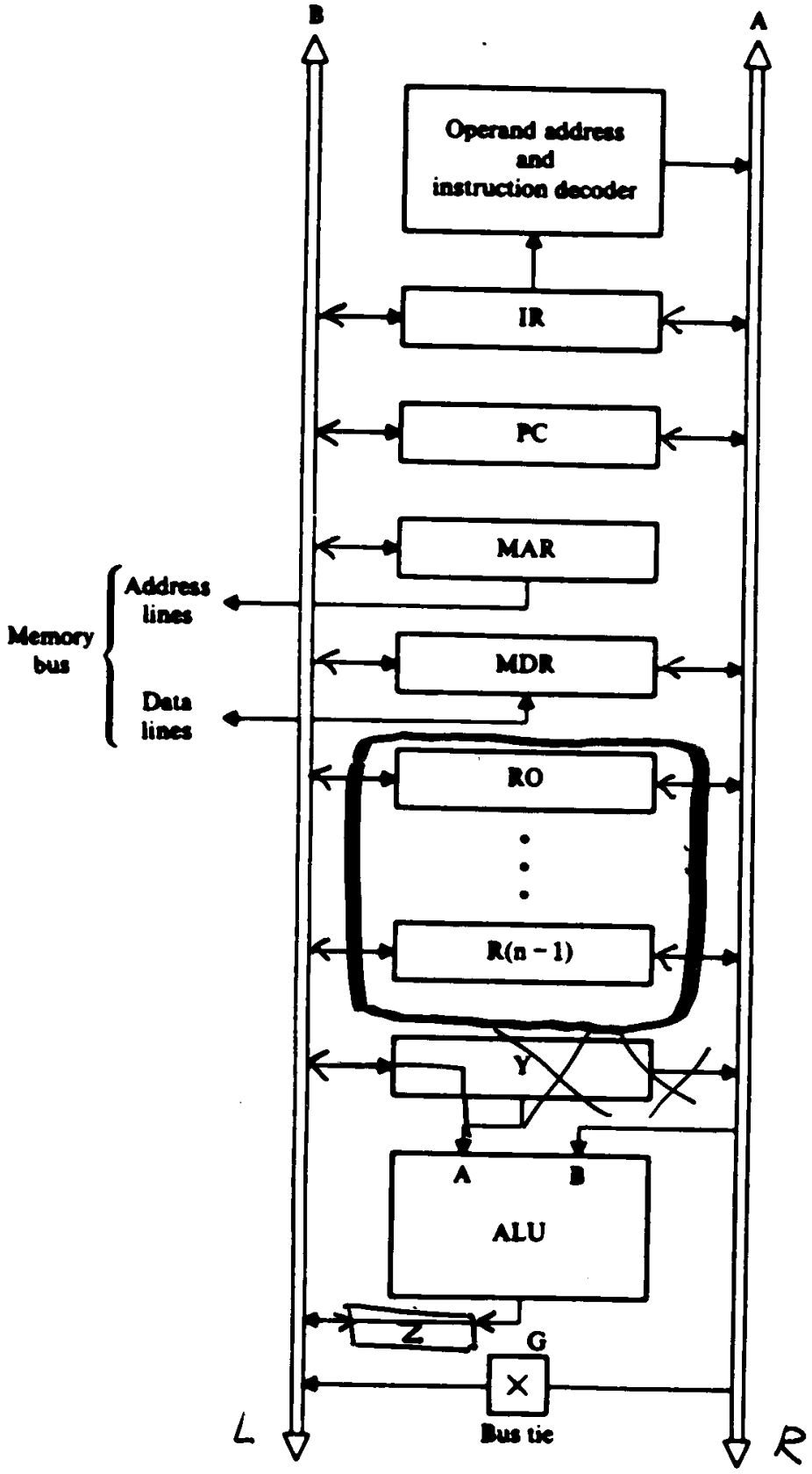


Figure 4.6 Two-bus structure.

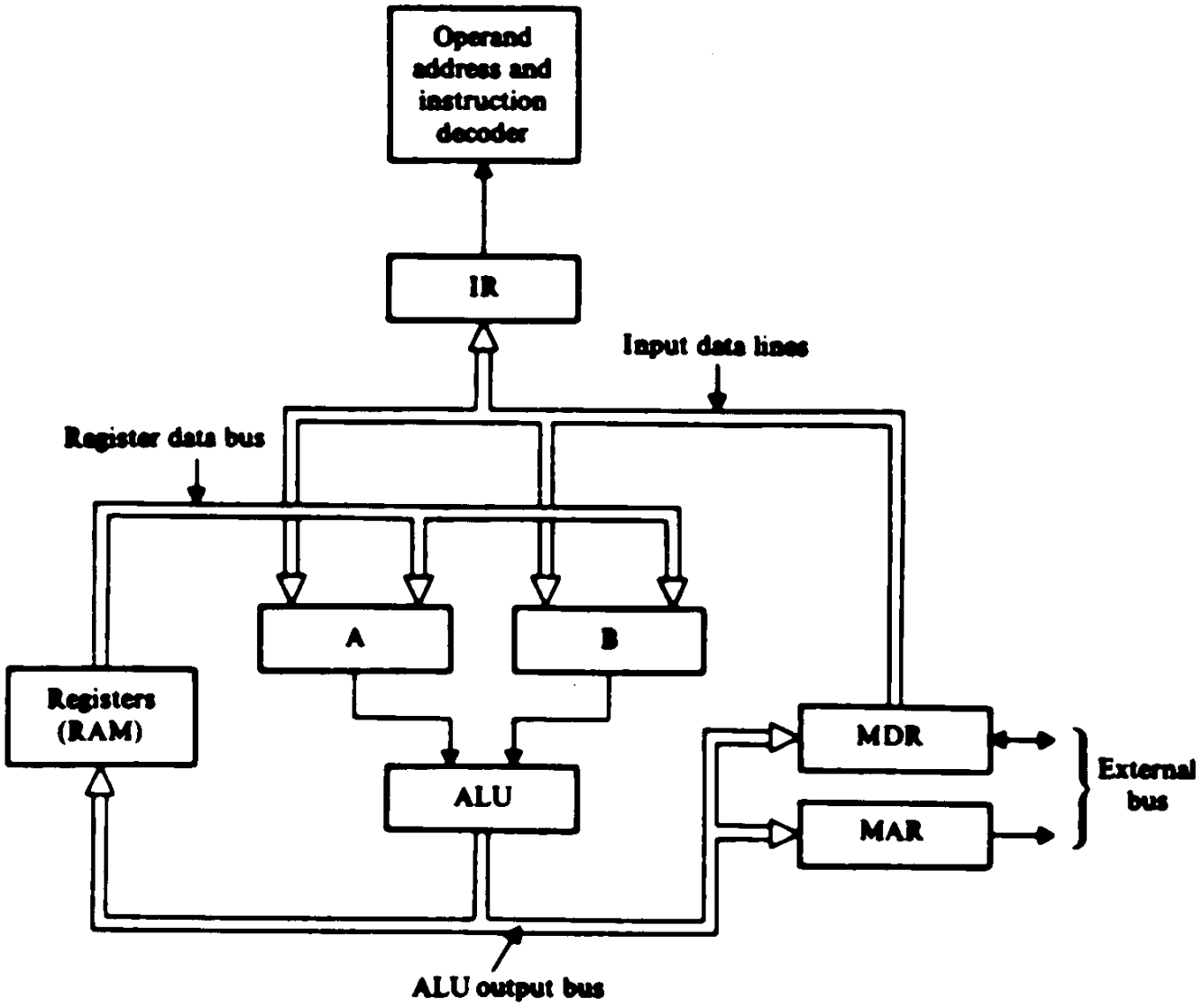
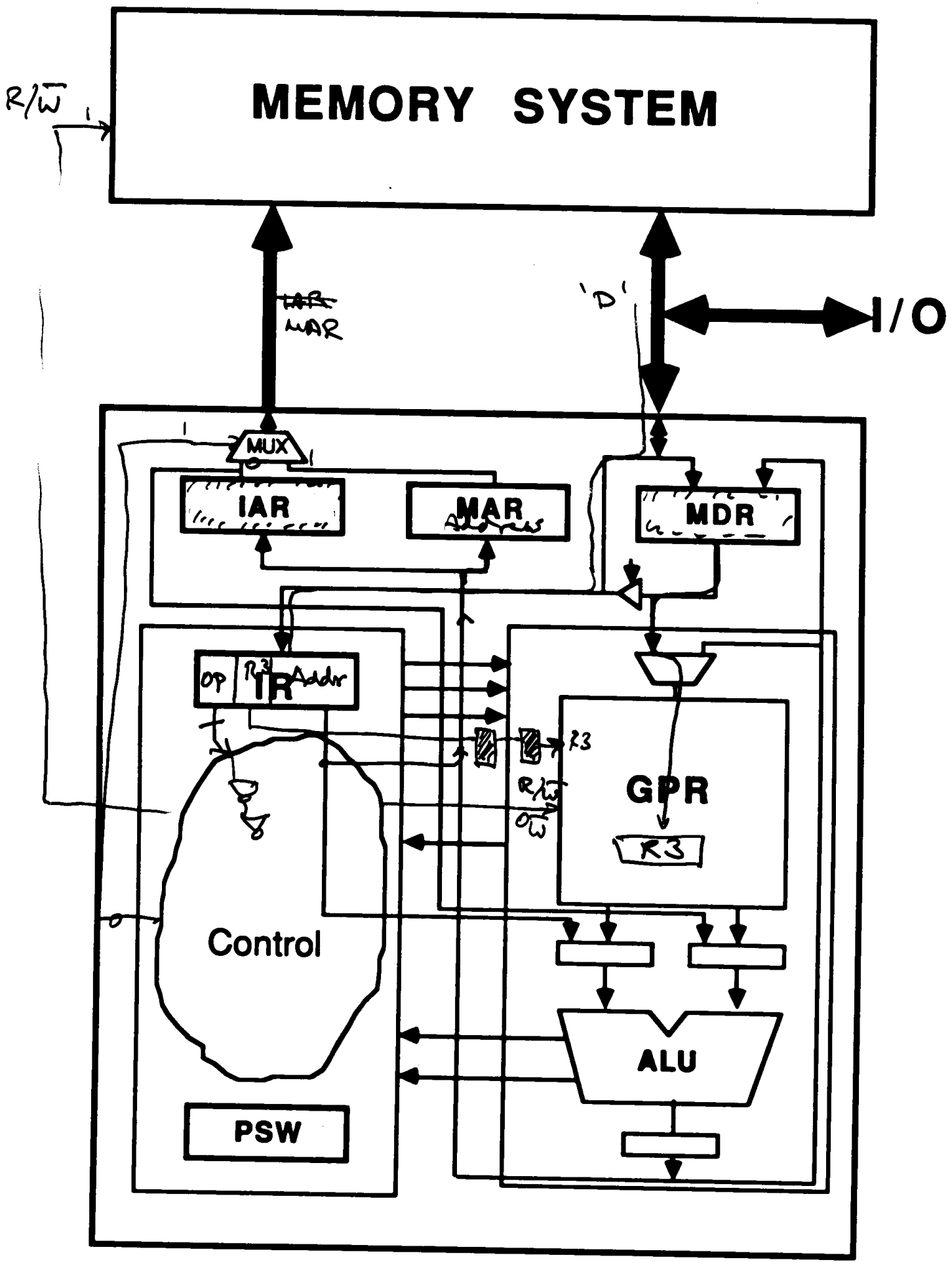
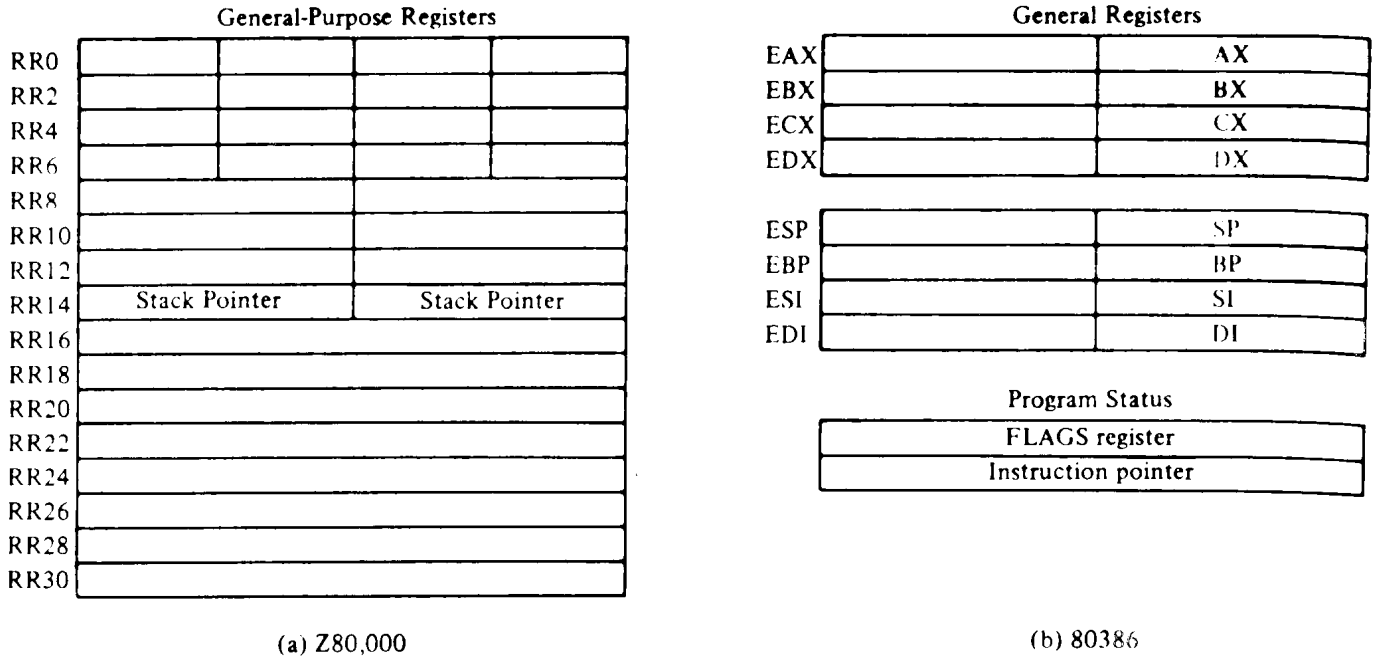


Figure 4.7 Three-bus structure.


MEMORY SYSTEM
R/W
MAR
'D'
I/O
MUX
IAR
MAR
MDR
op
R3
IR
Addr
R3
R/W
GPR
R3
Control
ALU
PSW

CPU: Concepts, Organization



(a) Z80,000 (b) 80386

FIGURE 10-5. Register organization extensions for 32-fix microprocessors

CPU: Concepts, Organization

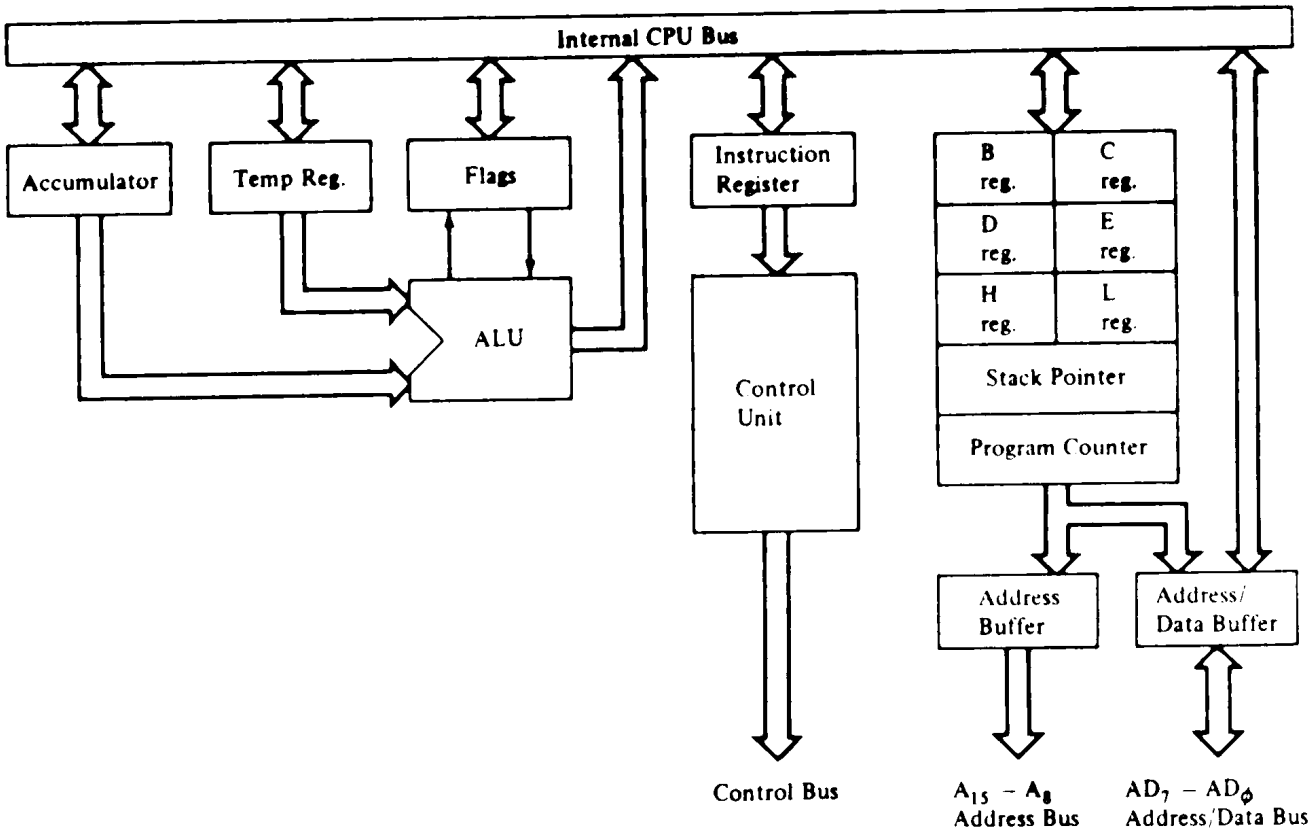


FIGURE 10-3. Simplified Intel 8085 organization.

CPU: Concepts, Organization

Instruction Formats (example):

Load/ Store:

Operation

Branch