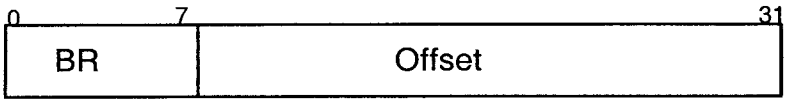
1. (20 pts) Compare 0,1,2, and 3 address machines by writing a program to compute:

   X=(A+BxC) / (D-ExF-GxH)

   for each of the four types of instruction sets. The available instructions are:

| **0-address** | **1-address** | **2-address** | **3-address** |
|---|---|---|---|
| Push M | Load ACC | Mov (R1 <- R2) | Mov (R1<-R2) |
| Pop M | Store ACC | | |
| Add | Add ACC | Add (R1<-R1+R2) | Add (R1<-R2+R3) |
| Sub | Sub ACC | Sub (R1<-R1-R2) | Sub (R1<-R2-R3) |
| Mul | Mul ACC | Mul (R1<-R1XR2) | Mul (R1<-R2xR3) |
| Div | Div ACC | Div (R1<-R1/R2) | Div (R1<-R2/R3) |

2. (25pts) Given is a Branch instruction BR

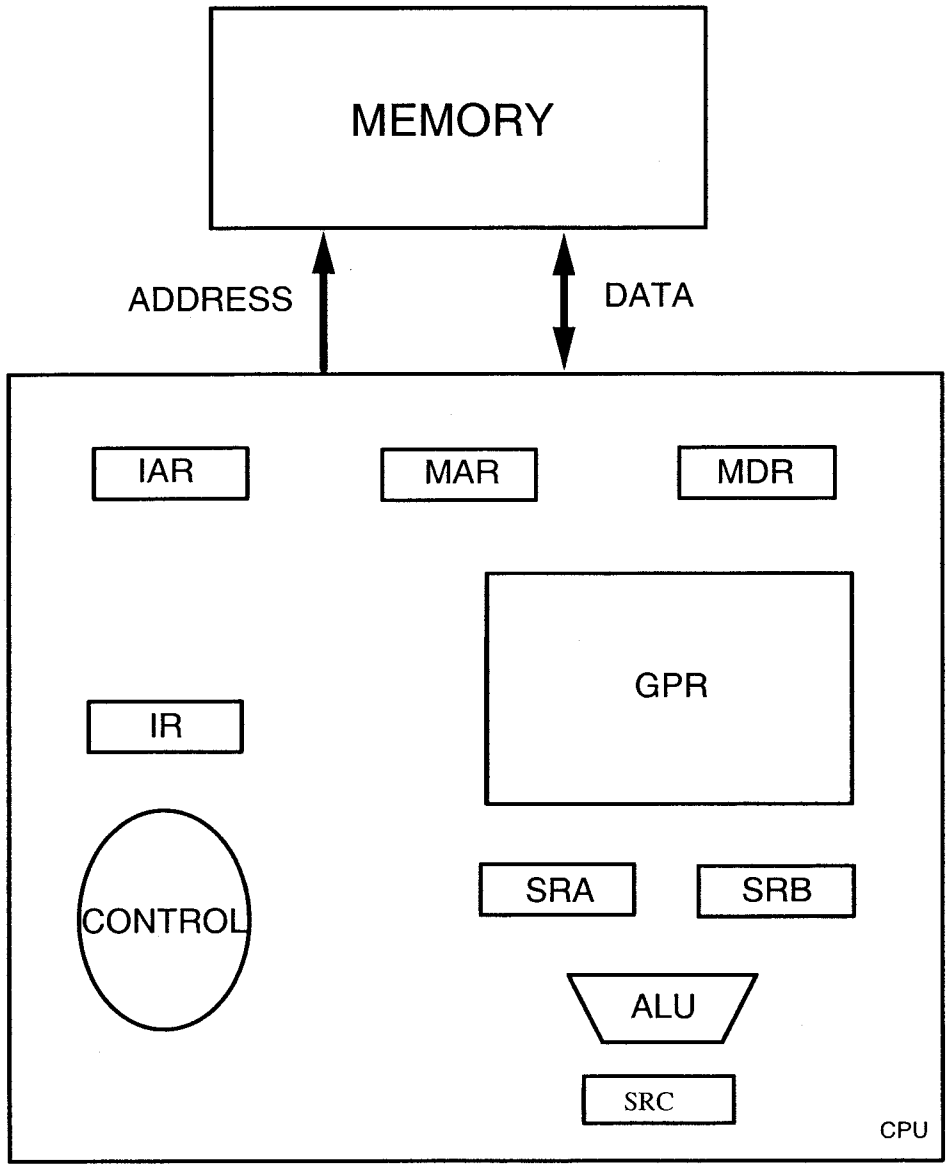



the address of the target instruction is specified in the instruction (in the IAR- relative mode) providing 24-bit displacement from the IAR.

(a) List cycle by cycle all the steps of this instruction

(b) Fill in all the necessary paths (busses) in the CPU diagram provided.

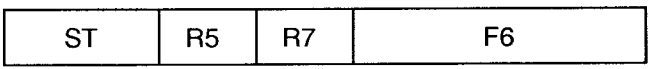
* there is no separate adder for branch address calculation, so ALU will be used for that purpose.



3. (15pts) Fill in the missing entries of the following table.

| Binary | Octal | Decimal | Hexadecimal |
|---|---|---|---|
| 110101 | | | |
| 11100110 | | | |
| | 01344 | | |
| | 666 | | |
| | | 99 | |
| | | 73 | |
| | | | A3 |
| | | | FD2 |

4. (15pts) Given is the Store instruction




the register file has 8 (32-bit) registers containing the following values:

R5 = FFA1  R7 = FF00

The memory is Byte addressable

(a) What are the address locations in memory that will be affected by this instruction ?

(b) List the values in those locations after the STORE instruction is executed ?