Unger and Tan's paper

There exists a flaw in Unger and Tan's paper. Identify the flaw and provide the correct solution. Highlight the affected equations. (enclose those pages of the paper with highlights).

S. H. Unger and C. J. Tan, "Clocking Schemes for High-Speed Digital Systems", IEEE Transaction on Computers, Vol. C-35, No. 10, pp. 880-895, October 1986.

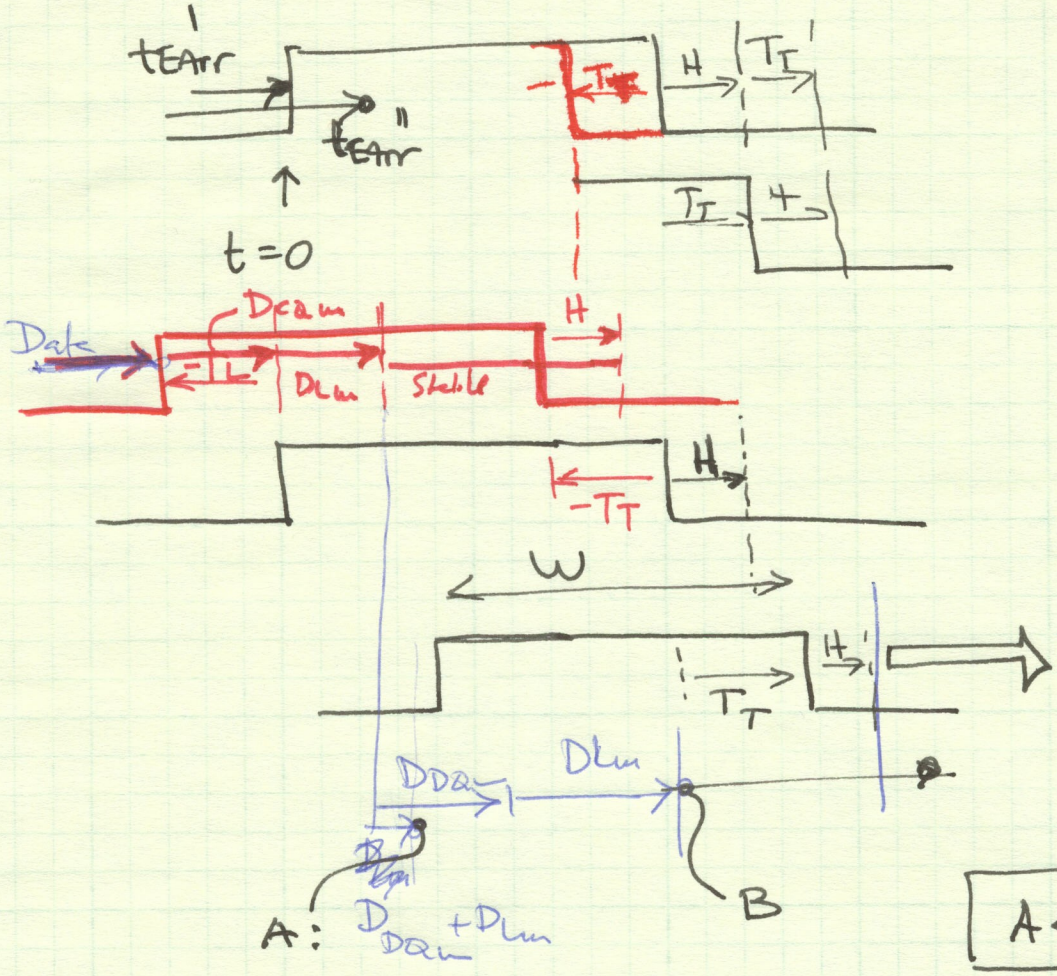
(*please see below the following pages class notes and personal correspondence with the authors*)

$$t_{DEARN} = \min\left\{ \underbrace{-T_L + D_{CQm} + D_{Lm}}_{A},\ \underbrace{t_{DEArr} + D_{DQm} + D_{Lm}}_{B} \right\} > W + T_T + H$$

A: clock first

B: data during the same clock

Satisfied if:



t_{DEArr}

$A < B$

$$t_{DEArr} + D_{DQm} + D_{Lm} > W + T_T + H$$

$$-T_L + D_{CQm} + D_{Lm} > W + T_T + H$$

$$\boxed{D_{Lm} > W + T_T + T_L + H - D_{CQm}}$$

Date: Sat, 2 Dec 95 8:38:34 EST
From: Stephen Unger <unger@cs.columbia.edu>
To: vojin@ece.ucdavis.edu (Prof. V.G. Oklobdzija)
Cc: unger@opus.cs.columbia.edu, tan@watson.ibm.com
Subject: Re: Clocking Scheme ..... , IEEE-TC
In-Reply-To: Your message of Thu, 30 Nov 95 10:27:25 PST
Message-ID: <CMM.0.90.2.817911514.unger@ground.cs.columbia.edu>

Vojin,

It is nice to hear from you again, and I thank you for the kind words about our
paper.

You raise an interesting question regarding the 3 expressions starting with the one after (13) on page 885. I believe they are all correct as they stand. There is, however, a confusing point having to do with the use of (1) (on p. 881) to derive the first of these.

Equation (1) specifies the LATEST time at which the output of a latch can change, as a function of the occurrence times of changes in the C and D signals, and the MAXIMUM values of the delays DCQ and DDQ (i.e. delays between D or C input terminals, respectively and the Q output). This is a valid expression, but it is less general than what is needed in the discussion under question. It correctly indicates the LATEST time for a Q-change, but what is needed on p. 885 is the EARLIEST time for a Q-change.

A slightly generalized version of (1) that can be used for both purposes is tQ=max[tC+DCQ, tD+DDQ]. This more general expression states that, if you know the EXACT values of the delays DCQ and DDQ (as well as the exact occurrence times of the changes in the C and D signals), then you can compute PRECISELY when Q will change. (Note that this is a POSTULATE, which we believe to be sufficiently valid for most real latches to be useful.) It states that the output change occurs EXACTLY when the effects of BOTH the C and D changes have passed thru the latch. The SLOWEST of these signals therefore determines the time of change. This explains why the max is taken. If we are interested in the EARLIEST time that Q may change, we STILL have to use the max, but now we use the MINIMUM values for the arguments of the max, namely tC+DCQm and tD+DDQm. This is what was done in deriving the p. 885 expressions. We should have used the more general form of (1) in the paper. (I just checked and saw that I did use that form in the abbreviated version of this material that appears in my book, Essence of Logic Circuits.)

Thank you for calling attention to this matter. It is a pleasure to know that our work is receiving such careful, intelligent scrutiny.

Best regards, and stay in touch.

Steve