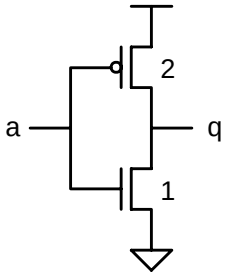
Take-Home Exam Solution #2

For problems 1-6, normalize each answer for g and p to following reference inverter. Use equal pull-up and pull-down sizing unless stated otherwise.



$$g = \frac{R_{gate} C_{in-gate}}{R_{inv} C_{in-inv}}$$

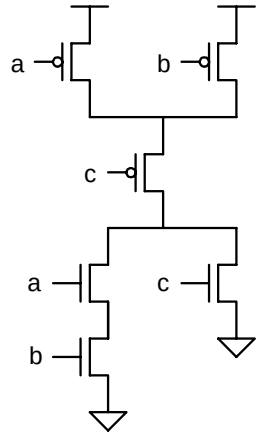
$$p = \frac{R_{gate} C_{p-gate}}{R_{inv} C_{in-inv}}$$

For this Exam:
$g_{up\text{-}inv} = g_{down\text{-}inv} = 1$
$p_{up\text{-}inv} = p_{down\text{-}inv} = 1$

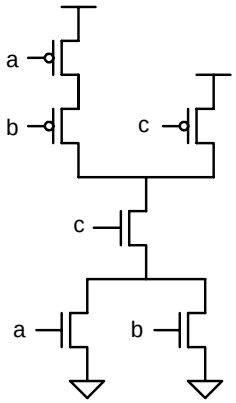
Problem 1:
Size each gate to have the same pull up and pull down resistance as the reference inverter. Calculate the logical effort (g_{up}, g_{down}, g_{avg}) and parasitic delay (p_{up}, p_{down}, p_{avg}) for each input of the following gates.

Note: $g_{avg} = \frac{1}{2}(g_{up}+g_{down})$
$p_{avg} = \frac{1}{2}(p_{up} + p_{down})$

(a)



(b)



For simplicity, size the above circuits to have the same effective sizing as the above inverter.

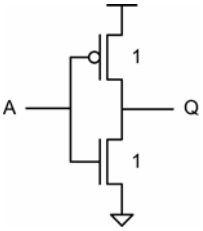
(a) AOI gate

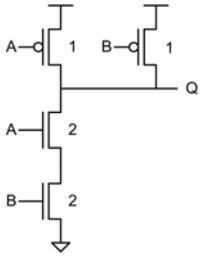
Input a, b:	$g_{up} = (1*6)/(1*3) = 2$	$g_{down} = (1*6)/(1*3) = 2$	$g_{avg} = 2$
Input c:	$g_{up} = (1*5)/(1*3) = 5/3$	$g_{down} = (1*5)/(1*3) = 5/3$	$g_{avg} = 5/3$

(b) OAI gate

Input a, b:	$g_{up} = (1*6)/(1*3) = 2$	$g_{down} = (1*6)/(1*3) = 2$	$g_{avg} = 2$
Input c:	$g_{up} = (1*4)/(1*3) = 4/3$	$g_{down} = (1*4)/(1*3) = 4/3$	$g_{avg} = 4/3$

Problem 2:
Calculate the logical effort (g_{up}, g_{down}, g_{avg}) for each input of the following asymmetric gates.





(a) Skewed Inverter
Input a: $g_{up} = (2*2)/(1*3) = 4/3$ $g_{down} = (1*2)/(1*3) = 2/3$ $g_{avg} = 1$

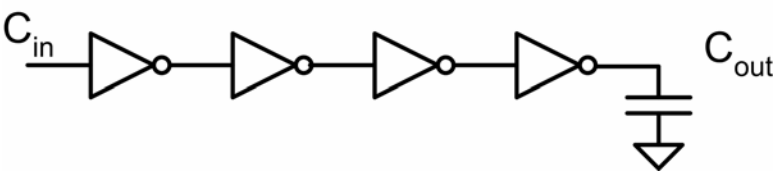
(b) Skewed NAND
Input a, b: $g_{up} = (2*3)/(1*3) = 2$ $g_{down} = (1*3)/(1*3) = 1$ $g_{avg} = 3/2$

Problem 3:

Find the p/n ratio which gives the best delay for the following path.

Note: Use g_{avg} and p_{avg} for your calculation

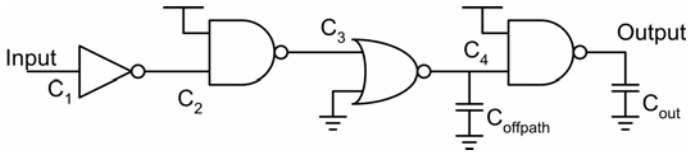
$C_{out} = 128C_{inv}$, $C_{in} = C_{inv}$.



Denote the P/N ratio of the inverter is γ. Then, the average logical effort is:
$g_{up} = (2/\gamma)(\gamma+1)/3 = (2/3)(\gamma+1)/\gamma$ $g_{down} = (\gamma+1)/3$ $\Rightarrow$ $g_{avg} = (\gamma+1)(\gamma+2)/(3\gamma)$
From given condition that $p_{inv} = 1$, we'll get $C_{p,inv} = C_{inv}$. So, the average parasitic delay is:
$p_{up} = (2/\gamma)(\gamma+1)/3 = (2/3)(\gamma+1)/\gamma$ $p_{down} = (\gamma+1)/3$ $\Rightarrow$ $p_{avg} = (\gamma+1)(\gamma+2)/(3\gamma) = g_{avg}$

Since the path has an even number of inverters, the total delay will be minimal if and only if all inverters have the same P/N ratio. The result optimal stage effort is:
$f_{opt} = (g_{avg}^4 . C_{out}/C_{in})^{1/4} = g_{avg} (256C_{in}/C_{in})^{1/4} = 4\ g_{avg}$.
The total delay,
$T_d = 4\ (f_{opt} + p_{avg}) = 20\ g_{avg} = (20/3)(\gamma+1)(\gamma+2)/\gamma$
With the form of the delay function, it reaches minimal if and only if $dT_d / dp = 0$. After simple algebraic transformation, we'll get:
$\gamma = 2^{1/2} \approx 1.41$

Problem 4:



Given the following path, with C_{out} = 64, C_{in} = C_1 = 1. Size the circuit using LE and determine the total delay for (See Horowitz's slides):

a. $C_{offpath}$ = 0

Due to no off-path loading, the optimal stage effort f and sizing can be done directly.

$f_o = (GBH)^{1/4} = [(1)(4/3)(53)(4/3).(1).(64/1)]^{1/4} \approx 3.71$

The gate sizes:

$C_4 = g_4 (C_{out} / f_o) = (4/3)\ (64/3.71) \approx 23.0$

$C_3 = g_3 (C_4 / f_o) = (5/3)\ (23.0/3.71) \approx 10.3$

$C_2 = g_2 (C_3 / f_o) = (4/3)\ (10.3/3.71) \approx 3.71$

$C_1 = g_1 (C_2 / f_o) = (1)\ (3.71/3.71) = 1.0$: *matching to given input size!*

Total delay:

$T_d = 4f_o + \Sigma p = 4\ (3.71) + 7 \approx 21.8$

b. $C_{offpath}$ = 5

Branching cannot be computed directly, so recursive solving is needed. However, as $C_{offpath} << C_4$. So, C_4 is not expected to change much. Then, branching at C_4 can be estimated.

$b_4 = (C_4 + C_{offpath})/C_4 \approx (23.0 + 5)/23.0 \approx 1.22$

The approximated optimal stage effort:

$f_o = (GBH)^{1/4} = [(1)(4/3)(5/3)(4/3).(1.22).(64/1)]^{1/4} \approx 3.90$

The gate sizes:

$C_4 = g_4 (C_{out} / f_o) = (4/3)\ (64/3.90) \approx 21.9$

$C_3 = g_3 (C_4 / f_o) = (5/3)\ (21.9+5.0)/3.90 \approx 11.5$

$C_2 = g_2 (C_3 / f_o) = (4/3)\ (11.5/3.90) \approx 3.93$

$C_1 = g_1 (C_2 / f_o) = (1)\ (3.93/3.90) = 1.01$: *matching quite close to given input size!*

Since calcuated C_1 matches well to the given value, the total delay can be computed from:

$T_d = 4f_o + \Sigma p = 4\ (3.90) + 7 \approx 22.6$

c. $C_{offpath}$ = 30

$C_{offpath} \sim C_4$ of problem 1. So, estimated branching using the value C_4 of problem 1 will not be accurate. Recursive computation of C_4 must be used. For the sake of comparison, let's do both.

* Estimated branching:

$b_4 = (C_4 + C_{offpath})/C_4 \approx (23.0 + 30)/23.0 \approx 2.30$

The approximated optimal stage effort:

$f_o = (GBH)^{1/4} = [(1)(4/3)(5/3)(4/3).(2.30).(64/1)]^{1/4} \approx 4.57$

The gate sizes:

$C_4 = g_4 (C_{out} / f_o) = (4/3) (64/4.57) \approx 18.7$

$C_3 = g_3 (C_4 / f_o) = (5/3) (18.7+30.0)/4.57 \approx 17.7$

$C_2 = g_2 (C_3 / f_o) = (4/3) (17.7/4.57) \approx 5.12$

$C_1 = g_1 (C_2 / f_o) = (1) (5.12/4.57) \approx 1.13$: *off by 13% compared to given input size.*

The total delay

$T_d = (C_2/C_{in}) + 3f_o + \Sigma p = (5.12/1) + 3 (4.57) + 7 \approx 25.8$

* Recursive computation:

$f_o \approx 4.74$

The gate sizes:

$C_4 = g_4 (C_{out} / f_o) = (4/3) (64/4.74) \approx 18.0$

$C_3 = g_3 (C_4 / f_o) = (5/3) (18.0+30.0)/4.74 \approx 16.9$

$C_2 = g_2 (C_3 / f_o) = (4/3) (16.9/4.74) \approx 4.74$

$C_1 = g_1 (C_2 / f_o) = (1) (4.74/4.74) \approx 1.00$: *matching to given input size.*

The total delay

$T_d = 4f_o + \Sigma p = 4 (4.74) + 7 \approx 26.0$: *even with $C_{offpath}$ comparable to C_4, the delay error due to simple branching estimation results within 1% of the accurate result.*

d. $C_{offpath} = 120$

* Estimated branching:

$C_{offpath} >> C_4$. So, the offpath load dominates the size of gate C_3. So, the optimal stage effort is best estimated from the first 3 gates. (*Note that using all 4-gate path in the estimation would cause more error because $C_{offpath} / C_4$ would vary more when C_4 is changed*)

$f_o \approx (GBH)^{1/3} = [(1)(4/3)(5/3).(1).(120+23)/1]^{1/3} \approx 6.44$

The gate sizes:

$C_4 = g_4 (C_{out} / f_o) = (4/3) (64/6.44) \approx 13.3$

$C_3 = g_3 (C_4 / f_o) = (5/3) (13.3+120.0)/6.44 \approx 34.5$

$C_2 = g_2 (C_3 / f_o) = (4/3) (34.5/6.44) \approx 7.15$

$C_1 = g_1 (C_2 / f_o) = (1) (7.15/6.44) \approx 1.11$: *off by 11% compared to given input size.*

The total delay:

$T_d = (C_2/C_{in}) + 3f_o + \Sigma p = (7.15/1) + 3 (6.44) + 7 \approx 33.5$

* Recursive computation:

$f_o \approx 6.66$

The gate sizes:

$C_4 = g_4 (C_{out} / f_o) = (4/3) (64/6.66) \approx 12.8$

$C_3 = g_3 (C_4 / f_o) = (5/3) (12.8+120.0)/6.66 \approx 33.2$

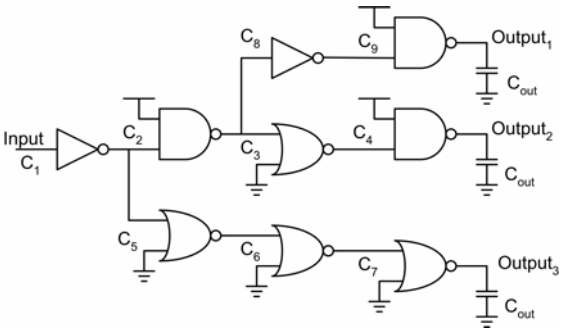
$C_2 = g_2 (C_3 / f_o) = (4/3) (33.2/6.66) \approx 6.66$

$C_1 = g_1 (C_2 / f_o) = (1) (6.66/6.66) \approx 1.00$: *matching to given input size.*

The total delay

$T_d = 4f_o + \Sigma p = 4 (6.66) + 7 \approx 33.6$: *using the above estimation, the delay error due to simple branching estimation results within 1% of the accurate result.*

Problem 5:



Assume $C_{out} = 64C$ and $C_{in} = C = C_1$.

a. Size the following circuit using simple branching. Report the total delay.

Using the inv (C_1) – NAND (C_2) – NOR (C_3) – NAND (C_4) path and simple branching (= counts of gate input), the optimal stage effort can be estimated.

$f_o = (GBH)^{1/4} = ((4/3)(5/3)(4/3).(2)(2).(64/1))^{1/4} \approx 5.25$

The gate sizes:

$C_9 = g(C_o/C_i) = (4/3)(64/5.25) \approx 16.3$

Similarly,

$C_8 \approx 3.1$; $C_4 \approx 16.3$; $C_3 \approx 5.16$

$C_2 \approx (4/3)(3.1 + 5.16)/5.25 \approx 2.10$

$C_7 \approx 20.3$; $C_6 \approx 6.45$; $C_5 \approx 2.05$

Check:

$f_{inv\ C1} = (1)(2.10 + 2.05) / 1 \approx 4.15$: it's 26% from the estimated f_o!

The total delay from input to:

* C_{out2} or C_{out3}:

$T_d = \Sigma(f + p) \approx (4.15 + 3(5.25)) + (1 + 2 + 2 + 2) \approx 26.9$

* C_{out1}

$T_d = \Sigma(f + p) \approx (4.15 + 3(5.25)) + (1 + 2 + 1 + 2) \approx 25.9$

b. Size the circuit using exact branching and report the total delay.

Ignore effects of parasitic delay difference between paths and use the same path as in part a (having worst parasitic delay).

Branching at C_3:

$b_{C3} = (g_{nor}\, g_{nand}\, C_{out2} + g_{inv}\, g_{nand}\, C_{out1}) / (g_{nor}\, g_{nand}\, C_{out2})$

$= [(5/3)(4/3)C_{out} + (1)(4/3)C_{out}] / [(5/3)(4/3)C_{out}] = 8/5$

Branching at C_2:

$b_{C3} = (g_{nand}\, b_{C3}\, g_{nor}\, g_{nand}\, C_{out2} + g_{nor}\, g_{nor}\, g_{nor}\, C_{out3}) / (g_{nand}\, b_{C3}\, g_{nor}\, g_{nand}\, C_{out2})$

$= [(4/3)(8/5)(5/3)(4/3)C_{out} + (5/3)(5/3)(5/3)C_{out}] / [(4/3)(8/5)(5/3)(4/3)C_{out}] \approx 1.98$

The optimal stage effort:

$f_o = (GBH)^{1/4} = ((1)(4/3)(5/3)(4/3).(8/5)(1.98).(64/1))^{1/4} \approx 4.95$ *(simple branching is off by 6%)*

The gate sizes:

$C_9 = g(C_o/C_i) = (4/3)(64/4.95) \approx 17.24$

Similarly,

$C_8 \approx 3.48$; $C_4 \approx 17.24$; $C_3 \approx 5.81$

$C_2 \approx (4/3)(3.48 + 5.81)/4.95 \approx 2.50$

$C_7 \approx 21.6$; $C_6 \approx 7.26$; $C_5 \approx 2.44$

Check:

$C_1 = g(C_o/C_i) = (1)(2.50 + 2.44)/4.95 \approx 1.00$ (*the same as given input*).

The total delay from input to:

* C_{out2} or C_{out3}:

$T_d = \Sigma(f + p) \approx 4\ (4.95) + (1 + 2 + 2 + 2) = 26.8$

* C_{out1}

$T_d = \Sigma(f + p) \approx 4\ (4.95) + (1 + 2 + 1 + 2) = 25.8$

Despite simple branching assumption, the delay in part (a) is within 1% of the optimal delay. The main reason is the error in total branching is offset by the 4^{th}-root of f_o computation.

c. Identify the critical path on the schematic. Explain your selection.

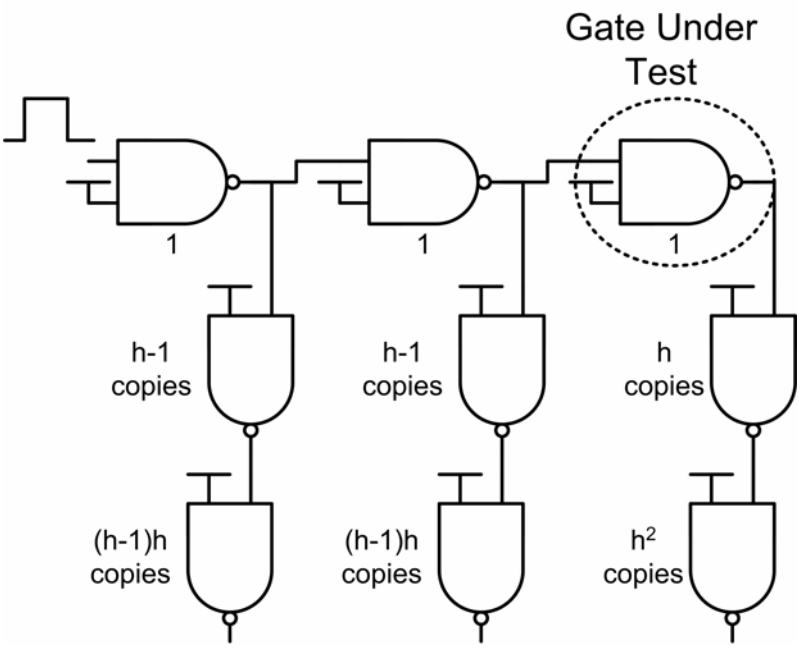
The above results show that due to equal-f sizing in all paths, the critical paths will be from the input to either C_{out2} or C_{out3}, where each have the worst-case parasitic delay of 7. In reality, the path to C_{out3} is likely more critical as NOR gates have more parasitic delay than NAND gates.

d. Comment on what would happen if the load at $Output_1$, $Output_2$ and $Output_3$ differ. Would the critical path change?

Changes at individual output load will directly affect the branching factors and therefore the optimal stage effort of all paths. However, since the paths are all sized with equal f_o, their delay only differ on the total parasitic delay. So, the critical paths remain to go to C_{out2} and C_{out3}.

Problem 6:

Use the following characterization setup (shown for a nand2).

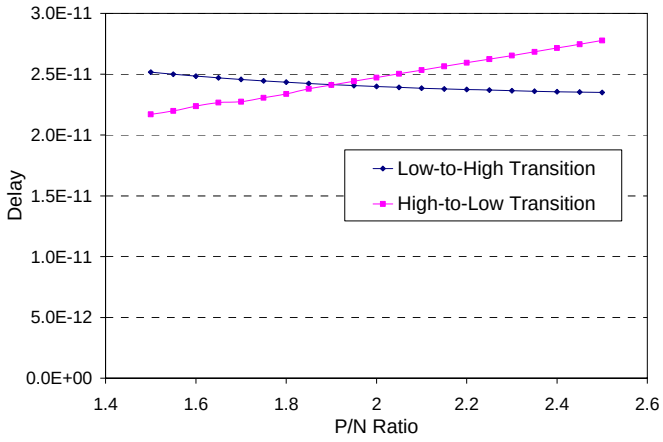


Note: For inverter characterization, replace each gate in the setup with inverters, for nor2 replace each gate in the setup with NOR2.

(a) Find the p/n ratio for an inverter where $g_{up} = g_{down}$

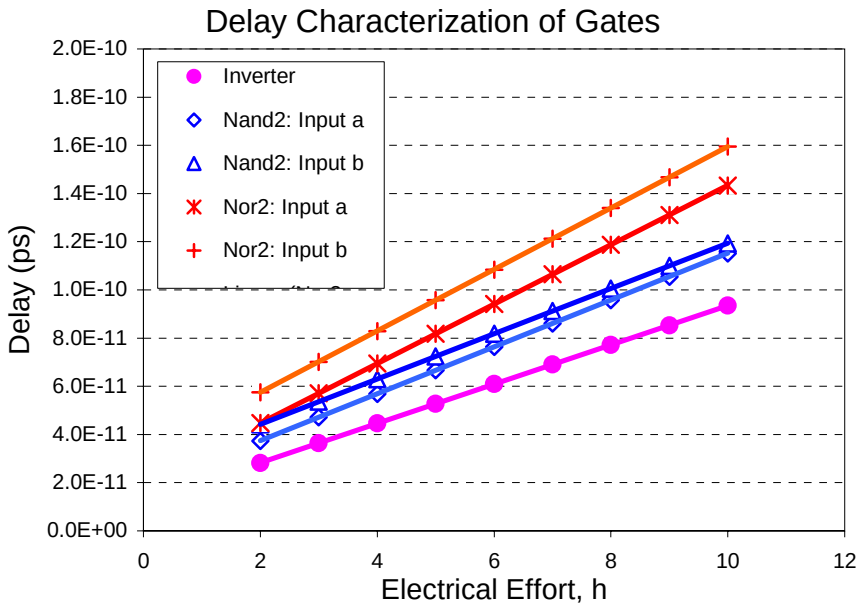
Observation:
The above requirement implies that the rise and fall times are equal at both input and output of the inverter at the optimal p/n ratio. They can be equivalently translated into equal delay for both output transitions. In simulation, either can be used. I choose to use the latter.

I use the above test setup and electrical effort of 2 (arbitrary choice). The p/n ratio is swept from 1.5 to 2.5 in 0.05 step. The result is graphically shown. Clearly, the optimal ratio is ~1.90.



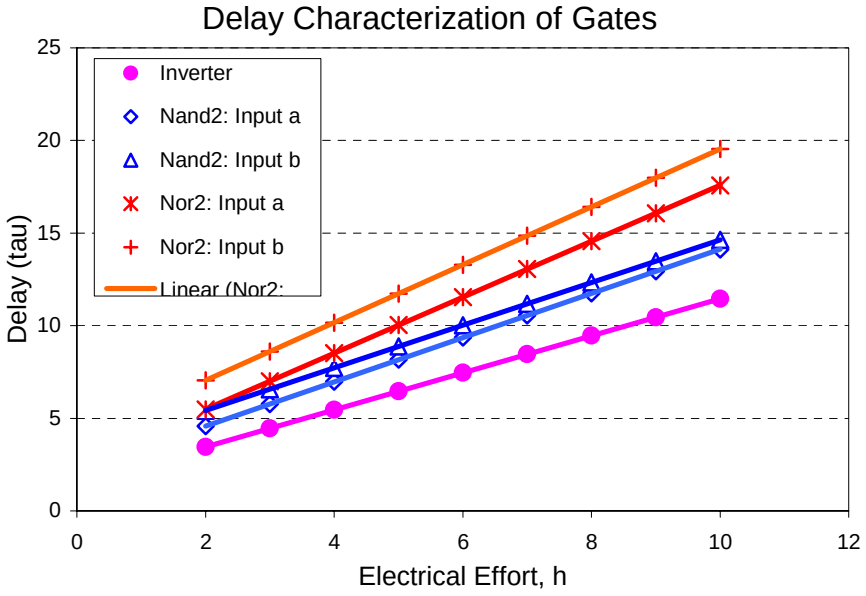
(b) Characterize an INV, NAND2, and NOR2 using HSPICE. Plot the delay vs. h relationship for each gate and input.

Using the above optimal p/n ratio, the characterization of INV, NAND2 and NOR2 is obtained. All delays show linear relationship to electrical effort h.



(c) Normalize the delay to τ-inv and plot the delay vs. h relationship

The normalized delay to τ (= 8.16ps) is given below.



(d) Report the *g* and *p* of each gate for each input normalized to the inverter pull down g. Do the values for g and p differ for each input? If yes, explain.

The table of *g* and *p* values of each gate and for each input:

	g	p
inv	1	1.46
nand2(a)	1.19	2.20
nand2(b)	1.15	3.12
nor2(a)	1.51	2.47
nor2(b)	1.56	3.92

The *g* and *p* values vary for different input of a gate. There are a couple of main reasons, I think. First, driving strength of each input (which depends on the location of the transistor location in the pulling path) differs. Results of *g* values suggest that this difference is small. Second, each input see different parasitic capacitance (which it has to charge/discharge). The *p* values show large difference. So, the difference in parasitic capacitance is quite significant. It emphasizes that the LE estimation by only counting the diffusion capacitance at the output node is not very accurate.

(e) Do the values of g_{up} and g_{down} for *Input a* on the NAND2 differ? *Input b*? If yes, explain.

The table of *g* and *p* values in each output transition for each input of NAND2:

NAND2	g	p
Input a: up	1.26	2.44
Input a: down	1.13	1.96
Input b: up	1.38	3.51
Input b: down	0.92	2.72

Regardless input chosen, the g_{up} and g_{down} values are different. One reason is that the input slope does not match in both transitions. In addition, the driving strength may not match any more. These above reasons are due to the difference between the test circuit setup and assumption in theory. It is explained in more detail in the next answer.

(f) Do the values obtained for *g* and *p* differ from the hand estimates? If yes, explain.

It is clearly that the simulated values and hand estimates do not match well. The main reason is due to the change in effective driving of gates. The hand estimates assume the effective driving where all transistors along a path switched. In the test setup for simulation, only ONE input is changed (the rest are at fixed voltage). The resulting driving strength is clearly different than the effective one. Hence, the data show quite significant a difference.
To really set the circuit for effective driving, more detail setup is needed. You are recommended to figure out how to do that and verify your results with the hand estimates.