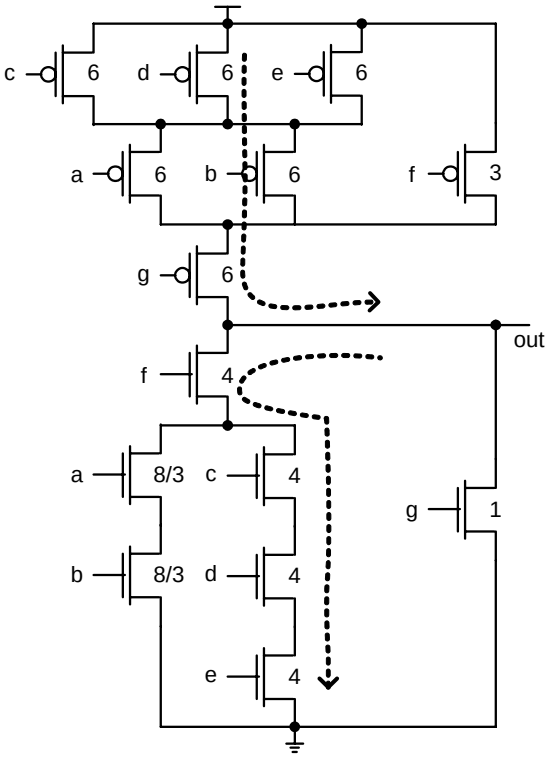
Solution to Take-Home Exam I

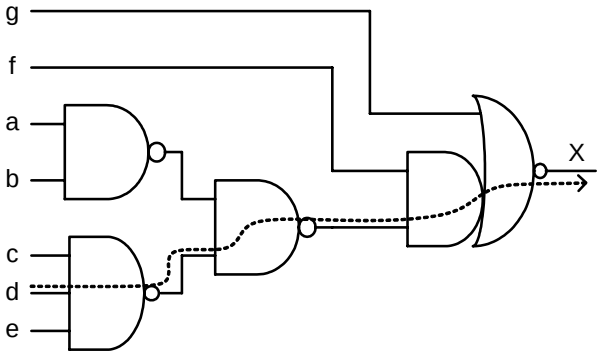
1) The implementation of the function **X** using complementary CMOS:
The loading is assumed 5fF. This load is equivalent to about 4.2x minimal-size inverter in Berkeley's 65nm CMOS technology.

The delay of the function depends not only on gate implementation, but also on the circuit gain (C_{out} / C_{in}). Since the load is quite small, the single CMOS implementation of the function X is expected the fastest.

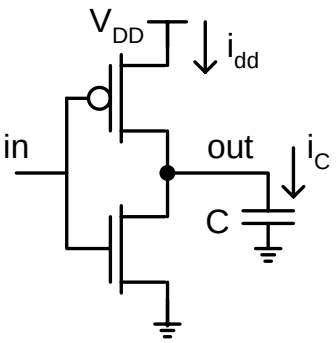
Because all transistors are sized for equal effective driving, the delays from each input are relatively the same. However, due to extra parasitic capacitance at different nodes, the critical paths are those with most parasitic capacitance and are shown in the circuit schematic.



An alternate CMOS implementation is given below. The critical path is through 3 gates: NAND3, NAND2, and AOI. This implementation is expected not as fast as the first because of more total parasitic delay and likely more total stage effort.



2) The power consumption is defined by:



$P = k\frac{1}{T}\int_0^T V_{DD}\, i_{dd}\, dt$, where

$$i_{dd} = \begin{cases} C\dfrac{dV_{out}}{dt} & t \in [\,0, 0.5T\,] \\ 0 & t \in [\,0.5T, T\,] \end{cases}$$

Note that the short-circuit current from V_{DD} to ground is ignored (students are suggested to quantify the power due to this current with simulation). So, the only power is consumed when charging the output capacitance.

Evaluate the power expression, we'll get:

$$P = k\frac{1}{T}\int_0^{0.5T} V_{DD} C\frac{dV_{out}}{dt}dt = k\frac{1}{T}\int_0^{V_{DD}} CV_{DD}dV_{out} = k\frac{1}{T}CV_{DD}^2 = kCV_{DD}^2 f$$

Part of the above power is used to store charge on the output capacitance; the rest is dissipated on the PMOS.

The energy stored in the capacitance is:

$$E_C = \int_0^{0.5T} V_{out} i_C dt = \int_0^{0.5T} V_{out} C\frac{dV_{out}}{dt}dt = \int_0^{V_{DD}} CV_{out}dV_{out} = \frac{1}{2}CV_{DD}^2$$

The power dissipated on the PMOS is:

$$E_{PMOS} = E_{Total} - E_C = CV_{DD}^2 - \frac{1}{2}CV_{DD}^2 = \frac{1}{2}CV_{DD}^2 \equiv E_C$$

In addition, due to the generality of the above integration, the total power consumption is the same even though the duty cycle of clock is changed.

3) Simulations of the possible implementations are performed using H-Spice and Berekeley 65nm transistor models.

Hspice netlists:

>> macros.lib

```
* Parameters
* ----------
.param Wmin='4*lambda'

* Three terminal FET macros
* -------------------------
.macro nmos s g d Le='2*lambda' Wi=Wmin
MN0 s g d gnd NMOS L=Le W=Wi AS='5*lambda*Wi' PS='2*5*lambda+Wi'
+ AD='5*lambda*Wi' PD='2*5*lambda+Wi'
.eom
.macro pmos s g d Le='2*lambda' Wi=Wmin
MP0 s g d vdd PMOS L=Le W=Wi AS='5*lambda*Wi' PS='2*5*lambda+Wi'
+ AD='5*lambda*Wi' PD='2*5*lambda+Wi'
.eom

* Inverter
* ---------
.macro inv in out
Xp0 vdd in out pmos Wi='2*Wmin'
Xn0 gnd in out nmos Wi='Wmin'
.eom
```

>> Implementation 1:

```
** Take-Home Exam #1
** CMOS implementation of the equation x
**--------------------------------------------------------------------
.include '65nm_nominal.lib'
.include 'macros.lib'

.param vdd=1V gnd=0V

*Defined lambda as half minimum channel length
.param lambda=32.5nm

.options accurate post
.temp 27

.tran 2ps 2.0ns

.op
.global vdd gnd
.probe

* Power Supplies
Vvdd vdd gnd vdd
```

```
*-----------------
* Input Stimulus
*-----------------
Vine ein gnd pulse (0V, vdd, 990ps, 10ps, 10ps, 990ps, 2.0ns)
Vina ain gnd 0
Vinb bin gnd vdd
Vinc cin gnd 0
Vind din gnd 0
Vinf fin gnd 0
Ving gin gnd vdd

* ---------------------
* Logic Implementation
* ---------------------
.subckt xgate a b c d e f g x
Xna nb_d a na_d  nmos Wi='4*Wmin'
Xnb gnd  b nb_d  nmos Wi='4*Wmin'
Xnc nd_d c na_d  nmos Wi='6*Wmin'
Xnd ne_d d nd_d  nmos Wi='6*Wmin'
Xne gnd  e ne_d  nmos Wi='6*Wmin'
Xnf na_d f x     nmos Wi='2*Wmin'
Xng gnd  g x     nmos Wi='Wmin'

Xpc vdd  c pa_d  pmos Wi='8*Wmin'
Xpd vdd  d pa_d  pmos Wi='8*Wmin'
Xpe vdd  e pa_d  pmos Wi='8*Wmin'
Xpa pa_d a pc_d  pmos Wi='8*Wmin'
Xpb pa_d b pc_d  pmos Wi='8*Wmin'
Xpf vdd  f pc_d  pmos Wi='4*Wmin'
Xpg pc_d g x     pmos Wi='4*Wmin'
.ends

xinva ain ai inv
xinvb bin bi inv
xinvc cin ci inv
xinvd din di inv
xinve ein ei inv
xinvf fin fi inv
xinvg gin gi inv

Xdut  ai bi ci di ei fi gi x xgate
cout  x  gnd  5f

*-------------------
*Delay measurements
*-------------------
.measure tran tdr_e trig v(e) val='0.5*vdd' fall=1
+                  targ v(x) val='0.5*vdd' rise=1
.measure tran tdf_e trig v(e) val='0.5*vdd' rise=1
+                  targ v(x) val='0.5*vdd' fall=1

.end
```

The worst case delay is:

```
Td = max(tdr_e,tdf_e) = max(1.613e-10, 1.170e-10) = 1.613e-10 (s)
```

>> Implementation 2: The HSPICE logic netlist is given below.

```
* ---------------------
* Logic Implementation
* ---------------------
.subckt xgate a b c d e f g x
Xna nb_d a  y1   nmos Wi='2*Wmin'
Xnb gnd  b  nb_d nmos Wi='2*Wmin'
Xpa vdd  a  y1   pmos Wi='2*Wmin'
Xpb vdd  b  y1   pmos Wi='2*Wmin'

Xnc nd_d c  y2   nmos Wi='3*Wmin'
Xnd ne_d d  nd_d nmos Wi='3*Wmin'
Xne gnd  e  ne_d nmos Wi='3*Wmin'
Xpc vdd  c  y2   pmos Wi='2*Wmin'
Xpd vdd  d  y2   pmos Wi='2*Wmin'
Xpe vdd  e  y2   pmos Wi='2*Wmin'

Xn1 n2_d y1 y    nmos Wi='2*Wmin'
Xn2 gnd  y2 n2_d nmos Wi='2*Wmin'
Xp1 vdd  y1 y    pmos Wi='2*Wmin'
Xp2 vdd  y2 y    pmos Wi='2*Wmin'

Xny nf_d y  x    nmos Wi='2*Wmin'
Xnf gnd  f  nf_d nmos Wi='2*Wmin'
Xng gnd  g  x    nmos Wi='2*Wmin'
Xpy pg_d y  x    pmos Wi='4*Wmin'
Xpg vdd  g  pg_d pmos Wi='4*Wmin'
Xpf pg_d f  x    pmos Wi='4*Wmin'
.ends

*-----------------
* Input Stimulus
*-----------------
Vine ein gnd pulse (0V, vdd, 990ps, 10ps, 10ps, 990ps, 2.0ns)
Vinc cin gnd 0
Vind din gnd 0
Vina ain gnd vdd
Vinb bin gnd 0
Vinf fin gnd 0
Ving gin gnd vdd
```

Critical-path delay:

```
Td = max(tdr_e,tdf_e) = max(2.482e-10, 2.159e-10) = 2.482e-10 (s)
```

Thus, the simulation reinforces that the single CMOS-gate implementation is the fastest.