Homework 4 Solutions

Problem 1: *pulsed latches* (Taken from UC Berkeley)

Two pulsed latches are shown in Figure 1.

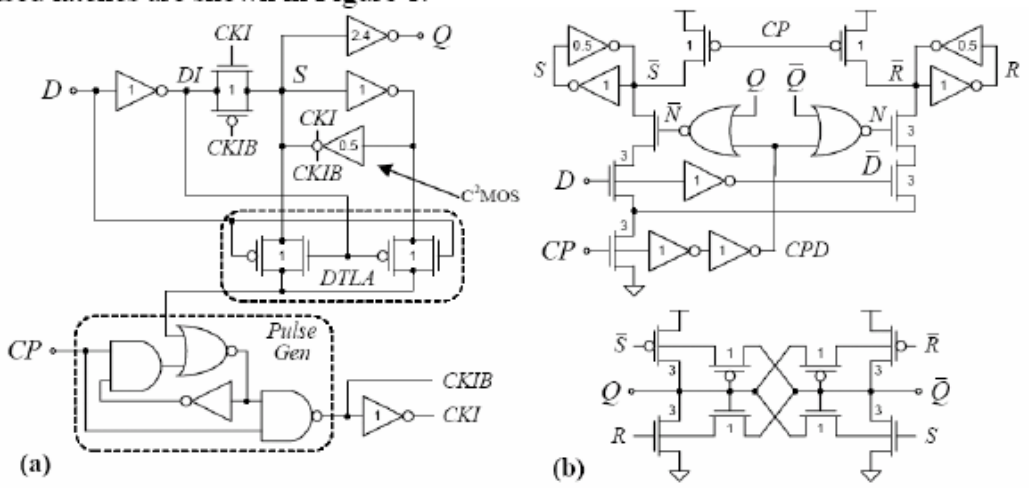


Figure 1 Pulsed latches

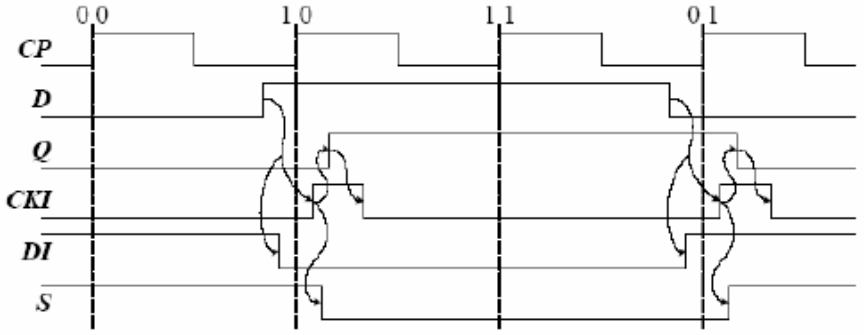
a) Briefly explain how the circuit from Figure 1a works. What is the function of blocks labeled as *Pulse Gen* and *DTLA*?

PG generates pulse {CKI, CKIB}, which triggers the latch only when D ≠ Q.

DTLA checks if D ≠ Q and enables generation of the pulse {CKI,CKIB} only when output Q needs change i.e. when D ≠ Q.

Circuit outside the dashed lines is a simple pulsed-latch

b) Draw a timing diagram of signals *CKI*, *DI* and *S* over 4 clock cycles for all combinations of *D* and *Q*.



c) If the *DTLA* circuit was taken out from the schematic, and its output replaced with a constant logic level, the circuit would still operate as a pulsed latch. Compare the setup and hold times of this new flip-flop to the original one from Figure 1a.

t_{setup} is determined by the rising edge of CP and $t_{setup} \downarrow$ by the amount of time it takes DTLA to compute clock enable signal.

t_{hold} is determined by the falling edge of CKI and $t_{hold} \uparrow$ because signal CKI would last longer instead of being shortened by DTLA circuit due to a transition at the output.

d) This latch can sometimes be used in your design to lower the energy dissipation. How would you calculate the switching probability of the input D when this flip-flop saves energy as compared to a conventional flip-flop? Label appropriate variables that you use in your calculations.

Conventional latch:

$$E^c = E^c_{Clk} + \alpha E^c_{Data}$$

Data-transition look-ahead latch:

$$E = \alpha\left(E_{Clk} + E_{Data} + E_{DTLA} + E_{PG}\right)$$

Energy is saved when $E < E^c$. Then,

$$\alpha \le \frac{1}{\frac{E_{Clk}}{E^c_{Clk}} + \frac{E_{DTLA} + E_{PG}}{E^c_{Clk}}} \rightarrow \frac{1}{1 + \frac{E_{DTLA} + E_{PG}}{E_{Clk}}} \quad (assume\, E^c_{Clk} = E_{Clk})$$

The smaller the overhead in DTLA and PG, the higher the activity for which energy can be saved. Ideally, when the overhead is zero, energy is equal at maximum data activity of 0.5.

e) Briefly explain how the pulsed latch from Figure 1b works.

This is also data-transition look-ahead latch.

When D ≠ Q, generation of set and reset signals $\overline{S}$ and $\overline{R}$ is enabled and the circuit operates as standard SR latch

Problem 2: *Timing* (Taken from UC Berkeley)

An example pipeline with a loop is shown in Figure 2. L1 latches are transparent when C1 is high; L2 latches are transparent when C2 is high.

The pipeline is clocked by an asymmetric two-phase clock as shown in Figure 3. The clock edges are ideal and there is no skew or jitter.

Assume that the latches have propagation delays, setup and hold times equal to $t_{C\text{-}Q} = t_{D\text{-}Q} = t_{su} = t_h =$ 100ps.

Each of the pipeline stages, S1, S2, S3, S4, S5, and S6 is designed using static logic.

Worst-case propagation delay of logic block S3 is dependent on both of its inputs shown in figure. Propagation delays of each of the combinational logic stages are t_{s1} = 1ns, t_{s2} = 1ns, t_{s3} = 1.5ns, t_{s4} = 1.5ns, t_{s5} = 2ns, t_{s6} =1.2ns.

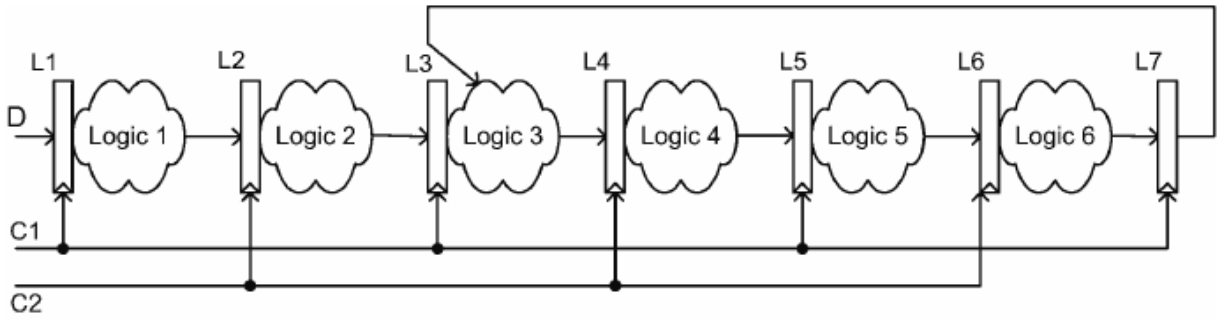


Figure 2 Pipeline system

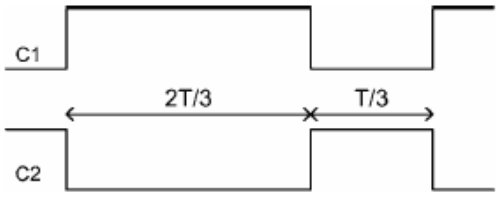


Figure 3 2-phase clock timing

(a) If the input datum D is available 200ps before the falling edge of the clock C1, what is the minimum cycle time of this system? Please show all delay constraints for this system.

Since there is only T/3 time for logic in front of even latches and S_5 has the longest delay, critical timing constraints are related to the closing edge of C_2.

D-S_1-L_2:

$$t_{S1} - (200ps - t_{setup,L1}) + t_{setup,L2} \leq T/3 \quad \Rightarrow T \geq 3ns$$

max{S_6-L_7,S_2-L_3}-**S_3-L_4**:

$$t_{S3} - ((2T/3 - t_{S6}) - t_{setup,L7}) + t_{setup,L4} \leq T/3 \quad \Rightarrow T \geq 2.9ns$$

S_4-L_5-**S_5-L_6**:

$$t_{S5} - ((2T/3 - t_{S4}) - t_{setup,L5}) + t_{setup,L6} \leq T/3 \quad \Rightarrow T \geq 3.7ns$$

Solution: T ≥ 3.7ns

(b) How would a maximum skew of 100ps on both rising and falling edges of the clock affect your answer to question (a)?

In worst case, both edges of both clock signals are allowed to vary independently.

S_4-L_5-**S_5-L_6**:

$$t_{S5} - ((2T/3 - t_{S4} - \mathbf{2t_{skew}}) - t_{setup,L5}) + t_{setup,L6} \leq T/3 - \mathbf{2t_{skew}}$$

$$\mathbf{T \geq T_{min}^{(a)} + 4t_{skew} = 4.1ns}$$

(c) What is the minimum clock period if the input datum D arrives 200ps *after* the falling edge of the clock? Assume zero skew.

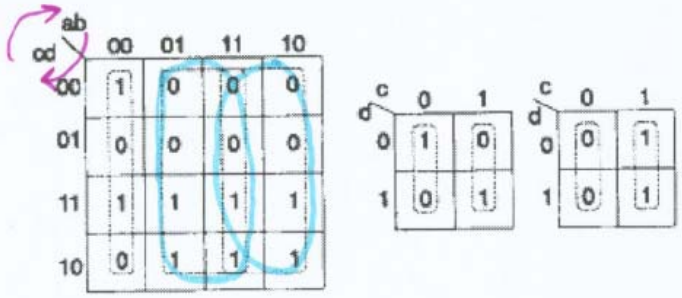
Minimum clock period is the same as in (a), but we will have one extra cycle of latency.

$T \geq 3.7ns$

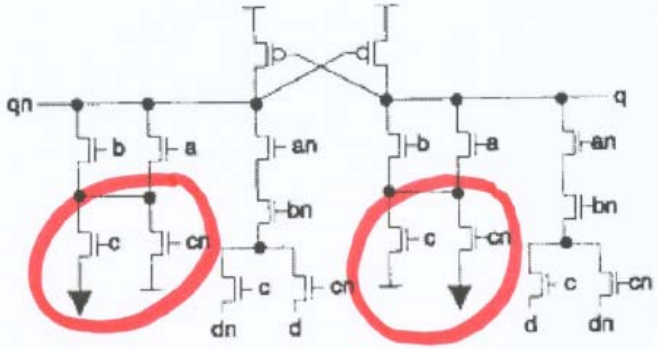
Problem 3.

Show that the following implementation of the function given by Karnaugh-maps is incorrect and give the correct solution.

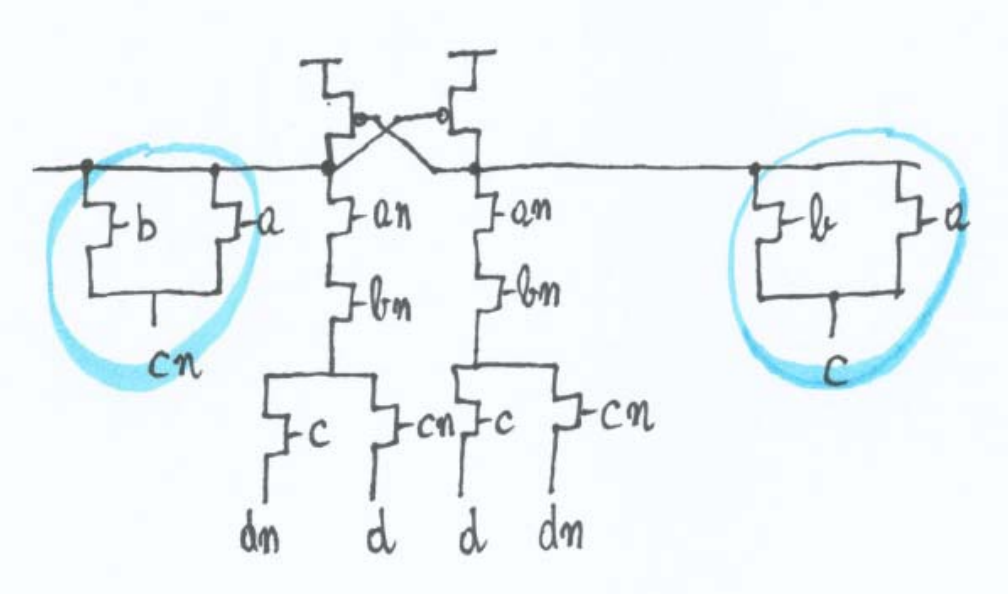
(from paper: F. S. Lai, W. Hwang, "Differential Cascode Voltage Switch with the Pass-Gate (DCVSPG) Logic Tree for High Performance CMOS Digital Systems", Proceedings of the 1993 International Symposium on VLSI Technology, Taipei, Taiwan, June 2-4, 1995)



(a)



Functionally, the circuit operates correctly. The only synthesis inconsistency is found in the branches which cover case where (a=1 or b=1). In Karnaugh-map, two groups for this case are formed, which means that part should be realized with pass transistors with a and b being control variable.
The correct solution is given below:



NOTE: Please note that in the paper, the function given as an example doesn't correspond to the Karnaugh-map shown here. The error is that (ab) and (cd) variables are switched, as marked with the arrows in the Karnaugh-map above.
The correct solution for the given Karnaugh-map as it is in this problem is shown here. The realization for the correct Karnaugh-map function realization is similar to the one shown, only variables are exchanged but the topology is the same.

Unger and Tan's paper

There exists a flaw in Unger and Tan's paper. Identify the flaw and provide the correct solution. Highlight the affected equations. (enclose those pages of the paper with highlights).

S. H. Unger and C. J. Tan, "Clocking Schemes for High-Speed Digital Systems", IEEE Transaction on Computers, Vol. C-35, No. 10, pp. 880-895, October 1986.

In their discussion of Optimum Parameters for 1-Phase Clocking with Latches, Unger and Tan uses the wrong formula for the earliest possible arrival of a D signal for the next cycle, i.e. t_{DEArrN}. Eq. (14) ought to use the min() function, instead of the max() function because it corresponds to the *earliest* time.

So, the correct equation should be:

$$t_{DEArrN} = \mathbf{min}\ [-T_L + D_{CQm} + D_{Lm},\ t_{DEArr} + D_{DQm} + D_{Lm}].$$