II. Relating Rabaey Book (RB) Model to Logical Effort

(the terms used here will be those from RB, with the corresponding LE notation mentioned where appropriate)

The RB Model is based on the same RC delay model as LE.

$$t_p = 0.69 R_{eq}\left(C_{\text{int}} + C_{ext}\right) \qquad (22)$$

Again to accommodate sizing a scaling factor is introduced, which RB refers to as S.

$$R_{eq} = \frac{R_{ref}}{S} \qquad (23)$$

$$C_{\text{int}} = SC_{iref} \qquad (24)$$

Substitution obtains

$$t_p = 0.69 \frac{R_{ref}}{S}\left(SC_{iref} + C_{ext}\right) \qquad (25)$$

The scaling factor still exists in an undesirable location, therefore the equation can be rearranged as follows

$$t_p = 0.69 R_{ref} C_{iref}\left(1 + \frac{C_{ext}}{SC_{iref}}\right) \qquad (26)$$

Substituting $C_{\text{int}} = SC_{\text{iref}}$ obtains

$$t_p = 0.69 R_{ref} C_{iref}\left(1 + \frac{C_{ext}}{C_{\text{int}}}\right) \qquad (27)$$

Since the RB model uses $C_{\text{int}}$ rather than $C_g$ , the relationship between $C_{\text{int}}$ and $C_g$ must be defined.

$$C_{\text{int}} = \gamma_{gate} C_g \qquad (28)$$

Define $t_{p0}$ as the parasitic delay of the gate

$$t_{p0} = 0.69 R_{ref} C_{iref} \qquad (29)$$

Yields the following form for the delay model

$$t_p = t_{p0}\left(1+\frac{C_{ext}}{\gamma_{gate}C_g}\right) \qquad (30)$$

Again this model is only applicable to a single gate type and thus a relationship must be established as in LE. Again the relationship will be shown versus and inverter.

$$t_p = t_{pgate}\left(1+\frac{C_{ext}}{\gamma_{gate}C_g}\right) \qquad (31)$$

$$t_p = \frac{t_{pinv}}{t_{pinv}}t_{pgate}\left(1+\frac{C_{ext}}{\gamma_{gate}C_g}\right) \qquad (32)$$

$$t_p = t_{pinv}\left(\frac{t_{pgate}}{t_{pinv}}+\frac{C_{ext}}{\gamma_{gate}C_g}\frac{t_{pgate}}{t_{pinv}}\right) \qquad (33)$$

$$t_p = t_{pinv}\left(\frac{t_{pgate}}{t_{pinv}}+\frac{C_{ext}}{\gamma_{gate}C_g}\frac{t_{pgate}}{t_{pinv}}\right) \qquad (34)$$

Note $t_{pgate} = 0.69R_{refgate}C_{irefgate}$ , where $R_{refgate}$ for all gates are equal (by assumption on pg. 253).

$$t_p = t_{pinv}\left(\frac{t_{pgate}}{t_{pinv}}+\frac{C_{ext}}{\gamma_{gate}C_g}\frac{0.69R_{refgate}C_{irefgate}}{0.69R_{refinv}C_{irefinv}}\right) \qquad (35)$$

$$t_p = t_{pinv}\left(\frac{C_{refgate}\gamma_{gate}}{C_{refinv}\gamma_{inv}}+\frac{C_{ext}}{\gamma_{gate}C_g}\frac{C_{refgate}\gamma_{gate}}{C_{refinv}\gamma_{inv}}\right) \qquad (36)$$

$$t_p = t_{pinv}\left(\frac{C_{refgate}\gamma_{gate}}{C_{refinv}\gamma_{inv}}+\frac{1}{\gamma_{inv}}\frac{C_{ext}}{C_g}\frac{C_{refgate}}{C_{refinv}}\right) \qquad (37)$$

Where the following relationships can be defined

$$p'_{gate} = \frac{C_{refgate}\gamma_{gate}}{C_{refinv}\gamma_{inv}} \qquad (38)$$

$$g_{gate} = \frac{C_{refgate}}{C_{refinv}} \qquad (39)$$

$$h = \frac{C_{ext}}{C_g} \qquad (40)$$

Thus the delay model is as follows

$$t_p = t_{pinv}\left( p' + \frac{1}{\gamma_{inv}} gh \right) \qquad (41)$$

Since $\gamma_{inv}$ is constant it can be factored out to produce the same delay model as logical effort.

$$t_p = \frac{t_{pinv}}{\gamma_{inv}}\left(\gamma_{inv} p' + gh\right) \qquad (42)$$

The relationship between RB model and LE can be seen as

$$p = p'\gamma_{inv} \qquad (43)$$

$$\tau = \frac{t_{pinv}}{\gamma_{inv}} = \frac{0.69 R_{ref} C_{iref}}{\gamma_{inv}} = \frac{0.69 R_{ref} \gamma_{inv} C_g}{\gamma_{inv}} = 0.69 R_{ref} C_g \qquad (44)$$

Since the models are of the same form the optimization results from LE hold for the RB model.

III. Errors in RB

The first error that exists in RB is on pg. 209. This error is what creates the confusion with their modeling. The first sentence of the 2nd paragraph should be eliminated. If anything it should apply to equation 5.37, not 5.35.

Also on pg. 209 confusion arises from their mentioning $\gamma = 0$, thus making 5.36 appear to equal infinity. However $t_{p0}$ also depends on $\gamma$, and thus through substitution it will lead back to td = 0.69 R ( $\gamma C_g + C_{ext}$) which is not equal to infinity when $\gamma = 0$.

Problem 5.5 on page 210-211. The hints for finding the gate size should be eliminated. The $2.52 = 16^{1/3}$ should be eliminated as it is really not applicable. If anything it should be shown as f = $f = (B \cdot H)^{1/3} = (16 \cdot 64)^{1/3}$, instead of introducing some sizing factor which just happens to equal 2.52, because there is a branch of 4 at each node and an f of 4 for the path without branching.

**15.** Sizing a chain of inverters.

**a.** In order to drive a large capacitance ($C_L$ = 20 pF) from a minimum size gate (with input capacitance $C_i$ = 10fF), you decide to introduce a two-staged buffer as shown in Figure 5.12. Assume that the propagation delay of a minimum size inverter is 70 ps. Also assume that the input capacitance of a gate is proportional to its size. Determine the sizing of the two additional buffer stages that will minimize the propagation delay.

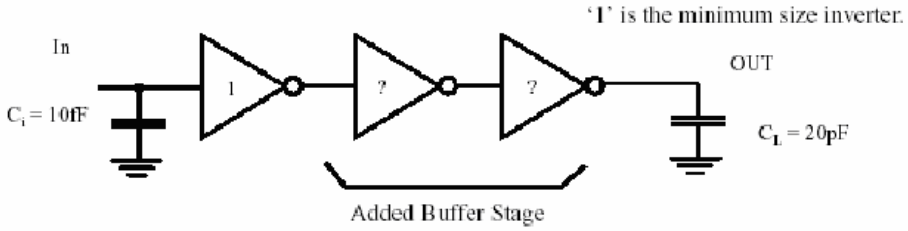


**Figure 5.12** Buffer insertion for driving large loads.

**Solution**

Minimum delay occurs when the delay through each buffer is the same. This can be achieved by sizing the buffer as f, $f^2$, respectively

where $f = \sqrt[N]{F} = \sqrt[3]{2000} = 12.6$, so ($\gamma$=0)

$$t_p = Nt_{p0}(1 + f/\gamma) = 3 \cdot 70ps \cdot (1 + 12.6) = 2.8ns$$

ERRORS:

The problem can not be solved without defining $\gamma$ in the problem.

For part a their solution is for $\gamma = 1$ , not $\gamma = 0$. Obviously if $\gamma = 0$ the delay would be

$$t_d = N0.69R\left(\gamma C_{g,i} + C_{ext,i}\right) = N0.69RC_{ext,i}$$

where $C_{ext,j}$ are sized according to $f = 2000^{1/3}$ or f = 12.6

Although this is really difficult to solve using this model since only $t_{p0}$ is given instead of what should be given $\tau$ from LE, for which this solution would be trivial.

**b.** If you could add any number of stages to achieve the minimum delay, how many stages would you insert? What is the propagation delay in this case?

**Solution**

From the text, we know that the minimum delay occurs when f = e. Therefore,

$$N = \frac{\ln(2000)}{\ln(f)} = 7.6$$

$$f = e^{\frac{\ln(2000)}{7}} = 2.96$$

$$t_{delay} = 7 \times 3.96 \times 70\text{ps} = 1.9ns$$

Errors:

Again this can only be solved if γ is known, which defines how N is computed. There solution for N comes from γ = 0, which can be seen by the assumption that optimal deal occurs at f = e.

The rounding down of 7.6 to 7 is also strange, as this should be rounded up to 8.

The solution for f is extremely odd as it should be shown using the equation

$f = 2000^{1/7}$ , not that they are different, but it is odd…

Finally the delay is again reported using γ = 1 for the final solution, which is different than the original assumption of γ = 0, which was used for finding the optimal number of stages.

**c.** Describe the advantages and disadvantages of the methods shown in (a) and (b).

**Solution**

Solution (b) is faster but it consumes much more area than (a).

Difficult to make any conclusion here since the result for part a is incorrect and unattainable given the problem statement and the result for part b is incorrect and unattainable as well.

**d.** Determine a closed form expression for the power consumption in the circuit. Consider only gate capacitances in your analysis. What is the power consumption for a supply voltage of 2.5V and an activity factor of 1?

**Solution**

The power consumption is determined as follows

$$P = C_{tot} V_{dd}^2 \frac{1}{T} \alpha$$

$$P = C_t V_{dd}^2 \frac{1}{T} \alpha \sum_{k=0}^{3} f^k = C_t V_{dd}^2 \frac{1}{T} \alpha \left( \frac{f^4 - 1}{f - 1} \right) = 136 \left( \frac{1}{T} \right) \text{ pWatts}$$

Since (a) and (b) are incorrect no actual result can be given.

$C_t$ is undefined so this is strange. The assumption is that $C_t$ is the template size, however this wouldn't work correctly, so it must be $C_i$ .

Probably should also be

$$P = C_t V_{dd}{}^2 \frac{1}{T} \alpha \left( \frac{f^4 - 1}{f - 1} \right)$$