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Chapter 1

Introduction

Designing high-speed digital circuits is an art. Even though a solid background in physics and electrical engineering is required in order to perform this task, it can not be accomplished without a great degree of creativity, inventiveness and free spirited will to always try something new, unconventional and untried. Therefore acquiring those skills requires a talent, gift, dedication and above all love for this work. Good designers take an exceptional pride in their work. They know each other, they meet, and they constantly compete to produce designs that are better than any one done previously. Demands placed on those designs are exceptionally high. It is not only exceptional performance and speed that is desired, but design has to fit in a smaller area, use much less power for the same performance level, be reliable and satisfy number of other difficult tasks imposed upon it. This is also a very dynamic discipline where things are constantly changing making what we know rapidly obsolete. The life of one technology generation is about three years and even getting shorter. Therefore one should be constantly learning because just a few years of inactivity will set the person behind. Just like the top athletes, good digital designers are constantly practicing and improving their skills. However, in spite of this unprecedented dynamic, the foundations of all the work are in the basic sciences: mathematics and physics, therefore a deep knowledge and understanding of both is a must.

Historical Perspective

Since the invention of the transistor microelectronics has experienced an unprecedented development not ever seen in the history of the mankind. The electronic era really took of with the invention of the transistor by Bardeen, Brattain and Shockley unveiled by Bell Laboratories on June 30, 1948. On December 16, 1947 Bardeen and Brattain built the point-contact transistor, made from strips of gold foil on a plastic triangle, pushed down into contact with a slab of germanium.

Fig. 1. The first contact transistor developed in Bell Laboratories by Bardeen and Brattain under the supervision of Shockley in 1948.

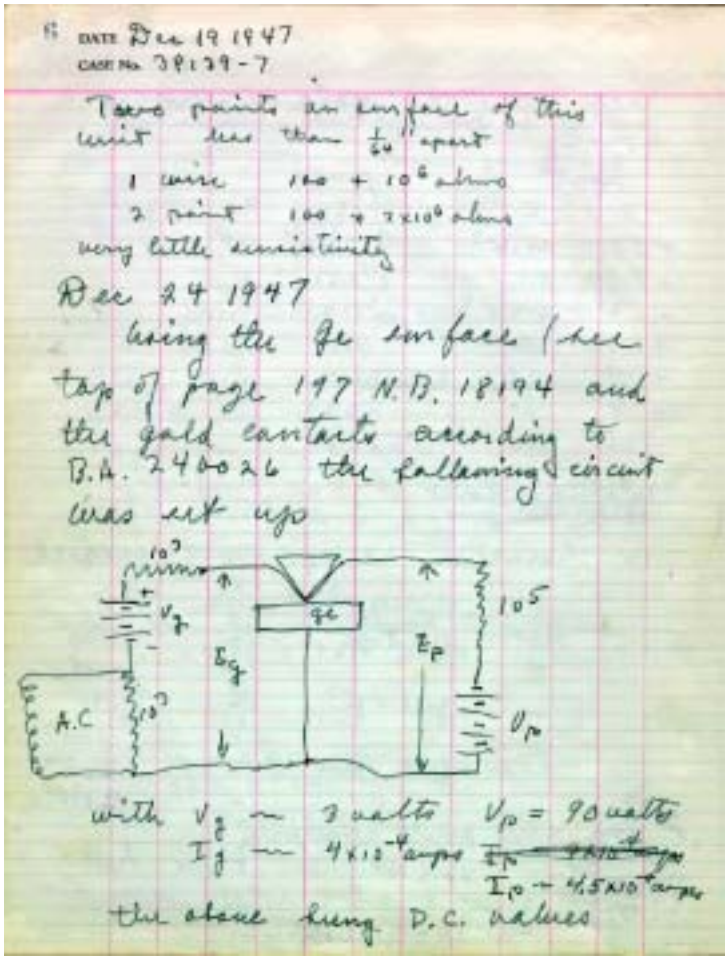
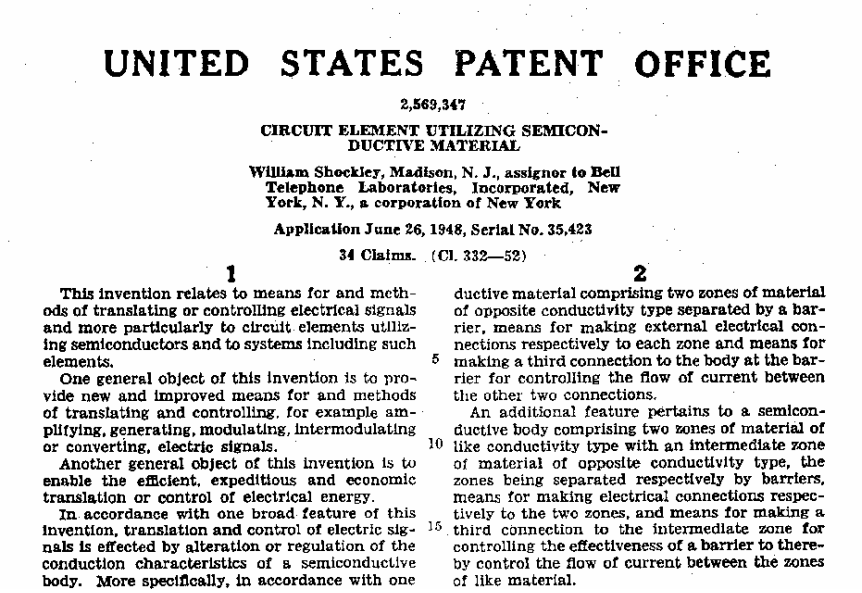


Fig. 2. December 24th, 1947 entry into Walter Brattain's laboratory notebook describing point-contact transistor operation.

Shockley followed that with the invention of junction (sandwich) transistor, which he developed in a burst of creativity and anger. It took him a total of four weeks to develop it, although it took another two years before he could actually build one. His device was more rugged and more practical than Bardeen and Brattain's point-contact transistor, and much easier to manufacture. This enabled the transistor to be practically built.



UNITED STATES PATENT OFFICE

2,569,347

CIRCUIT ELEMENT UTILIZING SEMICONDUCTIVE MATERIAL

William Shockley, Madison, N. J., assignor to Bell Telephone Laboratories, Incorporated, New York, N. Y., a corporation of New York

Application June 26, 1948, Serial No. 35,423

34 Claims. (Cl. 332—52)

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This invention relates to means for and methods of translating or controlling electrical signals and more particularly to circuit elements utilizing semiconductors and to systems including such elements.

One general object of this invention is to provide new and improved means for and methods of translating and controlling, for example amplifying, generating, modulating, intermodulating or converting, electric signals.

Another general object of this invention is to enable the efficient, expeditious and economic translation or control of electrical energy.

In accordance with one broad feature of this invention, translation and control of electric signals is effected by alteration or regulation of the conduction characteristics of a semiconductive body. More specifically, in accordance with one

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ductive material comprising two zones of material of opposite conductivity type separated by a barrier, means for making external electrical connections respectively to each zone and means for making a third connection to the body at the barrier for controlling the flow of current between the other two connections.

An additional feature pertains to a semiconductive body comprising two zones of material of like conductivity type with an intermediate zone of material of opposite conductivity type, the zones being separated respectively by barriers, means for making electrical connections respectively to the two zones, and means for making a third connection to the intermediate zone for controlling the effectiveness of a barrier to thereby control the flow of current between the zones of like material.

Fig. 3. Shockely's patent No. 2,569,347 describing junction transistor, applied for June 26, 1948

The invention of transistor received little attention at the time. However, Shockley saw its potential. He left Bell Labs to found Shockley Semiconductor in Palo Alto, California where he hired superb engineers and physicists. Fortunately or not, Shockley's personality drove out eight of his best and brightest. Those "traitorous eight" founded a new company called Fairchild Semiconductor. Bob Noyce and Gordon Moore, two of the eight, went on to form Intel Corporation. Nonetheless, Shockley's company was the beginning of Silicon Valley.

In the 1950s and 1960s, most U.S. companies chose to focus their attentions on the military market in producing transistor products. That left the door wide open for Japanese engineers like Masaru Ibuka and Akio Morita, who founded a new company named Sony Electronics that mass-produced tiny transistorized radios. A large part of their success layed in developing the ability to quickly mass-produce transistors.

(from PBS: www.pbs.org)

The invention of transistor was followed by the next important milestone, development of the integrated circuit by Kilby and Noyce in 1958. This invention essentially enabled the era of digital electronics.

Jack Kilby was hired by Texas instruments just before summer of 1958. Being left alone and having a lot of time to think it suddenly occurred to him that all parts of a circuit, not just the transistor, could be made out of silicon. At the time, nobody was making capacitors or resistors out of semiconductors. If it could be done then the entire circuit could be built out of a single crystal, thus making it smaller and much easier to produce. By September 12, Kilby had built a working model, and on February 6, Texas Instruments filed a patent. Their first "Solid Circuit" the size of a pencil point, was shown off for the first time in March.

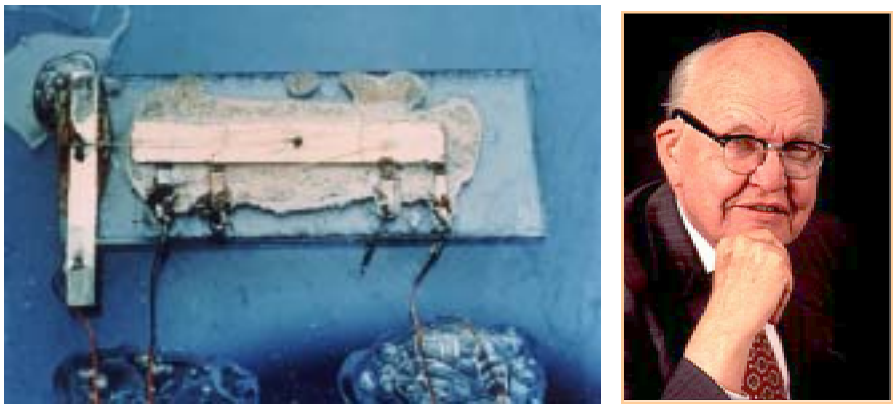


Fig. 4. The first integrated circuit built by its inventor Jack Kilby, September 12, 1958.

Fig. 5. Kilby's entry in his notebook dated September 12, 1958 describing integrated circuit. US Patent No. 3,138,743 was filed on February 6, 1959

In January of 1959, Robert Noyce, who was working at the Fairchild Semiconductor, realized independently of Jack Kilby that a whole circuit could be made on a single chip. While Jack Kilby's contribution was in hammering out the details of making individual components, Noyce thought of a much better way to connect the parts. That spring, Fairchild began a push to build what they called "unitary circuits" and they also applied for a patent on the idea. Knowing that TI had already filed a patent on something similar, Fairchild wrote out a highly detailed application, hoping that it wouldn't infringe on TI 's similar device. All that detail paid off. On April 25, 1961, the patent office awarded the first patent for an integrated circuit to Robert Noyce while Kilby's application was still being analyzed. Today, both men are acknowledged as having independently conceived of the idea.

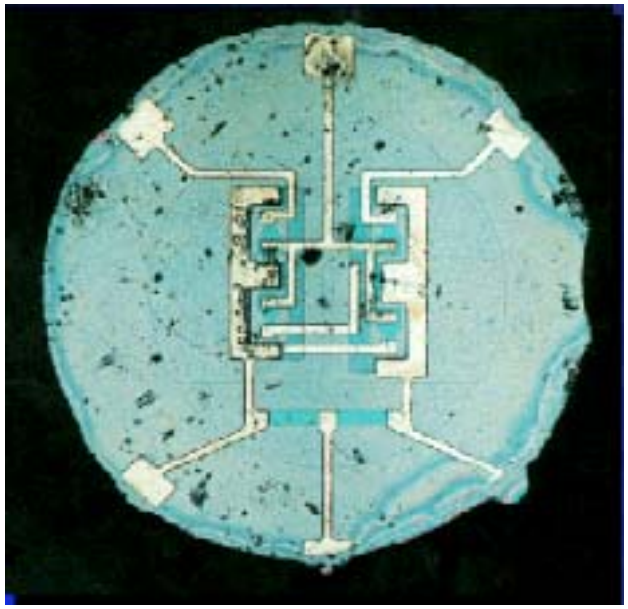


Fig. 6. The first planar integrated circuit, 1960. Designed and built by Lionel Kattner and Isy Haas under the direction of Jay Last at Fairchild Semiconductor. Courtesy of Lionel Kattner

It was reasonable to expect that an attempt to integrate entire computer processor on the single chip would occur when the integrated circuit fabrication process matured enough. This indeed happened as collaboration between a Japanese calculator producing company Busicom and a startup company Intel, a successful producer of semiconductor computer memory chips at the time. This first microprocessor, Intel's 4004 containing 2,108 transistors was build by Masatoshi Shima, Federico Faggin and Marcian E. "Ted" Hoff, under direction of Robert Noyce, in 1971. It could be said that 1971 was the beginning of the boom years in microelectronics. In the 35-year period, the industry has grown 80 fold with a compound annual growth of 14 percent. The number of transistors shipped per year has grown eight and a half orders of magnitude over that period, i.e. 300 million fold, maintaining an average growth of about 80 percent per year over the whole time period doubling every year over a significant period. More electronics was built in a year than existed in the beginning of that year.

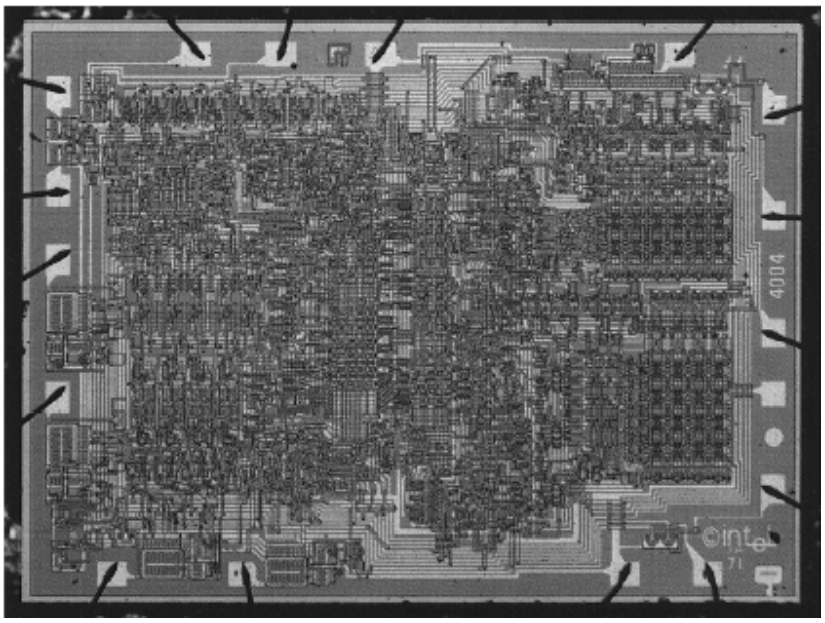


Fig. 7. The first microprocessor announced in 1971, Intel 4004 developed by Shima, Faggin and Hoff

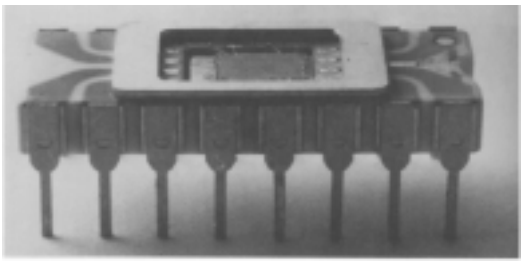


Fig. 8. Exernal view of the first microprocessor, Intel 4004 packaged in 16-pin standard dual-in line package.

The number of transistors integrated on a single chip continues to grow at an unprecedented rate. If there are estimated 10^{16} to 10^{17} ants in the world, Gordon Moore, Intel's founder, remarked in his keynote speech in 2003 that "each ant has to carry between 10 to a 100 transistors". This growth is illustrated in Fig. 9. Gordon Moore remarked that if the estimated number of printed characters produced every year is between ten to the seventeenth and ten to the eighteenth (representing all the newspapers, books, magazines, Xerox copies, the computer printouts), this is the same order of magnitude as the number of transistors that the industry produces every year. What is also phenomenal is that they are sold at about the same price as the printed character in the average Sunday New York Times. The transistor price has dropped from about a dollar to two-tenths of a micro-dollar. This number is an order of magnitude below at DRAMs with an average price of 50 million transistors for a dollar. This multiple million-fold reduction in cost requires a technology that has phenomenal capability. In addition it requires the contributions of a lot of people doing circuit design, providing clever extensions and developing the capability to continue it as well as technologists that keep the technology moving rapidly.

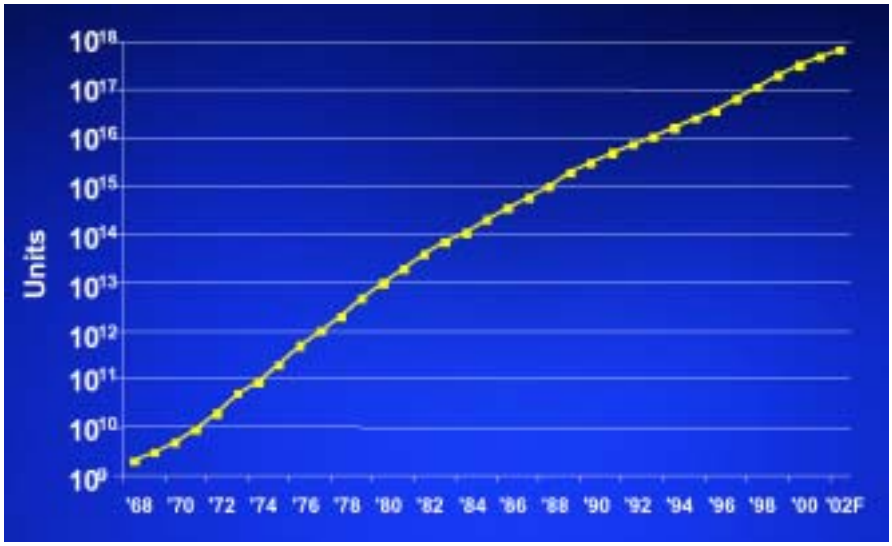


Fig. 9. Number of transistors shipped per year (Gordon Moore, keynote presentation ISSCC 2003, courtesy of Intel Corp.)

In an article written for the 35th anniversary of the Electonics Magazine on April 19, 1965, Moore predicted that the number of transistors in an integrated circuit will double every year. He did so by extrapolating from about 60 to 60,000 components in a period of ten years, never believing himself that this prediction will be precise. But in fact, it turned out to be more precise than he ever could have imagined. In 1975, he updated his projection and I argued why the slope was going to change from doubling every year to doubling every two years. The number of transistors on a die over the years is shown in Fig. 11. A few of the points shown over that time period are the most complex circuits available and they fit amazingly well on the curve. Carver Mead, a professor at Cal Tech, dubbed this Moore's Law.

Fitting more transistors on an integrated circuit requires remarkable inventiveness and progress across the number of disciplines: chemistry, solid-state physics, circuit theory and design, manufacturing etc. What is needed is the ability to shrink transistor area to about half the size for each new generation. In turn this made transistor faster, so the new generation of technology would result in an increase in clock frequency of about three times per generation, or doubling every two years. On the other hand the number of logic transistors is doubling every two years, while the increase in memory transistors has been higher, quadrupling in every new generation. A good illustration of the increase of the memory chip capacity is given in Fig. 12. An entire memory cell of 2002 memory chip fits more than comfortably in a space used for to make a contact in a 1978 memory chip.

Obviously the processor performance benefits from this growth roughly doubling every two years. In order to accommodate this growth, the size of the wafer had to grow too, but this growth has been not near as dramatic as the growth in the number of transistors. The size of the wafer has been increasing from the first 1” wafer in 1959 to 3” in 1974, moving further to 4” in 1978, 8” in 1988 to be reaching 12” in 1998. Currently

the advanced production facilities are using 12" wafers. Historical development of the wafer size is shown in Fig. 13.a, while Fig. 13.b. and c. show a view of the 12" wafer.

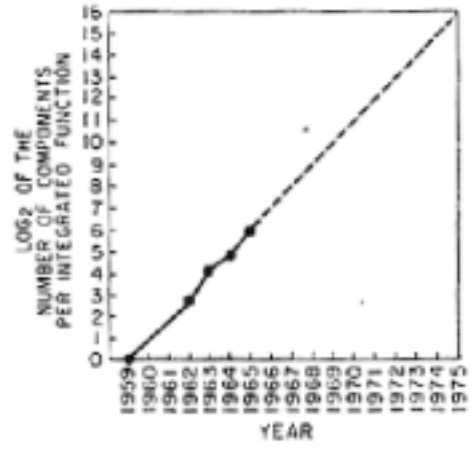


Fig. 10. Original Moore's prediction in 1965, (Electronics, Vol. 38, No.8, April 19, 1965)

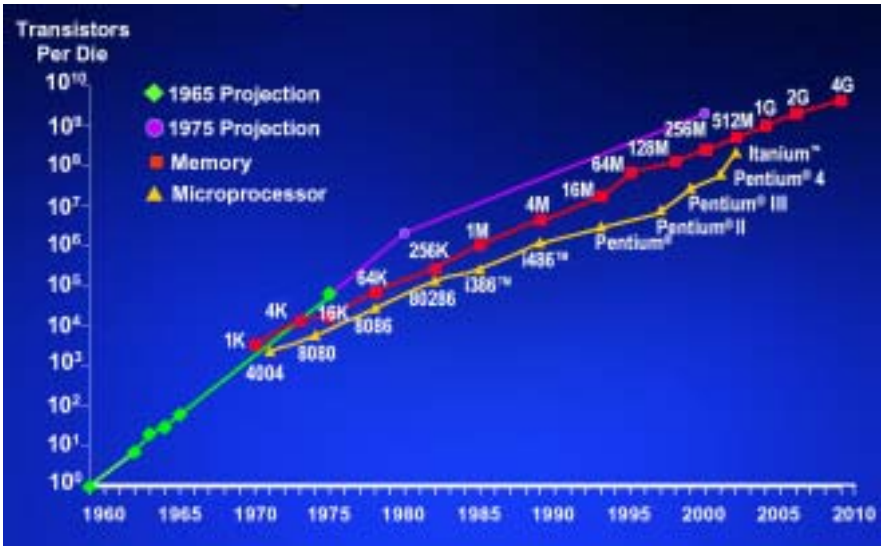


Fig. 11. Moore's law (ISSCC 2003)

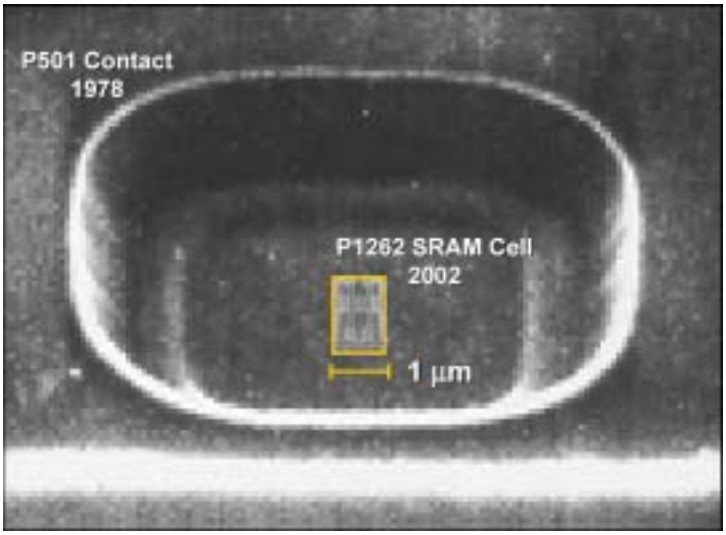


Fig. 12. SRAM memory cell of 2002 memory fits comfortably into a contact space of 1978 memory

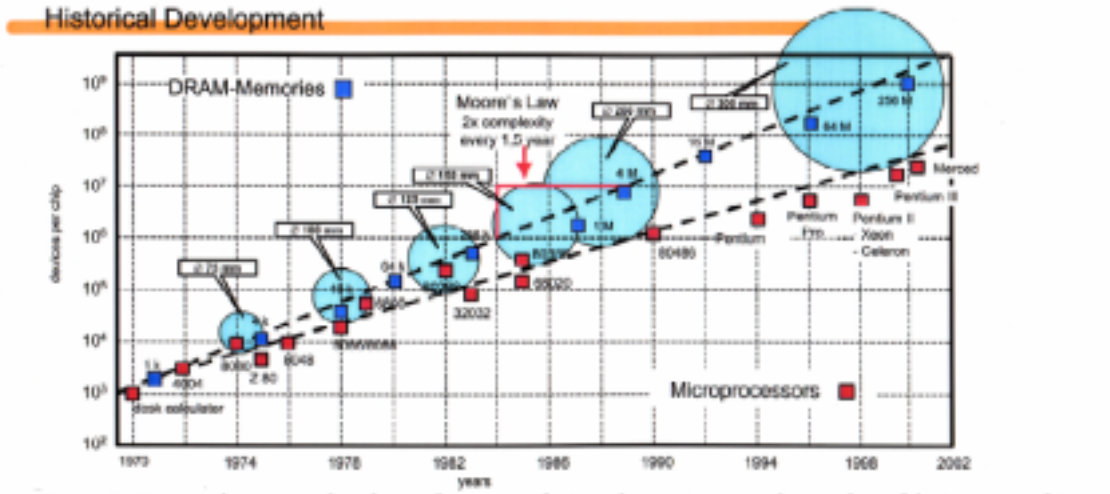
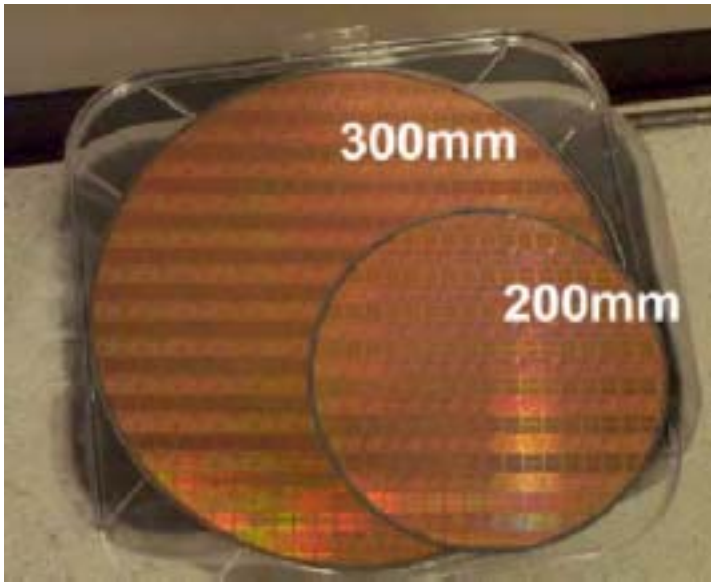
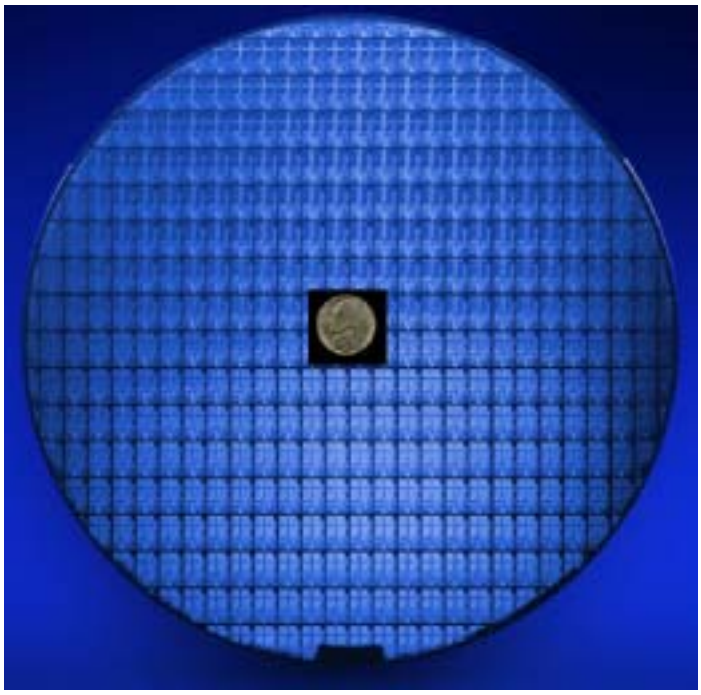


Figure 2: *Moore's law states that the performance of microelectronics, e.g., the number of devices on a chip, doubles every 18-24 months. The evolution has so far followed this prediction very well. For the future, there are different extrapolations, depending upon assumptions on the development of process technology. Also shown in the figure is the rapid development of the size of the silicon wafers.*

(a)



(b)



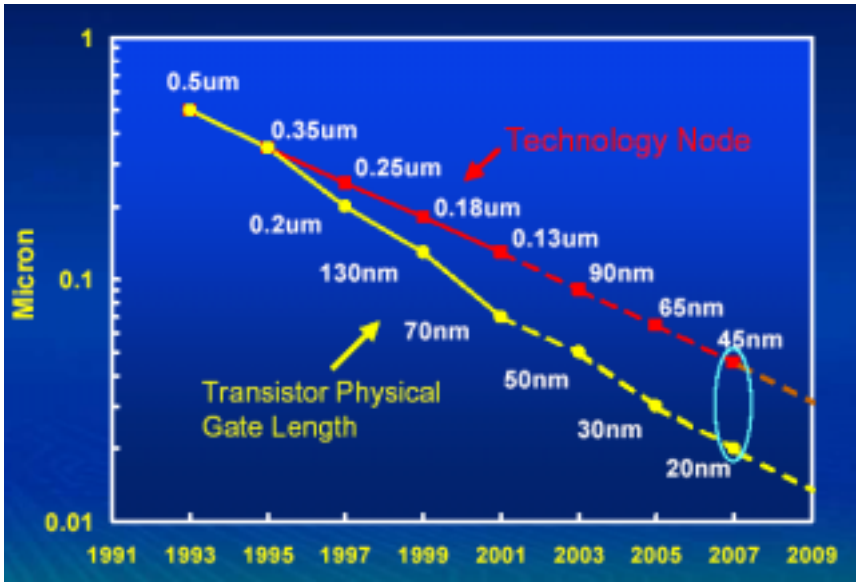
(c)

Fig. 13. (a) Historical growth of the silicon wafer over the years (b) Growth from 8" wafer to 12" wafer (c) Size of the 12" wafer as compared to a nickel coin

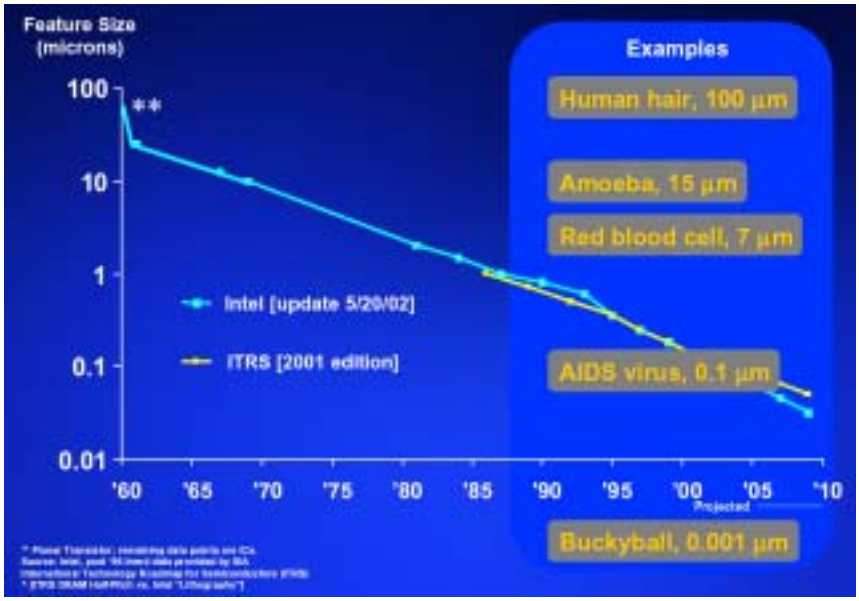
Scaling of the technology features, reducing the size of the lines, has been progressing at the rate of about 0.7 per generation. Since about 1993 this progress, which we call technology generation (or technology node), has been made every two years.

Using a rule of thumb we could estimate the reduction of the technology features to 70% for every generation from the previous one (every two years). Roughly that also means that the area occupied by a design will be reduced to about one half of the area occupied by the previous generation. However, the physical transistor size is reduced even further. For example the next step from the 0.25u technology would be into 0.18u technology, which is 70% of 0.25u. The change in the physical transistor size is actually from about 0.2u to 0.13u size, as illustrated in Fig. 14.a. An illustration of the actual transistor size as compared to some examples is shown in Fig. 14.b.

Since about 1995 the transistor size today has moved outside of the range of the visible light, given that the transistor features are smaller than the wavelength of the last visible color in the light spectrum. It was believed that this limit imposed on the optical lithography will represent a fundamental limit on how far the integration can go. However, with the use of X-ray lithography we have moved even further. It is believed that the technology will move to about 20-30nm features without any fundamental problems. Experimental fabrication results even confirm that this is possible. Some of the transistors that will be used in next generations of technology such as 2005, 2007 and 2009 are shown in Fig. 15.



(a)



(b)

Fig. 14. (a) Technology scaling over the years, (b) Comparison of technology features with the real world examples.

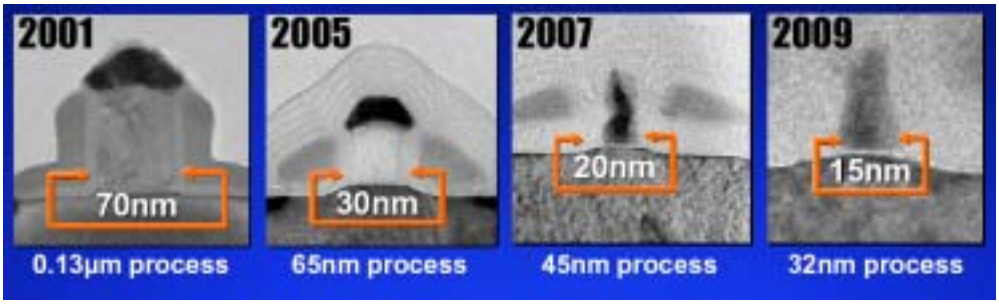


Fig. 15. Some of the experimental transistors to be used in next generations of technology

To be able to appreciate the progress made in VLSI technology one should look at the oxide thickness (the layer separating the transistor gate from the channel). In Fig. 16, we see how the oxide thickness is scaling for each technology generation. For example in 0.25u technology the physical oxide thickness is only about 35 Angstroms and moving toward 15 Angstroms for 0.13u technology generation. For 100nm technology the physical oxide thickness is 12 Angstroms (shown in Fig. 17.a) while for 70nm technology the physical oxide thickness will be only 8 Angstroms (Fig. 17.b), which is less than three layers of SiO_2.

Bellow 100nm dimension the conventional transistor structure may change and take a form of a three-gate structure in order to eliminate leakage currents. One such experimental transistor is shown in Fig. 18. Research in nano-structures may bring some

new and unusual configurations capable of processing the information on the atom level. In spite of reaching the atom level, some people are optimistic about the future progress.

We expect that after about 2010-2015 we will start running into some fundamental limits of what can be achieved with silicon. It will not be reasonable to expect any further scaling beyond, but this pessimistic prediction has been declared for the transistor dimensions reaching 1um and again at 0.25um. The optical lithography has, in the words of Gordon Moore, broken the laws of physics, because, in his words: "we are printing lines at a quarter of the wavelength of the light. This is something that I wouldn't have thought would have been possible". The relationship of the transistor line features to the wavelength of light used to process them is depicted in Fig. 19.

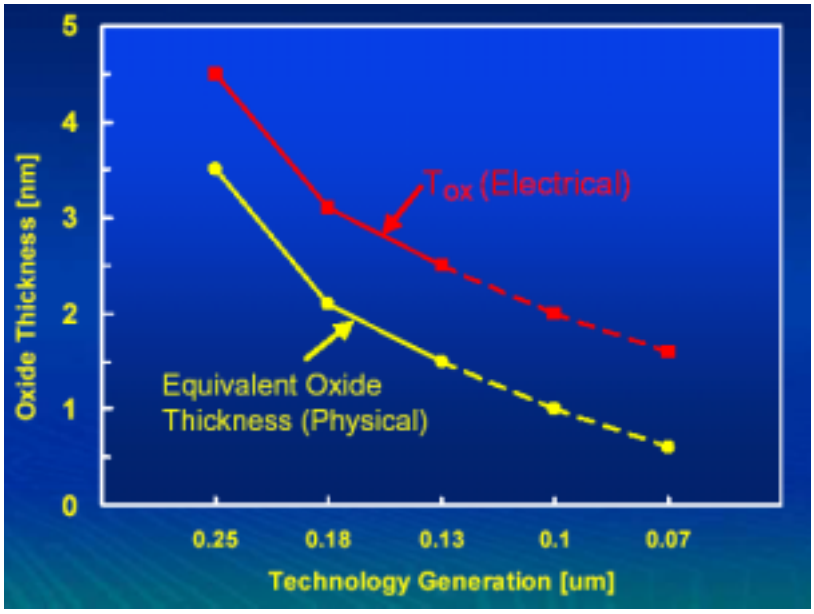
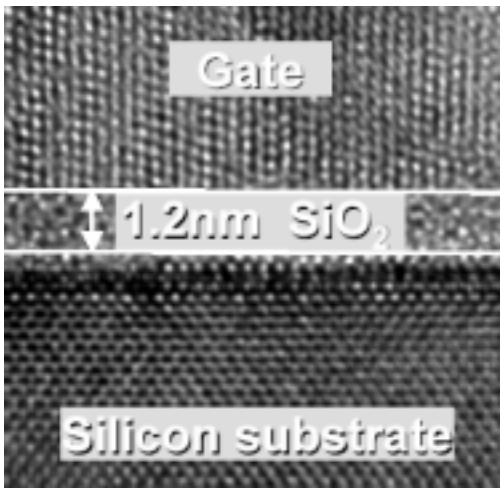
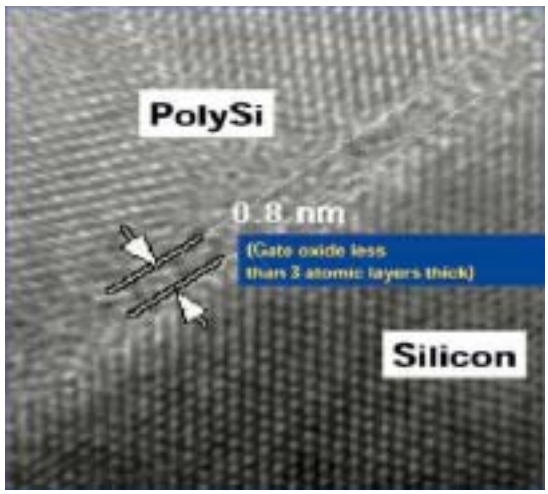


Fig. 16. Scaling of the silicon oxide over the technology generations





(a) (b)

Fig. 17. Oxide thickness for 100nm technology (a), oxide thickness for 70nm technology, it is less than 3 atomic layers thick.

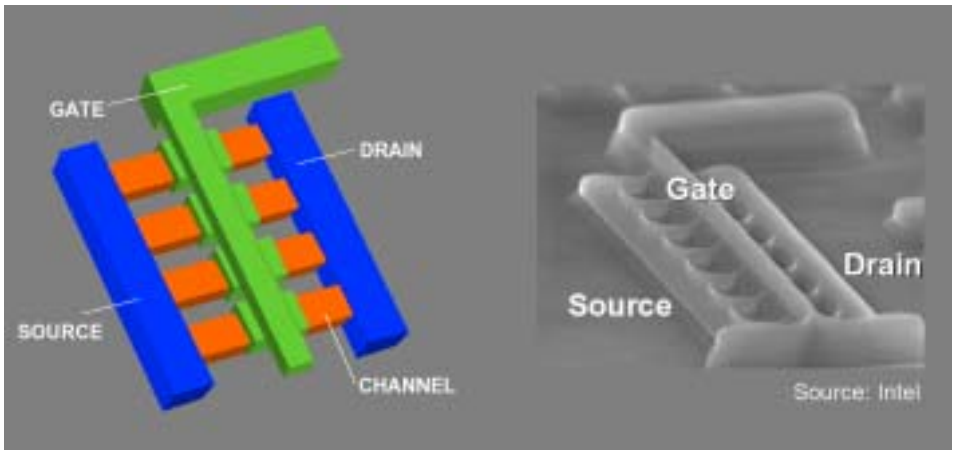


Fig. 18. Experimental three-gate transistor structure (the channel is surrounded by the gate on all three sides)

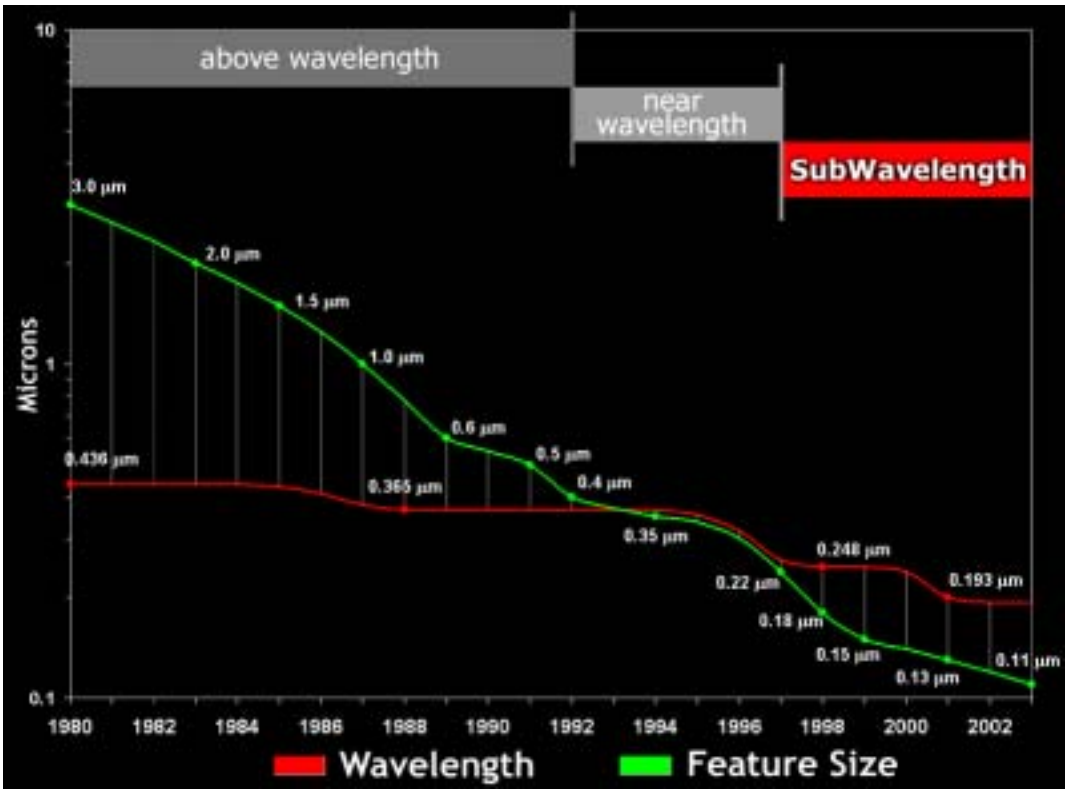


Fig. 19. The relationship of the light used for the optical lithography to the transistor lines

Such fabrication requires some tremendous investment. Today, estimated price of a new fabrication is about 2-4 billion of dollars. The worse part is that such investment will become obsolete in about 5-6 years. The picture of Extreme Ultraviolet Lithography tool is show in Fig. 20. Such machine operates at the 13nm wavelength, far bellow what humans can see: 400-700nm.

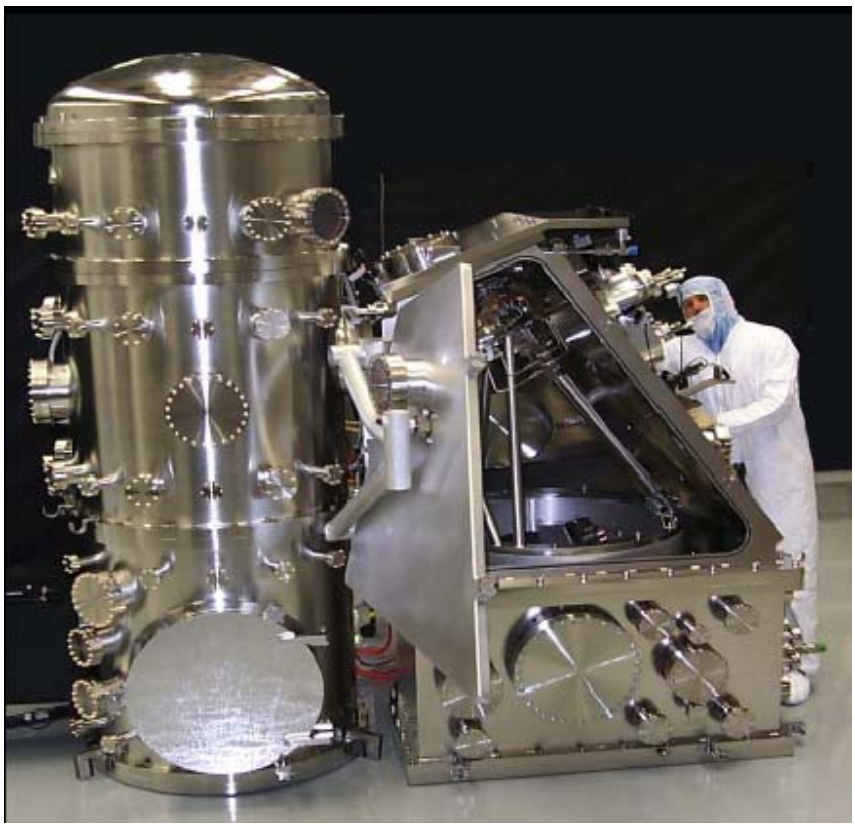


Fig. 20. Extreme Ultraviolet Litography machine used for 70nm fabrication process, costing several millions of dollars.

The VLSI progress has been facing many obstacles, but so far they have always been miraculously solved. Currently there are two notable problems (among many) on which VLSI research has been focusing. One is power and power density in the VLSI chip and other are leakage currents. The explosion of the numbers of transistors shipped each year, no matter how small, has its consequence in an increased need for energy. This is illustrated in Fig. 21. showing the increase in power consumption for all the microprocessor chips used to power personal computers. Obviously there is a need to design chips that consume less or a minimal amount of power. This requirement has been supported by a proliferation of mobile and portable consumer devices such as mobile telephones, laptop computers, personal digital assistants, games etc. They all operate from a battery and reducing power translates into longer operation between battery charging, or batteries that are smaller and weighting less.

In spite of all the obstacles and difficulties, VLSI progress continues with no signs of slowing down, at least for the next decade or more.

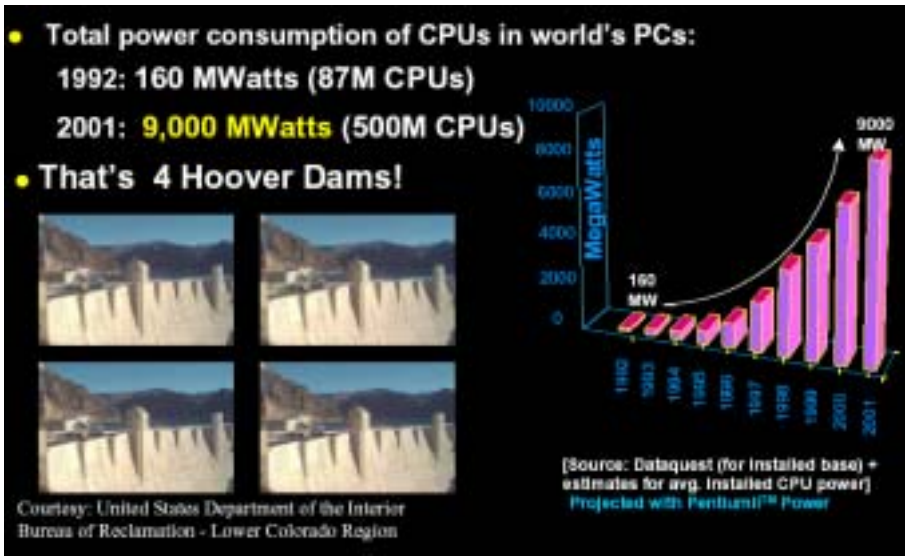


Fig. 21. Total power consumption increase in the world due to personal computer CPU chips only.

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