Pass-Transistor Adiabatic Logic Using Single Power-Clock Supply

Vojin G. Oklobdžija, *Fellow, IEEE*, Dragan Maksimović, *Member, IEEE*, and Fengcheng Lin

***Abstract*— We present a new pass-transistor adiabatic logic (PAL) that operates from a single power-clock supply and outperforms the previously reported adiabatic logic techniques in terms of its energy use. PAL is a dual-rail logic with relatively low gate complexity: a PAL gate consists of true and complementary NMOS functional blocks, and a pair of cross-coupled PMOS devices. In simulation tests using a standard 1.2 μ CMOS technology, the circuit has been found to operate up to 160 MHz clock frequency and down to 1.5 V peak-to-peak sinusoidal power-clock supply. Operation of a 1600-stage PAL shift register fabricated in the 1.2 μ CMOS technology has been experimentally verified.**

***Index Terms*— Adiabatic computing, energy recovery, low power logic.**

I. Introduction

LOW-ENERGY operation is a must in many portable and battery operated systems. Development of adiabatic logic, as an approach to reduce energy consumption of digital logic, has really taken off recently in the works of Athas, Koller and Svensson [1], [4], Younis and Knight [2], Hinman and Schlecht [3], Dickinson, Denker, Avery, Kramer, and Gabara [5]–[8]. The proposed adiabatic logic circuits utilize ac power supplies to recycle the energy used to charge node capacitances in the circuit. Although several interesting approaches have been presented, each encompassing many clever ideas, several weaknesses of these circuits can be identified: the implementation is overly complex [2]; the logic gates are not well suited for CMOS implementation [3]; multiple power-clock supplies are needed for proper stage-to-stage interfacing [4]–[7]; nonadiabatic transitions may compromise the energy savings [8].

In this paper we describe a new *pass-transistor CMOS adiabatic logic* (PAL) that requires only one sinusoidal power-clock supply, has simple implementation, and outperforms the previously published adiabatic logic families [6], [7] in terms of energy consumption.

II. PAL Operation

PAL is a dual-rail logic with pass-transistor NMOS functional blocks f and $\bar{f}$, and a pair of cross-coupled PMOS devices Q_1, Q_2 in each stage, as illustrated by the example of Fig. 1, which performs the 2:1 MUX function: $F1 = A \cdot S + B \cdot \bar{S}$. The PAL gate is supplied by a sinusoidal power-clock PC. Operation of the gate in Fig. 1 can be summarized as follows: initially PC $= 0$, and PC starts to raise. Suppose that the inputs A and S are high, making a conducting path from the power-clock PC to the output $F1$. Given that $F1$ is connected to PC, $F1$ will start raising from 0 toward the peak of PC. The node $\overline{F1}$ will be "tri-state" and kept close to 0 V by the load capacitance of the subsequent gates. As the power clock PC ramps up, the PMOS transistor Q_1 turns on, and the output $F1$ is charged up to the peak of PC. The transistor Q_2 will stay off. The power clock will then ramp down toward zero, recovering the energy stored on the $F1$ node capacitance.

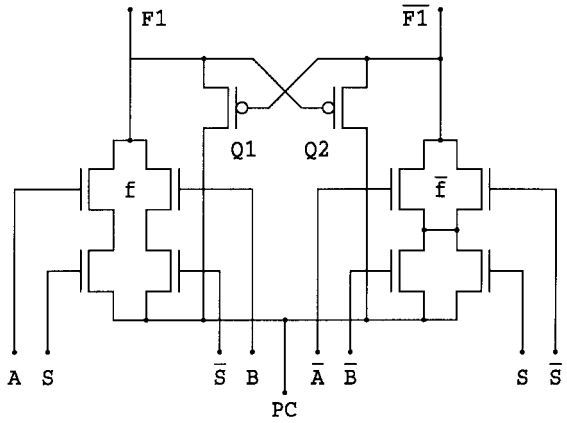

Fig. 1. 2:1 MUX implemented with PAL.

The complexity of the logic gate is relatively low, close to that of the style proposed in [7]. The dual-rail nature of the PAL implies that the function f will have to be duplicated as $\bar{f}$. However, this will not necessarily result in a 100% duplication because it is possible to "share" transistors in the realization of the NMOS functional blocks f and $\bar{f}$.

In a chain of PAL gates, the sinusoidal voltage PC supplies all even logic stages, while the inverted (phase-shifted by 180°) sinusoidal voltage $\overline{\text{PC}}$ supplies all odd logic stages. Both PC and $\overline{\text{PC}}$ can be obtained from an efficient single-inductor LC oscillator [5], [8], [9] that can serve as the PAL power supply.

The stage-to-stage interface is illustrated in Fig. 2, where the functional block per stage is a single NMOS pass transistor. Fig. 2 also shows several cycles of the power clocks PC and $\overline{\text{PC}}$, logic input $F0$ and logic output $F1$, as well as the energy consumption $W(t)$ for a gate supplied by PC. Note how the logic output $F1$ is delayed with respect to the logic input $F0$ by one-half of the power-clock period. The chain of PAL gates in Fig. 2 operates as a shift register. The simulation results in Fig. 2 are obtained for the case when a periodic sequence $\cdots$ 1010 $\cdots$ is propagated through the chain. The energy

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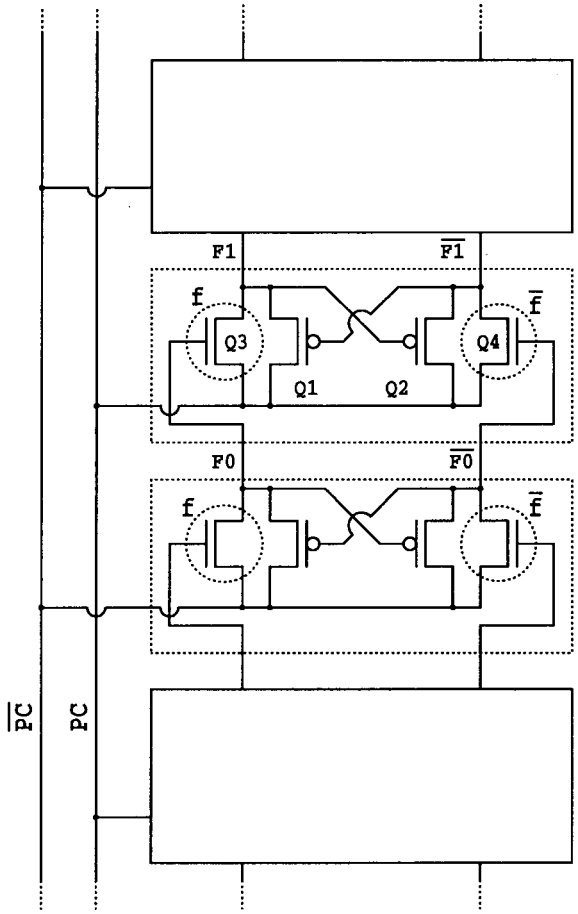

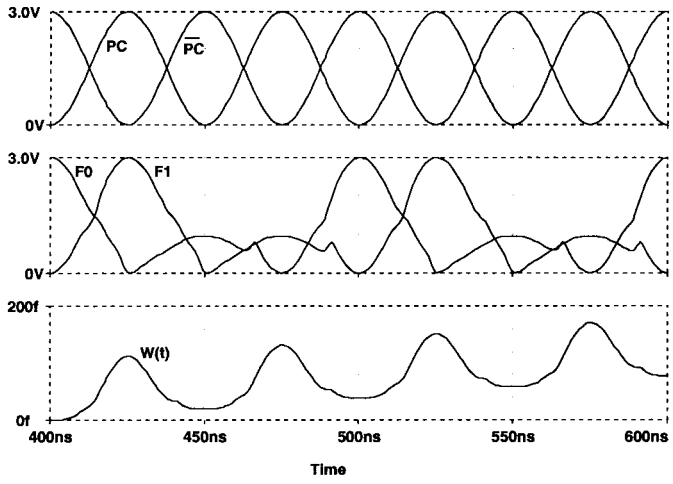

Fig. 2. A chain of simple PAL gates (shift register), and simulation waveforms: power clocks PC and $\overline{\text{PC}}$; logic input $F0$ and logic output $F1$; energy consumption $W(t)$ per gate. Power-clock frequency is 20 MHz. All device sizes are 1.8 μm/1.2 μm in a standard 1.2 μm CMOS technology.

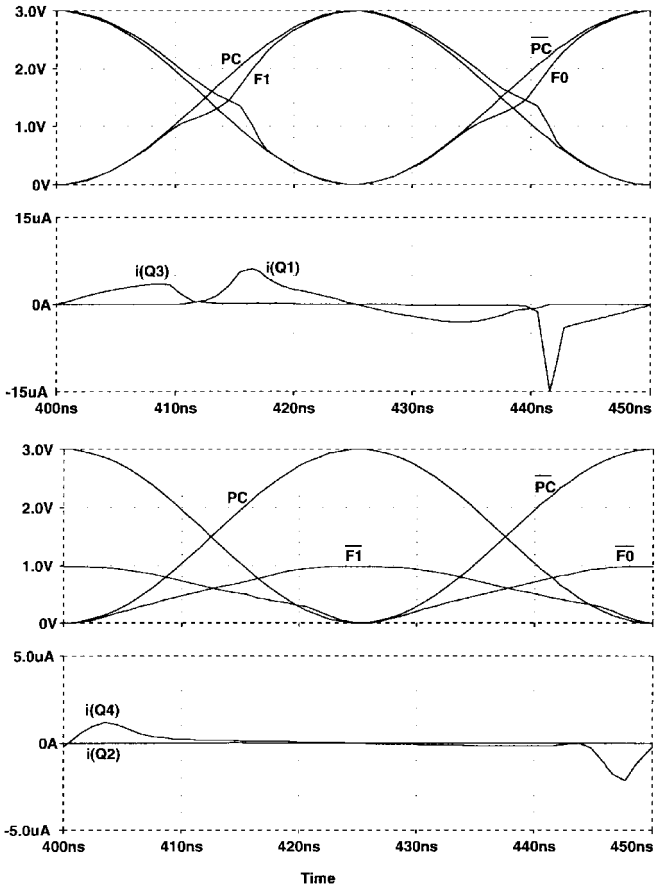

Fig. 3. Details of waveforms in the gate of Fig. 2 during one period of the power clock PC.

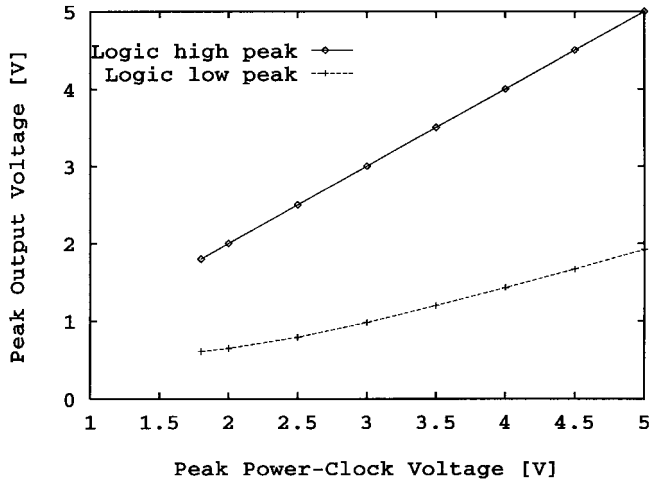

Fig. 4. Peak voltage of a logic high output and a logic low output as functions of the power-clock peak voltage. The simulation results are obtained for the chain of PAL gates shown in Fig. 2 at the power-clock frequency equal to 20 MHz. The device threshold voltages are $V_{tn} = 0.65$ V and $V_{tp} = -0.85$ V.

consumption waveform $W(t)$ shows how the energy is first delivered from the power-clock supply during the part of the clock period when PC is raising, and is then partially recovered during the part of the period when PC is going down. In this example, the energy loss per clock period is 19 fJ per gate.

Details of waveforms during one power-clock period are shown in Fig. 3. The logic operation has only two phases: *evaluate* (E), when the power clock is ramping up, and *discharge* (D), when the power clock is going down. The E phase of an odd stage coincides with the D phase of an even stage. Consider the stage with the logic inputs $F0$ and $\overline{F0}$ in Fig. 2. Initially, when $\text{PC} = 0$, both output nodes $F1$ and $\overline{F1}$ are discharged. During the E phase, when the PC starts ramping up, there is a path through one of the functional blocks because one of the logic inputs (let us assume $F0$) is

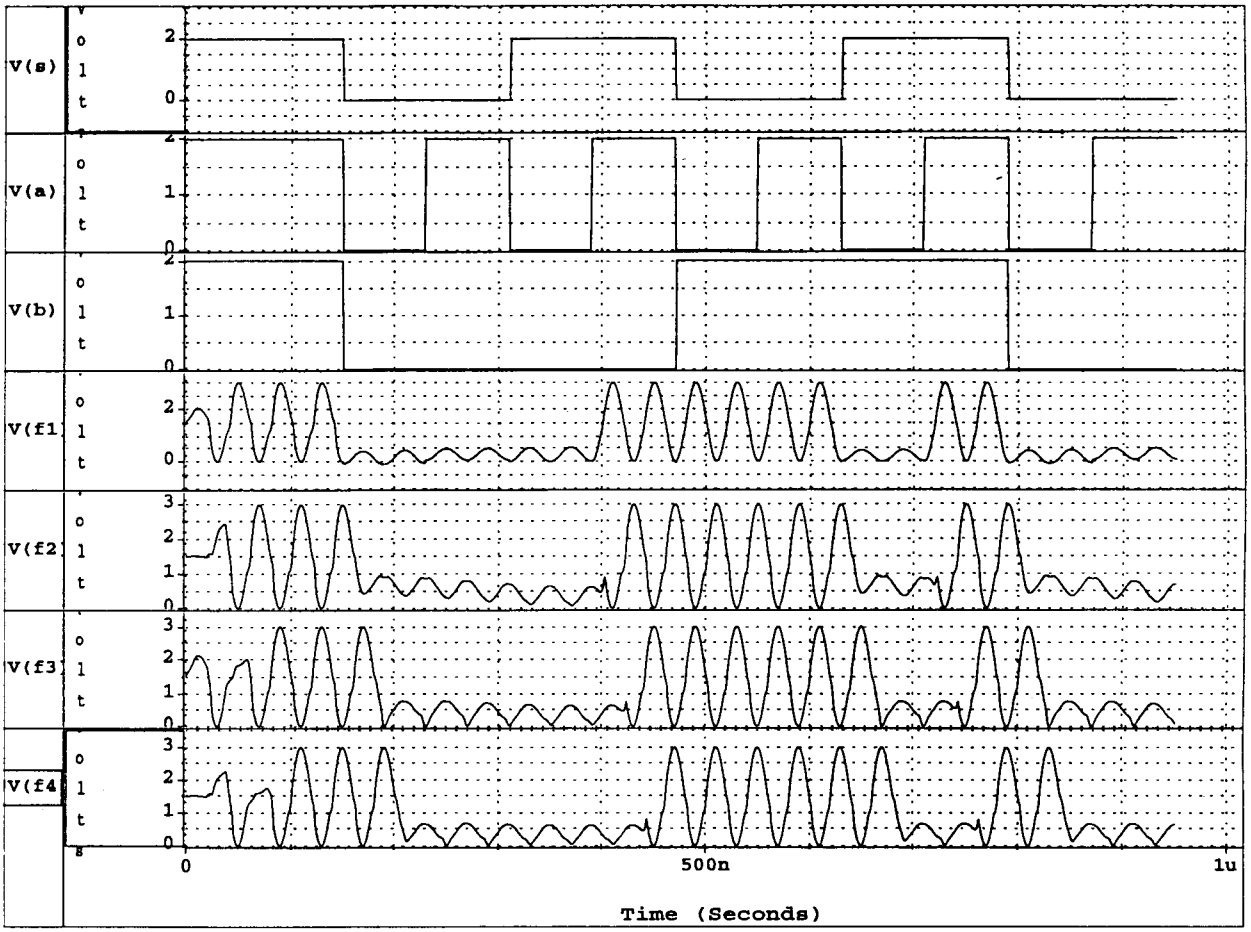

Fig. 5. Simulation waveforms obtained for a chain of 2:1 MUX PAL gates of Fig. 1. All device sizes are the same: $W/L = 1.8\ \mu$m/1.2 μm.

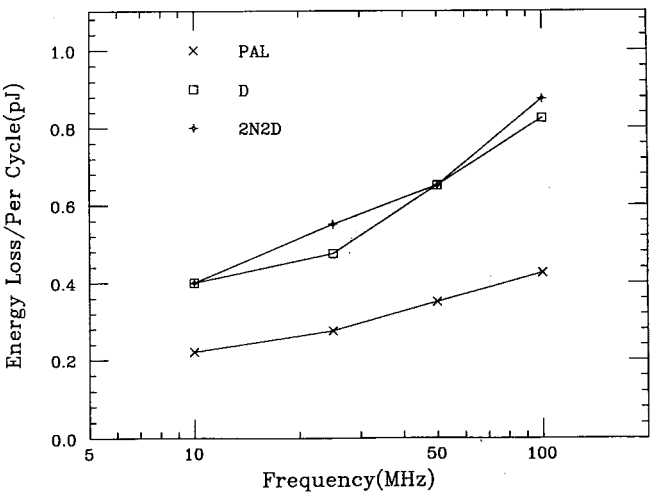

Fig. 6. The energy consumption versus power-clock frequency for a chain of 10 2:1 MUX gates implemented using PAL, the logic proposed by Denker (D) [7], and the 2N2D logic [6]. All device sizes are the same: $W/L = 1.8$ μm/1.2 μm. The peak power-clock voltage is 3 V.

at the peak of the power clock. Therefore, the output node $F1$ will begin to ramp up following the power clock PC. Once the voltage difference between $F1$ and $\overline{F1}$ increases above $|V_{tp}|$, where V_{tp} is the PMOS threshold voltage, Q_1 turns on and the $F1$ node capacitance is charged up through Q_1 to the peak of PC. As shown by the current waveforms $i(Q3)$and $i(Q1)$, the charge is initially supplied to the output node through $Q3$ (through the NMOS functional block f), and then by the PMOS device $Q1$. The other PMOS device $Q2$ stays off during this clock period because $F1$ closely follows PC and is always greater than $\overline{F1}$. The complementary output $\overline{F1}$ is tri-stated, and would ideally stay at 0 during the clock period when $F1$ follows the power clock. However, as shown by the simulation waveforms of Fig. 3, $\overline{F1}$ does not stay at zero. This is because the device $Q4$ (the complementary NMOS functional block $\bar{f}$) is conducting during a brief interval at the beginning, and at the end of the PC period, and because of capacitive coupling from the previous stage. Since $Q4$ is turned off earlier than $Q3$, and since the charge-up at node $\overline{F1}$ is not supported by the PMOS device $Q2$, the peak of $\overline{F1}$ is significantly lower than the peak of $F1$. Fig. 4 shows how the peak of the logic high and the logic low outputs depend on the peak of the power-clock supply. The results are obtained by simulation of the chain of PAL gates shown in Fig. 2 at the power-clock frequency equal to 20 MHz. The correct logic levels can be sampled at the peak of the power clock, although the tri-stated output is susceptible to parasitic charge coupling.

During the discharge phase D, the power clock is ramping down. Initially, the discharge of the node $F1$ is assisted by the PMOS device Q_1. At the time when PC approaches zero, logic high inputs are close to the peak of $\overline{\text{PC}}$, and the final portion of the discharge is done through the conducting functional block.

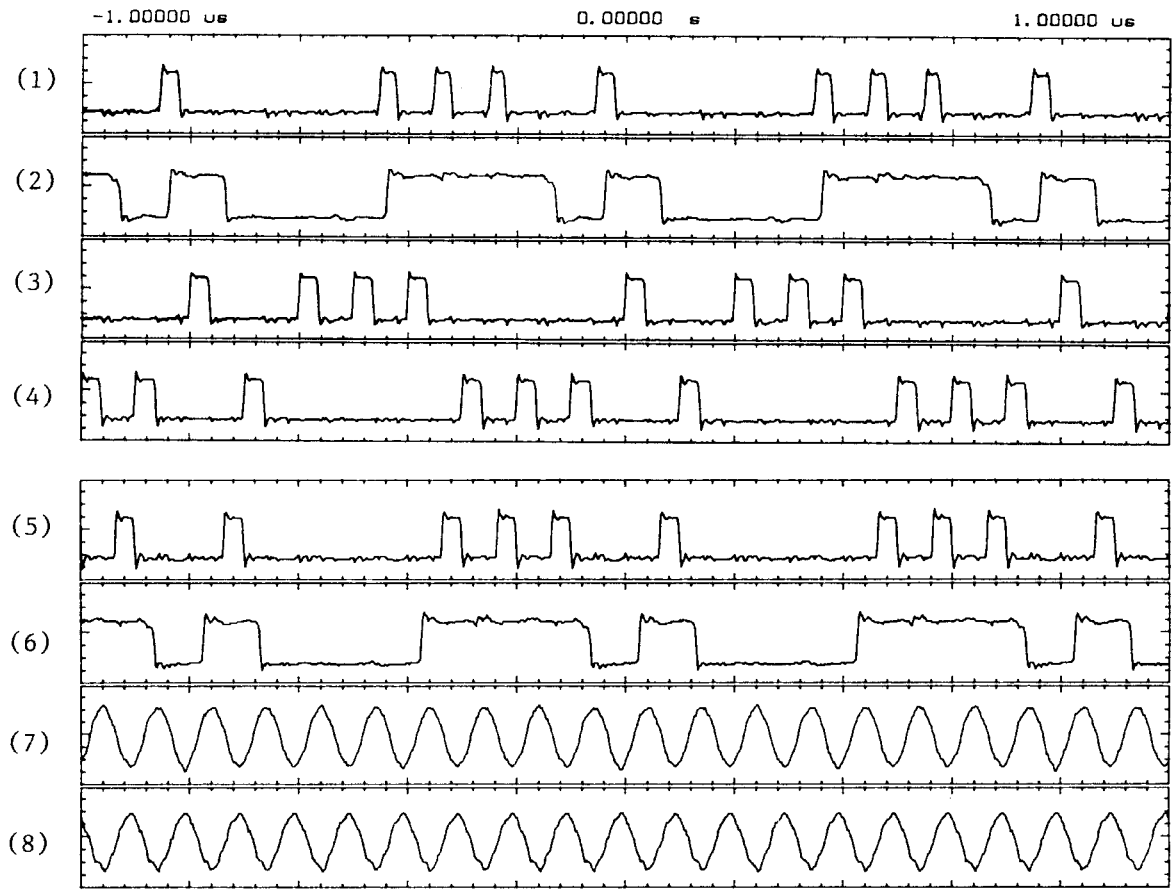

Fig. 7. Experimental waveforms obtained from a 1600-stage PAL shift register fabricated in 1.2 μ CMOS. Top-to-bottom (5 V/div, 200 ns/div): (1) output #1600; (2) input; (3) output $\overline{\#3}$; (4) output #3; (5) output #17; (6) input; (7) power clock $\overline{\text{PC}}$; (8) power clock PC. The periodic test sequence is $\cdots$ 11101000 $\cdots$. The sinusoidal 10 MHz power-clocks are 3.6 V peak-to-peak, with 1.8 V dc offset.

Above-threshold logic low inputs help discharge both outputs down to approximately zero volts without excess energy loss.

III. Simulation and Experimental Results

Fig. 5 shows the Spice simulation waveforms obtained for a chain of 2:1 MUX gates of Fig. 1 (extracted from layout), using device models available for a standard 1.2 μ CMOS technology. Logic inputs to the first gate in the chain are square-wave. In the simulation tests, the circuit has been found to operate up to the power-clock frequency of 160 MHz, and down to 1.5 V peak-to-peak sinusoidal power-clock supply voltage.

A comparison of energy consumption vs. power-clock frequency has been made against the 2N2D logic [6], and the logic proposed in [7]. The results obtained by simulation on the chain of 2:1 MUX gates are shown in Fig. 6. PAL outperforms the other two logic families in this comparison, while operated from a single two-phase power-clock supply.

A 1600-stage PAL shift register, a part of which is shown in Fig. 2, has been fabricated in the 1.2 μ CMOS technology available through MOSIS. For testing purposes, conventional dc-supplied CMOS buffers were placed between selected PAL outputs and the output pins. Odd stages are supplied by PC, even stages by $\overline{\text{PC}}$. Fig. 7 shows experimental waveforms obtained for the power-clock frequency equal to 10 MHz, and a periodic test sequence $\cdots$ 11101000 $\cdots$ passed through the shift register. The sinusoidal power-clocks were 3.6 V peak-to-peak, with 1.8 V dc offset. The conventional buffers are supplied by $V_{\text{DD}} = 4$ Vdc, and operate as voltage comparators: the logic high can be observed at an output pin as a pulse centered around the peak of the power-clock waveform. The experimental waveforms verify operation of the PAL shift register. More extensive tests, including power-consumption measurements, are under way.

IV. Conclusion

The pass-transistor adiabatic logic (PAL) circuit described here is a dual-rail logic supplied by a single two-phase AC power clock. The PAL gate complexity is relatively low: a PAL gate consists of true and complementary NMOS functional blocks, and a pair of cross-coupled PMOS devices. In simulation tests using a standard 1.2 μm CMOS technology, the circuit has been found to operate up to 160 MHz clock frequency and down to 1.5 V peak-to-peak sinusoidal power-clock supply. It outperforms the previously published adiabatic logic techniques in terms of energy consumption. Operation of a 1600-stage PAL shift register fabricated in the 1.2 μm CMOS has been experimentally verified.

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Fengcheng Lin, photograph and biography not available at the time of publication.