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Multi-Level Pass-Transistor Logic for Low-Power ULSIs

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Abstract

Multi-level pass-transistor logic (MPL) removes the redundancy in conventional single-level pass-transistor circuits to improve both power and delay. MPL is synthesizable based on the multi-level binary decision diagram, a new logic representation, and it has the potential to replace CMOS in any synthesized control block of an MPU. Overall improvement in the product of power, delay, and area of 42 % over CMOS is confirmed in actual microprocessor benchmark tests.

Introduction

Pass-transistor logic needs fewer transistors than conventional CMOS logic to perform the same function. Decreasing the number of transistors reduces not only power but also delay. However due to the difficulty of the synthesis, pass-transistor logic has not been used in random logic circuits. To overcome this difficulty, we previously developed an integration technique that features a new logic synthesizer with an original cell library as shown in Fig. 1 [1].

The pass-transistor logic we developed was a single-level logic. In CMOS circuits, however multi-level logic plays an important role in power and delay reduction, so it is conjectured that multi-level logic is essential to improve pass transistor circuits. But a good synthesis method combined with multi-level logic is needed to developg multi-level pass-transistor circuits. For single-level pass transistor logic, we developed a technique that uses a graph representation called a binary decision diagram (BDD)[2], because it conforms well with pass transistor circuits in that a node in a BDD corresponds to a pass-transistor multiplexer as shown in Fig. 2. In CMOSs, multi-level logic optimization using Boolean manipulation is well established, so we tried to apply this technique to the BDD-based pass-transistor synthesis. But due to the wide difference between the Boolean equation and BDD, it was very difficult to make use of the CMOS factorization technique for pass-transistor logic synthesis. So we developed a new optimization technique based on the BDD that made possible the use of MPL.

Multi-Level Pass-Transistor Logic

MPL is a hierarchical logic unlike single-level pass-transistor logic. The hierarchy is expanded in the direction of "gate inputs" (Fig. 3). In the conventional logic the source-drain inputs are connected to each other and gate inputs are driven only by the primary inputs. On the other hand. in MPL gate inputs are driven by either primary inputs or the outputs of other pass transistor circuits.

The advantage of MPL in terms of power and small area comes from the high sharing capacity of the circuits. MPL shares circuits in the upper level which are generated separately when using single-level pass-transistor logic. The more a circuit is shared , the more redundant transistors can be eliminated. Another advantage lies in its parallel operation in contrast to the sequential operation of single-level logic. Parallel operation changes the order of delay time from $O(n)$ to $O(\log n)$, where n is the number of inputs. This change results in a conspicuous improvement in circuits with large delay.

How multi-level circuits can be constructed is the key to MPL. Instead of using the conventional Boolean technique, we developed a technique based on a new extension of BDD. Multi-level pass transistor circuits are derived from this extended diagram by replacing all edges with multiplexers using pass-transistors and by inserting buffers where needed. We call this extension multi-level BDD and it is obtained through an algorithm which consists of the following three steps as shown in Fig. 4.

1) Extract partial diagrams from the original BDD, each of which share a logic (Fig. 4. (a)).
2) Replace extracted diagrams with new diagrams each of which have the same number of leaves as the original partial diagrams (Fig. 4. (b)).
3) Construct the upper-level logics for the control inputs of the replaced nodes. These new logics are adjusted to be the same as the original ones (Fig. 4. (c)).

An example of the effect of sharing logic is shown in Fig. 5. In this circuit a logic is shared by two outputs in the second level and two pass-transistors are eliminated.

The reduction in the delay time is illustrated in Fig. 6. Pass-transistor circuits for 8-NAND logic using conventional pass transistor logic and MPL are shown. In the conventional circuit, the critical path consists of seven cascaded pass transistors and three buffers. On the other hand, in MPL the critical path consists of only three cascaded pass transistors and one buffer.

Experimental

We applied MPL to 27 randomly selected circuits. These were mainly random logic circuits in a microprocessor. The delay time using MPL was compared with that of single-level pass-transistor logic as shown in Fig. 7. The effect of the multi-level optimization is clearly confirmed in circuits which have large delay. Also the power, the area, and the delay when using MPL were compared with those of conventional CMOS logic as shown in Fig. 8. On average, power was reduced by 23 % and area was reduced by 15 %. The delay time was also reduced by 12 %. The overall improvement with MPL was 42 %.

Acknowledgments

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Reference

[1] K. Yano, Y. Sasaki, K. Rikino, K. Seki, 1994 CICC, pp603-606.
[2] R. Bryant IEEE Trans. Comp., Vol. c-35, pp677-691, Aug. 1986

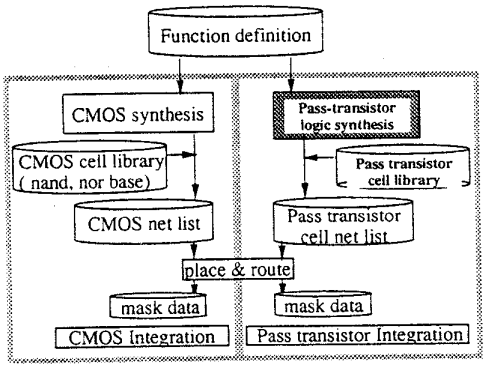
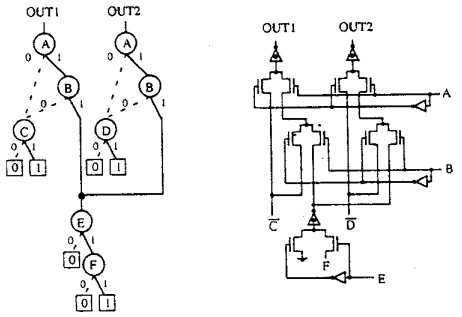
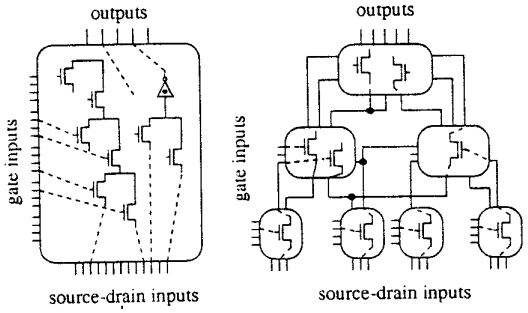


Fig. 1 CMOS integration vs. pass transistor integration



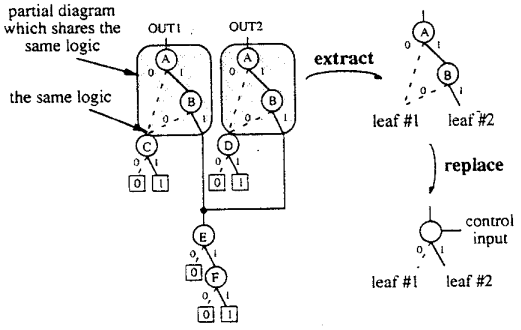
(a) BDD (b) Pass-transistor circuit

Fig. 2 Conventional pass-transistor logic synthesis using BDD

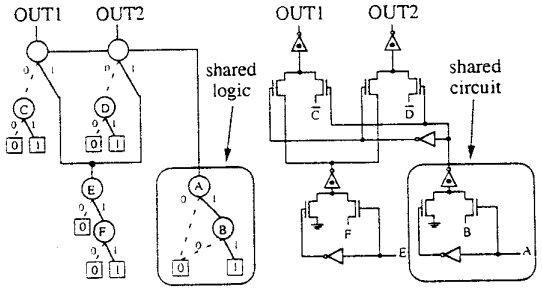


(a) Conventional (b) MPL

Fig. 3 Conventional pass-transistor logic vs. MPL

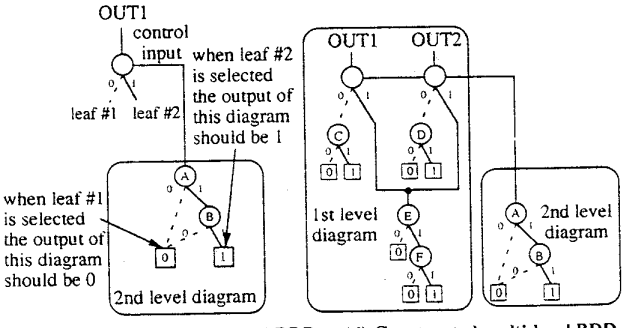


(a) Extract (b) Replace



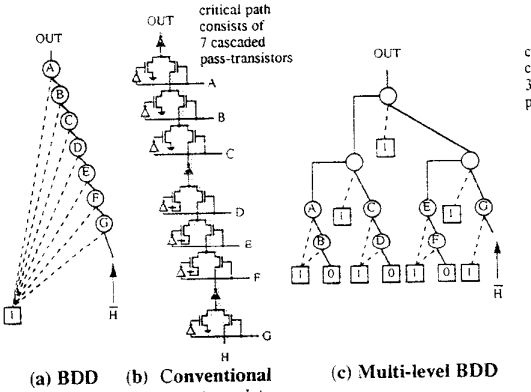
(a) Multi-level BDD (b) Multi-level pass-transistor circuit

Fig. 5 Transformation into a multi-level pass-transistor circuit



(c) Construct the upper-level BDD (d) Constructed multi-level BDD

Fig. 4 Construction of multi-level BDD



(a) BDD (b) Conventional pass transistor circuit (c) Multi-level BDD (d) Multi-level pass transistor circuit

Fig. 6 Delay time reduction (8-NAND logic)

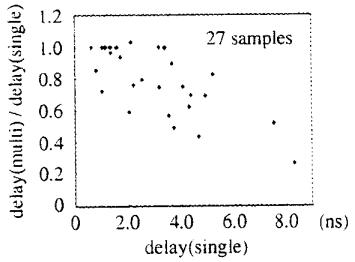


Fig. 7 Single-level pass-transisor logic vs. MPL

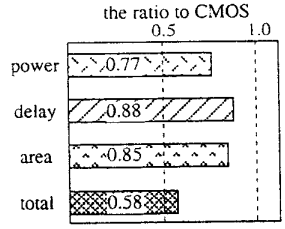


Fig. 8 CMOS vs. MPL in benchmark tests