Lecture 4

Model Calibration
Optimal Gate Sizing

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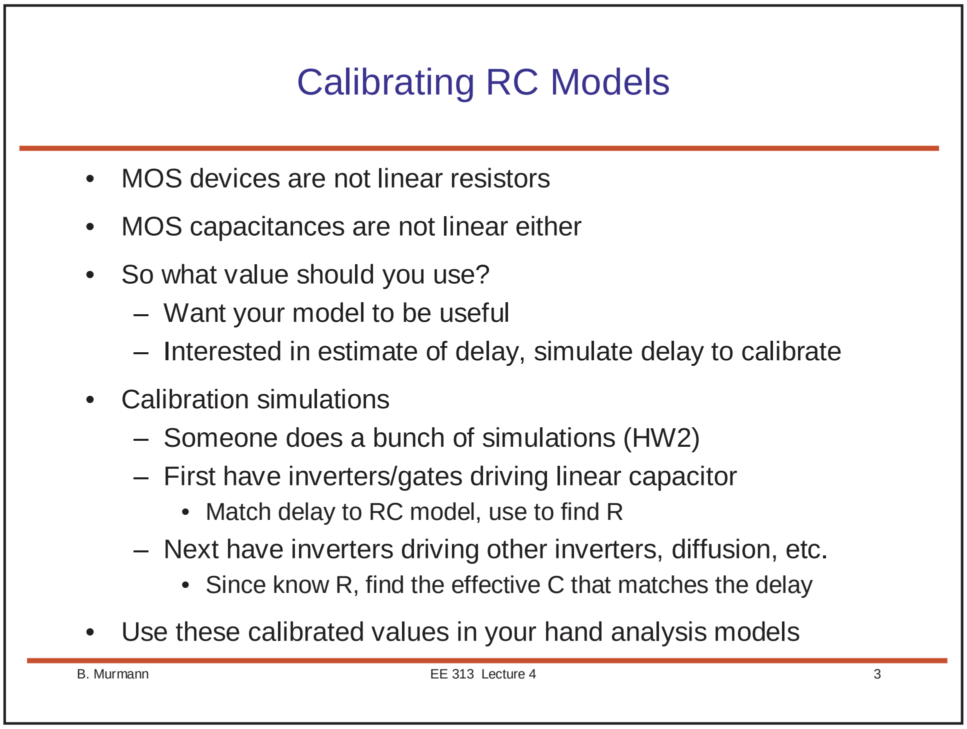
Overview

- **Reading**
  - Hodges 4.8, 6.5

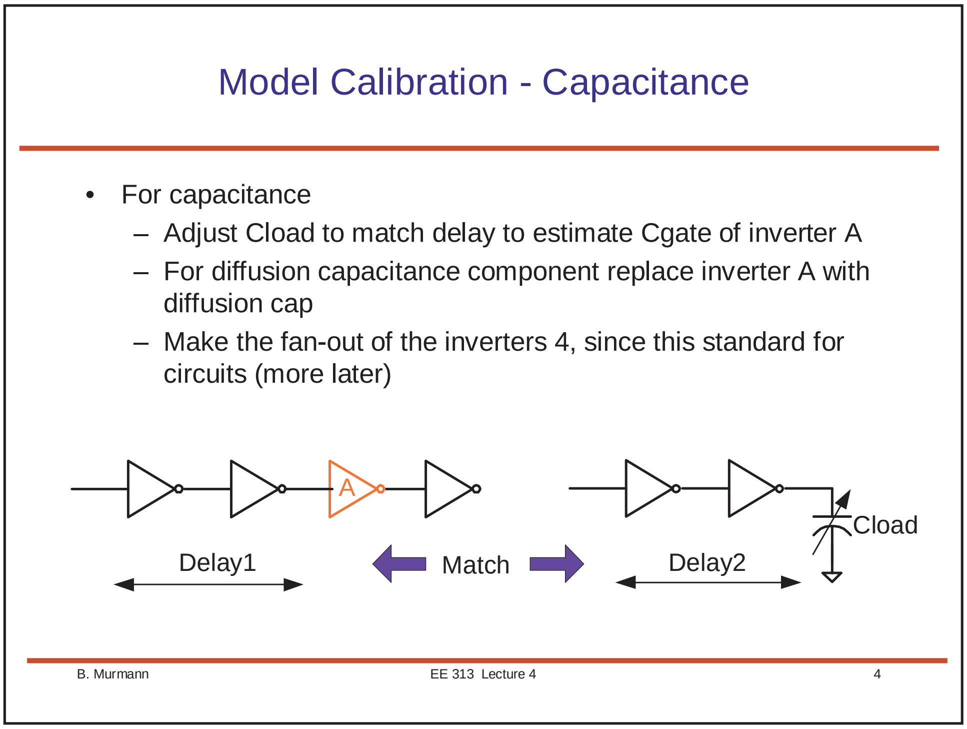
- **Introduction**

  The goal of this lecture is to provide you a set of tools for evaluating the performance of different gates, and optimize their performance in a chain of gates by changing their relative sizes. Using these tools you can quickly see why dynamic gates are faster than static CMOS gates, as well as the optimal way to size different gates in a sequence. To develop this set of tools we need to look at a very simple delay problem first, and that is the delay in a chain of inverters. Then we will take this result and look at a chain of logic gates. Before we start either of these tasks, we first look at how to get the RC values to use in our models.



Calibrating RC Models

- MOS devices are not linear resistors
- MOS capacitances are not linear either
- So what value should you use?
  - Want your model to be useful
  - Interested in estimate of delay, simulate delay to calibrate
- Calibration simulations
  - Someone does a bunch of simulations (HW2)
  - First have inverters/gates driving linear capacitor
    - Match delay to RC model, use to find R
  - Next have inverters driving other inverters, diffusion, etc.
    - Since know R, find the effective C that matches the delay
- Use these calibrated values in your hand analysis models

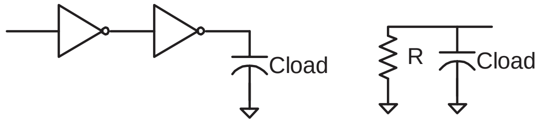


Model Calibration - Capacitance

- For capacitance
  - Adjust Cload to match delay to estimate Cgate of inverter A
  - For diffusion capacitance component replace inverter A with diffusion cap
  - Make the fan-out of the inverters 4, since this standard for circuits (more later)

Model Calibration - Resistance

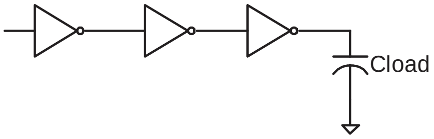
- For resistance
  - From the Cload experiment we get both the gate delay, and the effective input capacitance. R can be estimated by calculating Delay/Cload.
  - Typical values: Rsqn=12.5k/sq, Rsqp=30k/sq
    - For typical 0.13µm...0.35µm CMOS technologies



Calibration Issues

- Need to understand what the components depend on to make sure you are creating values that will give good estimates
- Resistance
  - Depends on gate overdrive, so need to get the correct V_{DD}
    - This might not be V_{DD} nominal, since you might want some margins. Generally measure delay at worst-case operating voltage, which is V_{DD} – 15%
  - Depends on input rise-time.
    - As we will see later, it actually depends on the ratio of input rise-time to output delay. So when we measure resistance, we need to use the correct input slope
    - First inverter in the calibration setups is used to make the input slope correct

Inverter Sizing

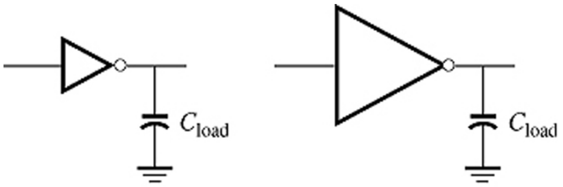


- Assume we have some load we need to drive, Cload
- Want to minimize the delay it takes to drive the load
  - Find the right number of inverters needed to drive load
  - Find the right sizes for these inverters

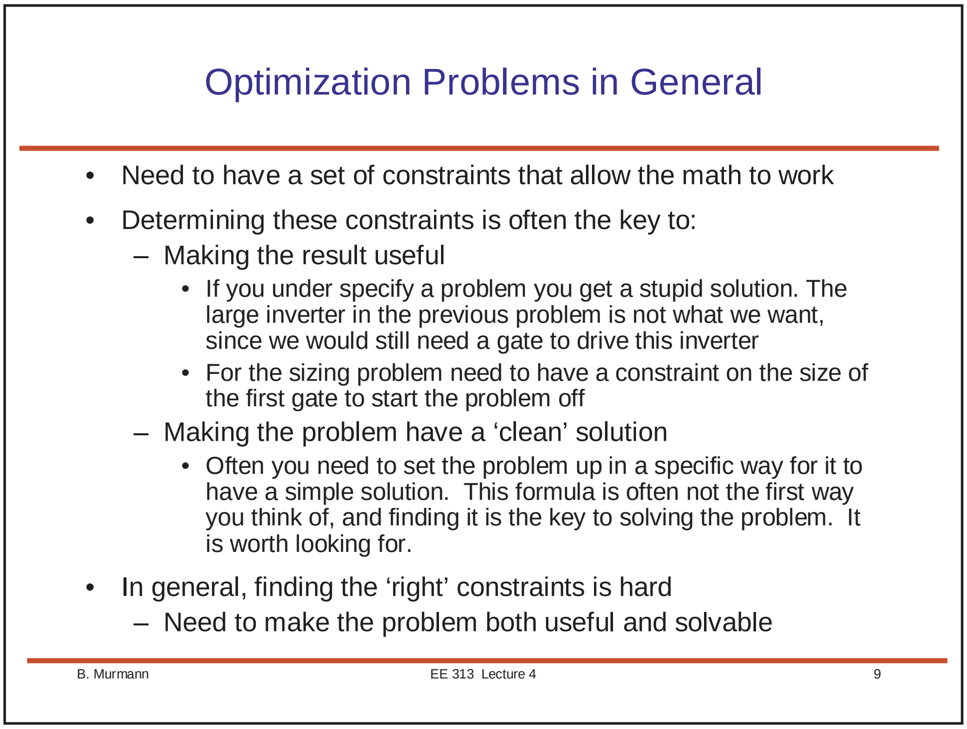
- Anyone want to guess the solution?

Careful about Optimization Problems

- Need to make sure you completely constrain them

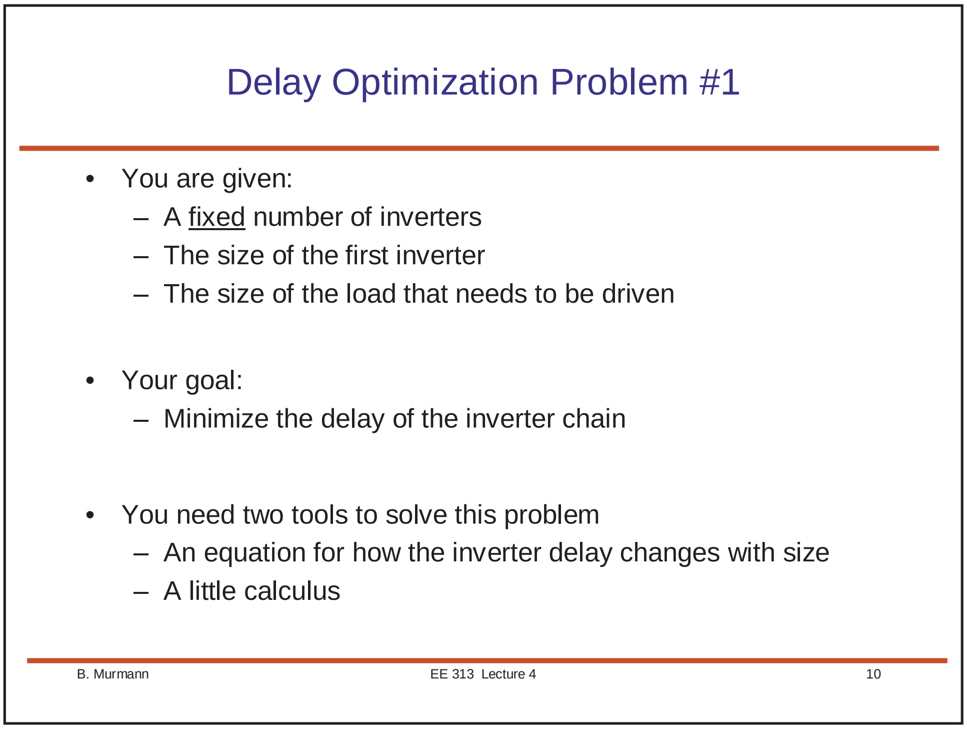


  - Fastest delay is to build one very big inverter
  - Make the inverter so large, the external load was small compared to internal parasitic capacitors. This would be the fastest gate, but it would have a large Cin
  - Probably not the real problem you are interested in



Optimization Problems in General

- Need to have a set of constraints that allow the math to work
- Determining these constraints is often the key to:
  - Making the result useful
    - If you under specify a problem you get a stupid solution. The large inverter in the previous problem is not what we want, since we would still need a gate to drive this inverter
    - For the sizing problem need to have a constraint on the size of the first gate to start the problem off
  - Making the problem have a ‘clean’ solution
    - Often you need to set the problem up in a specific way for it to have a simple solution. This formula is often not the first way you think of, and finding it is the key to solving the problem. It is worth looking for.
- In general, finding the ‘right’ constraints is hard
  - Need to make the problem both useful and solvable

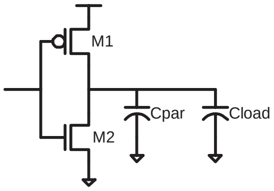


Delay Optimization Problem #1

- You are given:
  - A fixed number of inverters
  - The size of the first inverter
  - The size of the load that needs to be driven
- Your goal:
  - Minimize the delay of the inverter chain
- You need two tools to solve this problem
  - An equation for how the inverter delay changes with size
  - A little calculus

Inverter Delay Model

- Use RC model for gate delay
- Assume gate is sized for roughly equal rise and fall delays ($W_{M1} = 2W_{M2}$)
- Design parameter: $W=W_{M1}$
- Input capacitance: Cin=3·W·Cg' (1)
- Parasitic load: Cpar=γ·Cin (2)
- Resistance: Rdrive=Rsq/(W/L) (3)
- Delay= Rdrive · (Cload+Cpar) (4)
- Substitute: (3)->(4), and use (1) and (2):



$$\therefore Delay = 3R_{sq}LC_g\left(\frac{C_{load}}{C_{in}} + \gamma\right)$$

A Little Math

- Total delay is the sum of the delays of all the inverters
  - Calling $\tau_{inv} := 3 \cdot R_{sq} \cdot L \cdot C_g$
  - Total delay = $\sum_{j=1}^{N} \tau_{inv} \cdot \left(\frac{Cin_{j+1}}{Cin_j} + \gamma\right)$
  - Where Cin_{N+1} is defined to be Cload
- The size "C_{in}" of the jth inverter affects two terms in the delay equation
  - The delay of inverter j-1 (sets its load)
  - The delay of inverter j (sets its strength)

Finding the Optimal Size

- Change in delay with respect to any C_{in} should be zero

$$\frac{d}{dC_{in_j}}\text{Delay} = \tau_{inv}\cdot\left(\frac{1}{C_{in_{j-1}}}\right) - \tau_{inv}\cdot\left[\frac{C_{in_{j+1}}}{\left(C_{in_j}\right)^2}\right]$$

- Set this derivative equal to zero to get: $C_j=\text{sqrt}(C_{j+1} * C_{j-1})$
- Remember C_{in} proportional to W, so this result holds for W_j as well
- In the optimal case, W_j is therefore the geometric mean of W_{j-1} and W_{j+1}
- Optimum for a chain of N inverters
  - All inverters have the same fan-out
  - Fan-out per stage = $(\text{Cload}/\text{Cin})^{1/N}$

Delay Optimization Problem #2

- You are given:
  - The size of the first inverter
  - The size of the load that needs to be driven
- Your goal:
  - Minimize the delay of the inverter chain by
    - Finding the optimal number of gates
    - The sizes of the gates
- For a chain of length N, the fanout of each gate in the chain must match.Thus we want to find N that minimizes the following equation:

$$\text{Delay}= N\cdot\tau_{inv}\cdot\left[\left(\frac{C_{load}}{C_{in}}\right)^{\frac{1}{N}} + \gamma\right]$$

Number of Gates

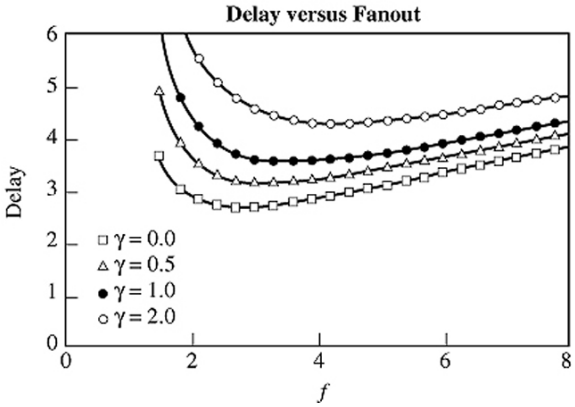
- Can rewrite in terms of fan-out, f

$$\frac{C_{load}}{C_{in}} = f^N \text{ solve}, N \rightarrow \frac{\ln\left(\frac{C_{load}}{C_{in}}\right)}{\ln(f)}$$

- Total chain delay is $\frac{\ln\left(\frac{C_{load}}{C_{in}}\right)}{\ln(f)} \cdot \tau_{inv} \cdot (f + \gamma)$

- Can plot this delay as a function of f
  - Factor out ln(Cout/Cin) and τ_{inv}, since both are not a function of the fanout or the number of stages

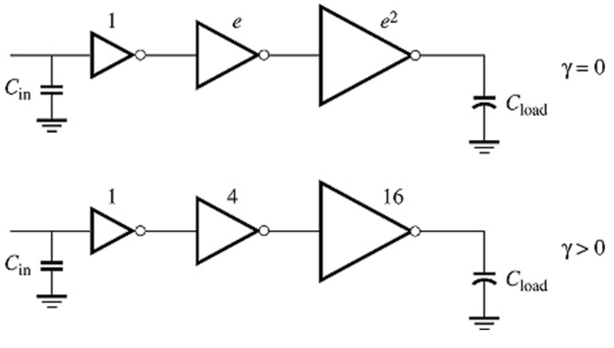
Plot of Total Delay



[Hodges, p.281]

- Total delay vs. fanout for different values of γ
  - Curves are very flat for f>2

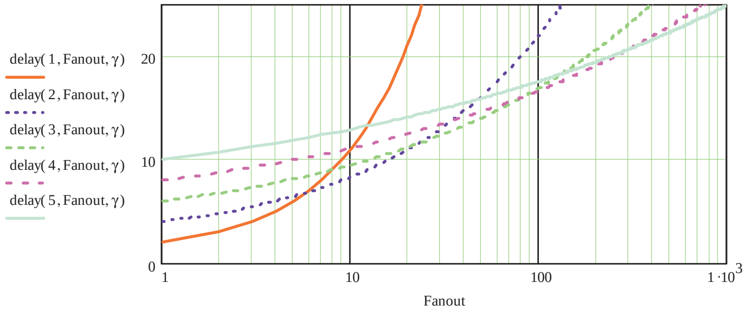
Inverter Sizing for Optimal Delay



- "Academic" result for γ=0: Size by e
- In practice: Size by 3...4
- Popular metric: FO4 delay, delay of an inverter with a fan-out of 4

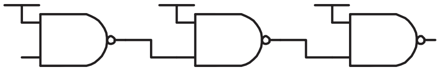
Another View: How Many Inverters?

$$\text{delay}(N, \text{Fanout}, \gamma) := N \cdot \left(\text{Fanout}^{\frac{1}{N}} + \gamma\right) \qquad \text{Fanout} := 1, 2 .. 1000 \qquad \gamma := 1$$



- Plots delay of different length inverter chain vs. total fanout of the chain. Breaks come at around 6, 22, 75, 240

Delay Optimization Problem #3



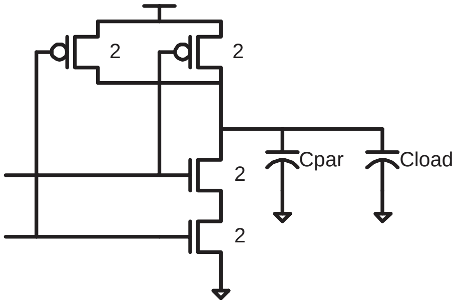
- Your goal:
  - Minimize the delay of a chain of NAND gates by
    - Finding the optimal number of gates
    - The sizes of the gates
- You are given:
  - The size of the first NAND gate
  - The size of the load that needs to be driven

NAND Delay Model

- Carry out same analysis as for inverter to get:

$$Delay = \tau_{NAND}\left(\frac{C_{load}}{C_{in}} + \gamma\right)$$

$$\tau_{NAND} = 4R_{sq}LC_g$$

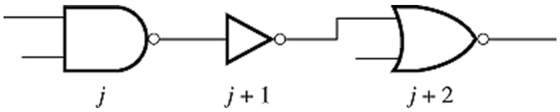


Delay for NAND Gates

- Can work out the delay for a string of gates
  - – Formula looks the same as the formula for inverters
  - – All that is different is the time constant for the gate
  - – Optimization will yield the same results
    - Equalize the delay of each stage
    - Optimal fan-out will be around 4
- But this is the wrong problem to solve!!!
  - – (That is the reason the answer is so boring)
  - – It assumed that we only had NAND gates
  - – Really have inverters too, and we could use them (as a buffer) to drive the large load. We don’t need to use only NAND gates. Always use the fastest gate as a buffer.

Delay Optimization Problem #4

- Your goal:
  - – Minimize the delay of a chain of <u>different kinds</u> of gates by:
    - Adding the optimal number of inverters
    - Sizing the transistors in each of the gates
- You are given:
  - – The size of the first gate
  - – The size of the load that needs to be driven



- What is new:
  - – The τ and the γ for each gate are no-longer the same

Delay Optimization

- Delay through first two stages:

$$\tau_{\mathrm{NAND}}\cdot\left(\frac{C_{in_{j+1}}}{C_{in_j}}+\gamma_{\mathrm{NAND}}\right)+\tau_{\mathrm{inv}}\cdot\left(\frac{C_{in_{j+2}}}{C_{in_{j+1}}}+\gamma_{\mathrm{inv}}\right)$$

- With same analysis as in the inverter case, we obtain for minimum value of this delay component:

$$\tau_{\mathrm{NAND}}\cdot\frac{C_{in_{j+1}}}{C_{in_j}}=\tau_{\mathrm{inv}}\cdot\left(\frac{C_{in_{j+2}}}{C_{in_{j+1}}}\right)$$

- This result holds in general, $\tau\cdot f$ of a given gate should be made equal to $\tau\cdot f$ of the next gate:

$$\tau_k\cdot f_k=\tau_{k+1}\cdot f_{k+1}$$

Result

- Same basic rule as in the inverter case
  - Need to match the "fan-out part" of the delay
  - But fan-out of each gate is no longer the same
- More convenient formalism for "back of the envelope" optimization: "Logical Effort"
- Normalize everything with respect to τ_{inv}
- More next lecture...