19.5   A Clock Skew Absorbing Flip-Flop

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A new Skew Tolerant Flip-Flop (STFF) that achieves the lowest reported delay and energy-delay product while absorbing up to 54ps of clock skew is described. In addition, a method for characterizing clock skew absorbing flip-flops is presented. This comparison is apples-to-apples because the best previously reported flip-flops [1-4] are fabricated on the same wafer and measured using a common test setup.

Other methods used to absorb clock skew incur large synchronization overhead (multi-phase latch-based design), require generation and distribution of overlapped multiple clock phases, and/or reduce design flexibility and complicate testing. To achieve high clock skew absorption while maintaining high speed and design simplicity, STFFs have a soft clock edge property [5], making them transparent during a short time interval after the clock edge. In addition, the soft clock edge allows some time borrowing between adjacent pipeline stages which can be traded for skew absorption.

Clock skew is modeled as a window around the nominal arrival time where the actual clock transition may occur causing a fluctuation of data to clock delay. This modifies data to output delay (t_{DQ}), [6] as seen in Fig. 19.5.1. The delay of a flip-flop in the presence of clock skew is the maximum t_{DQ} corresponding to the worst possible clock arrival time. If this delay increase is smaller than the initial clock arrival variation, the flip-flop absorbs clock skew. The clock skew absorption is the portion not reflected in increased t_{DQ}, (Fig. 19.5.1). The highest clock skew absorption (100%) is obtained if the data to output characteristic is flat in a region of expected clock arrival. Clock skew is defined as absorbed if the absorption is 80% or higher.

The proposed differential Skew Tolerant Flip-Flop (STFF-D), displayed in Fig. 19.5.2, consists of two stages. Stage one generates a pulse at node $S/\bar{S}$ (Set) or $R/\bar{R}$ (Reset) after the falling edge of Clk. Stage two is a set-reset latch that captures the pulses $S/\bar{S}$ or $R/\bar{R}$. When Clk is high, nodes C_S and C_R are low. Nodes $\bar{S}$ and $\bar{R}$ are high and I3, I4, M10, M12, M14 and M16 maintain the values of outputs Q and $\bar{Q}$. When Clk switches low, signals C_S and C_R are driven high, enabling evaluation of nodes $\bar{S}$ and $\bar{R}$. If D=1 (D=0), node $\bar{S}$ ($\bar{R}$) switches low and node S (R) high, which forces C_R (C_S) back to low. This disables subsequent switching of node $\bar{R}$ ($\bar{S}$) and ensures that node C_S (C_R) is driven high while Clk=0. The pulses at either $\bar{S}$/S or $\bar{R}$/R simultaneously pull Q/$\bar{Q}$ to D/$\bar{D}$. During the time when Clk=0, the low level of node $\bar{S}$ ($\bar{R}$) is maintained by transistor M1 and M3 (M5 and M7).

The Single-ended Skew Tolerant Flip-Flop (STFF-SE), shown in Fig. 19.5.3, also consists of two stages. Stage one conditionally generates a pulse at node $\bar{S}$ (Set), which is captured by the clocked half-latch (N1, N2) in stage two. When Clk=1, node C_S is low, node $\bar{S}$ is precharged high and N1 and N2 maintain the levels of the outputs Q and $\bar{Q}$. When Clk goes low, node C_S switches high, forcing node $\bar{S}$ low if D=1. This low level at node $\bar{S}$ keeps node C_S high while Clk=0, and drives outputs Q and $\bar{Q}$ to logic one and zero, respectively. If D=0 until node CKD switches high, node C_S switches low and $\bar{S}$ remains high. This drives Q to logic zero and $\bar{Q}$ to logic one. During the time when Clk=0, the level of node $\bar{S}$ is maintained by transistors M7, M9, and M10.

For either version of the flip-flop, if the data arrives while C_S and C_R are high, the transition of node $\bar{S}$ or $\bar{R}$ depends only on the data arrival time. In addition, the feedback applied in the first stage of STFF-SE drives C_S high if $\bar{S}$ switches low, even when the transparency window elapses [1]. These features allow negative setup time and widen the region for which the data to output characteristic is flat. Finally, STFF exhibits small delay due to the short critical path from D/$\bar{D}$ to Q/$\bar{Q}$. The effective delay may be further reduced by embedding an arbitrary logic function into the first stage.

STFF-SE and STFF-D are compared to the Semi-Dynamic Flip-Flop (SDFF) [1], the improved Sense Amplifier Flip-Flop (im-SAFF) [2,3], and a conventional Master-Slave latch [4]. All compared flip-flops are optimized for minimum Energy-Delay Product (EDP) at 25% data activity and fabricated in a 0.11μm 1.2V CMOS process [7]. The flip-flops are driven by FO4 inverters and loaded with 14 minimum inverters (18.9fF). Built-in test circuitry capable of measuring the delay $t_{Clk-Q}=f(t_{D-Clk})$ with 1σ uncertainty of 15ps is developed. Power consumption is measured by isolating the power supply for a bank of flip-flops.

The measured timing characteristics are shown in Fig. 19.5.4. STFF-SE and STFF-D have a wide region where the data to output characteristic is flat. Figure 19.5.5 shows the delay versus clock skew. The data to output delay of STFF-D is smallest when the clock skew is zero and absorbed skew is 33ps; absorbed skew of STFF-SE is 54ps. Overall measured characteristics of the flip-flops are shown in Fig. 19.5.6. In terms of the clocking overhead, a skew-absorbing flip-flop is equivalent to a conventional flip-flop with delay reduced for the amount of absorbed skew. The equivalent delay of STFF-D is 39ps and of STFF-SE is 30ps. Due to the skew absorption, STFFs have the largest hold times and may increase the padding needed to meet the fast path requirements. Introducing circuitry to enable clock skew absorption has no significant impact on power and area. Delay and EDP comparison indicates that STFF offers the best energy-delay trade-off even when clock skew is not taken into account.

References
[1] F. Klass, "Semi-Dynamic and Dynamic Flip-Flops with Embedded Logic," *Symposium on VLSI Circuits, Digest of Technical Papers*, p.108-109, 1998.
[2] B. Nikolic, V. G. Oklobdzija, "Design and Optimization of Sense Amplifier-Based Flip-Flops," *25th ESSCIRC,* pp. 410-413, 1999.
[3] V. Stojanovic, V. G. Oklobdzija, "Flip-Flop," US Patent No. 6,232,810, May 2001.
[4] G. Gerosa et al, "A 2.2W, 80MHz Superscalar RISC Microprocessor," *IEEE J. Solid State Circuits*, vol. 29, pp. 1440-1452, Dec. 1994.
[5] H. Partovi et al, "Flow-Through Latch and Edge-Triggered Flip-Flop Hybrid Elements," *ISSCC Digest of Technical Papers,* pp. 138-139, 1996.
[6] V. Stojanovic, V. G. Oklobdzija, "Comparative Analysis of Master-Slave Latches and Flip-Flops for High-Performance and Low-Power Systems," *IEEE J. Solid State Circuits*, vol.34, no.4, p.536-548, 1999.
[7] Y. Takao et al, "A 0.11um CMOS Technology with Copper and Very-low-k Interconnects for High-Performance System-On-a-Chip Cores," *IEDM Technical Digest,* p.559-562, 2000.
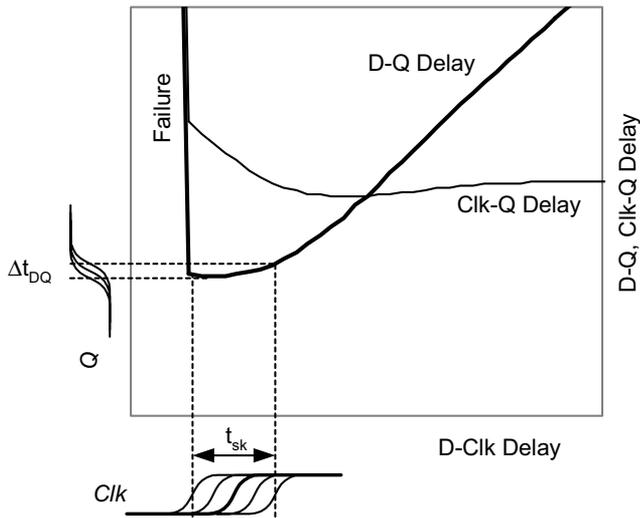
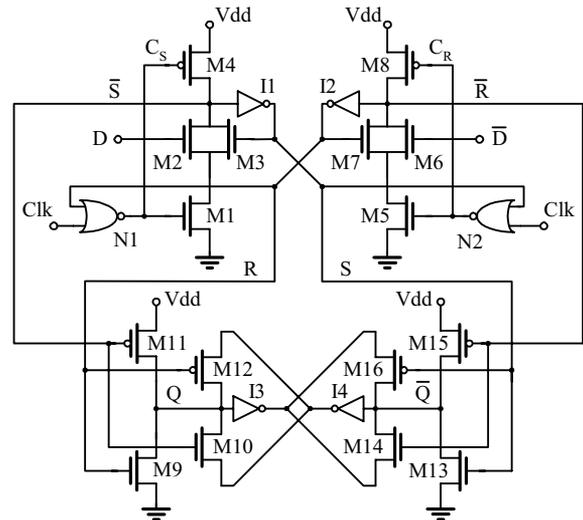Figure 19.5.1: Skew absorption model.

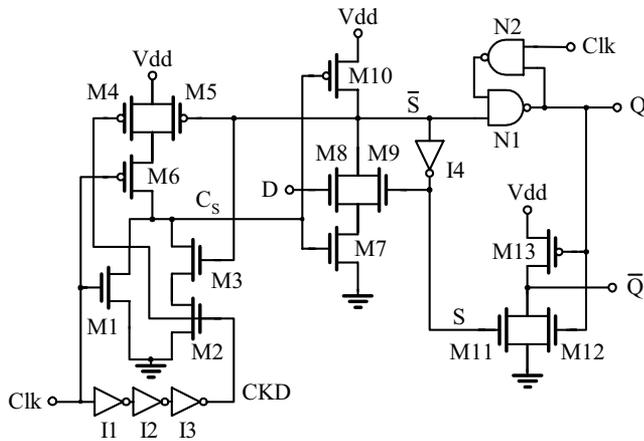Figure 19.5.2: Differential Skew Tolerant Flip-Flop (STFF-D).

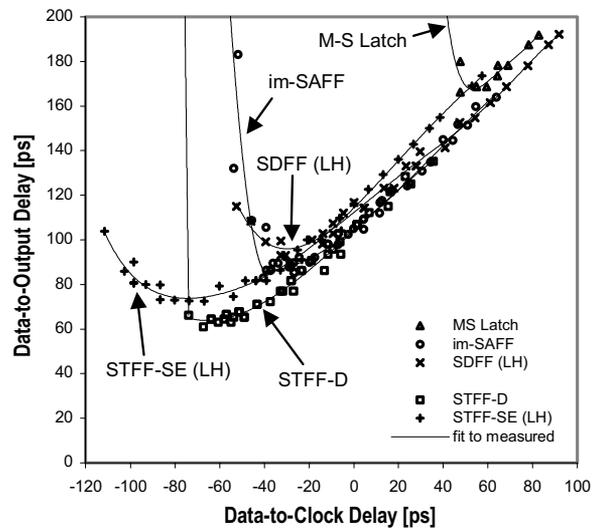Figure 19.5.3: Single-Ended Skew Tolerant Flip-Flop (STFF-SE).

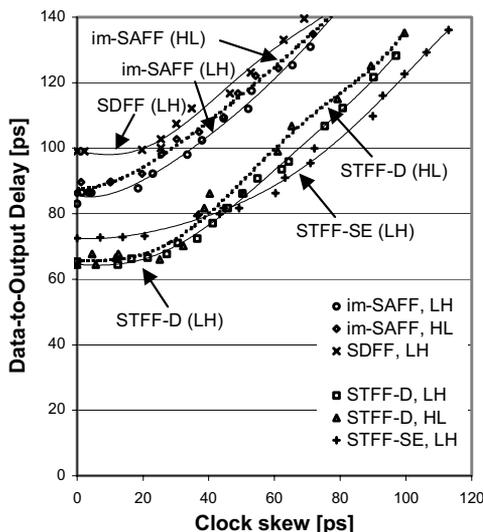
Figure 19.5.4: Data to output delay comparison.

Figure 19.5.5: Data to output delay vs. clock skew.

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	MS Latch	SDFF	im-SAFF	STFF-SE	STFF-D
Setup Time [ps]	55	-30	-37	-70	-54
Hold Time [ps]	23	82	80	120	110
Clk-Q delay @ $t_{SU} \to \infty$ [ps][1]	113	105	105	125	120
D-Q delay [ps][1]	168	99	87	73	65
Power [μW], 25% activity[2] @257MHz	10.6	20.2	15.8	17.3	17.9
EDP [x10^{-24}Js] @257MHz	55.2	62.4	44.8	42.1	37.9
Minimum padding (Hold – (Clk-Q)$_{min}$) [ps]	-47.4	14	-11	17	5
Sampling window [ps][3]	78	42	41	40	46
Input load (D) [min. inv]	8.7	3.7	2 X 2	2.3	2 X 2.1
Input load (Clk) [min. inv]	6.9	8.4	3.4	4.7	3.1
Absorbed skew [ps]	N/A	30	20	54	33
Equivalent delay [ps]	168	75	71	30	39
Size [μm^2]	46.08	57.6	53.76	53.76	59.52

[1] average delay difference between measurement and simulation 3% (max. 15%)
[2] average power difference between measurement and simulation 16% (max. 21%)
[3] Sampling window is the period of time when data must be stable

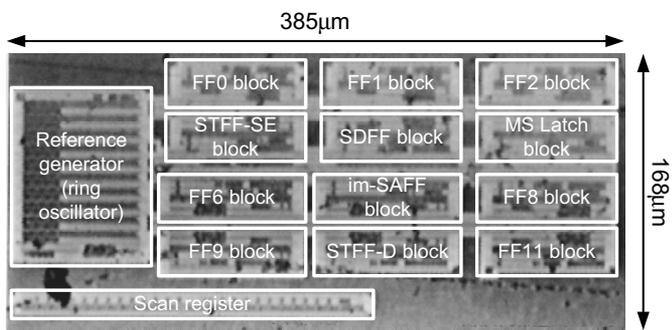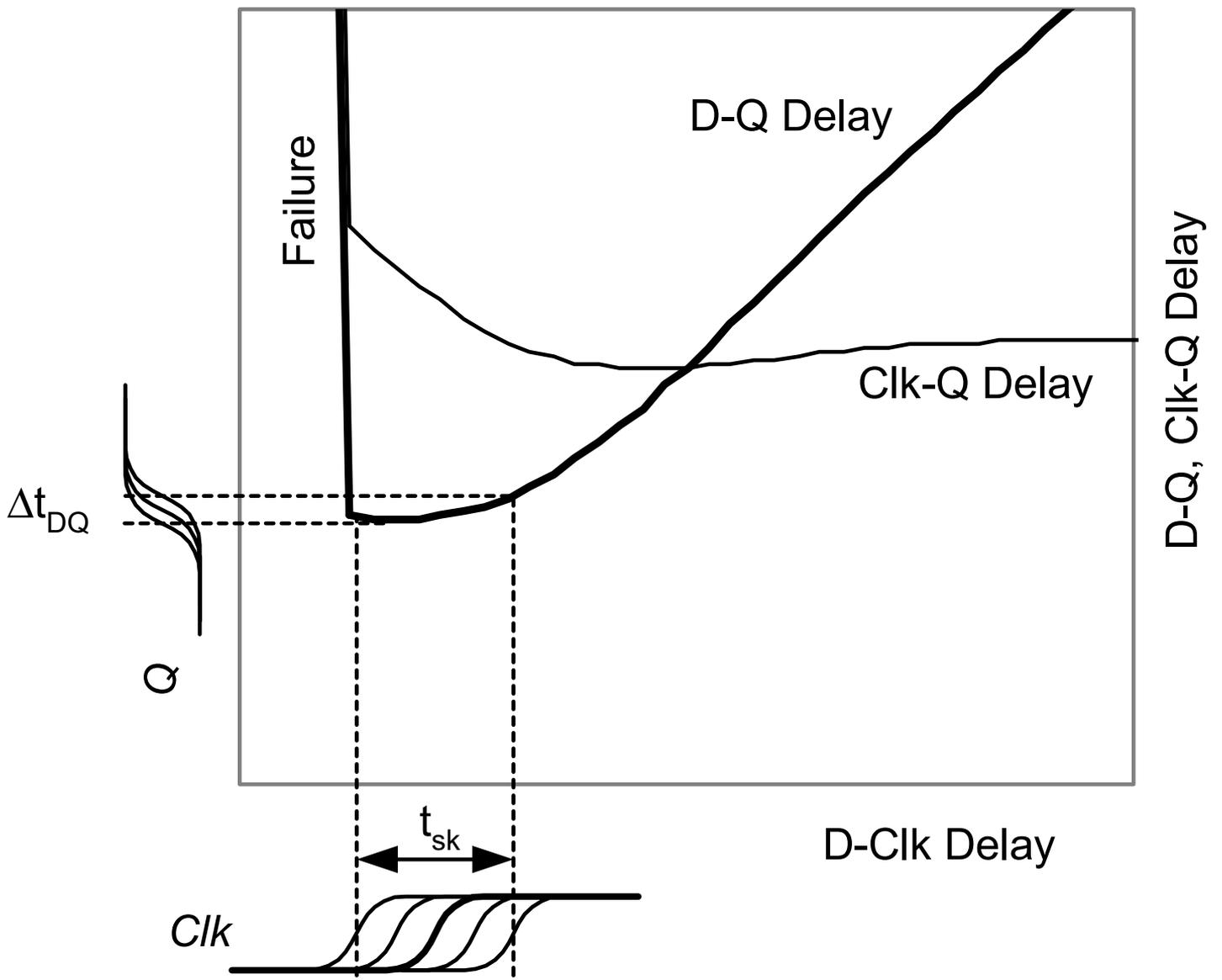Figure 19.5.6: Measured characteristics of flip-flops.

385μm

168μm

FF0 block | FF1 block | FF2 block

STFF-SE block | SDFF block | MS Latch block

FF6 block | im-SAFF block | FF8 block

FF9 block | STFF-D block | FF11 block

Reference generator (ring oscillator)

Scan register

Figure 19.5.7: Micrograph of delay measurement circuit.

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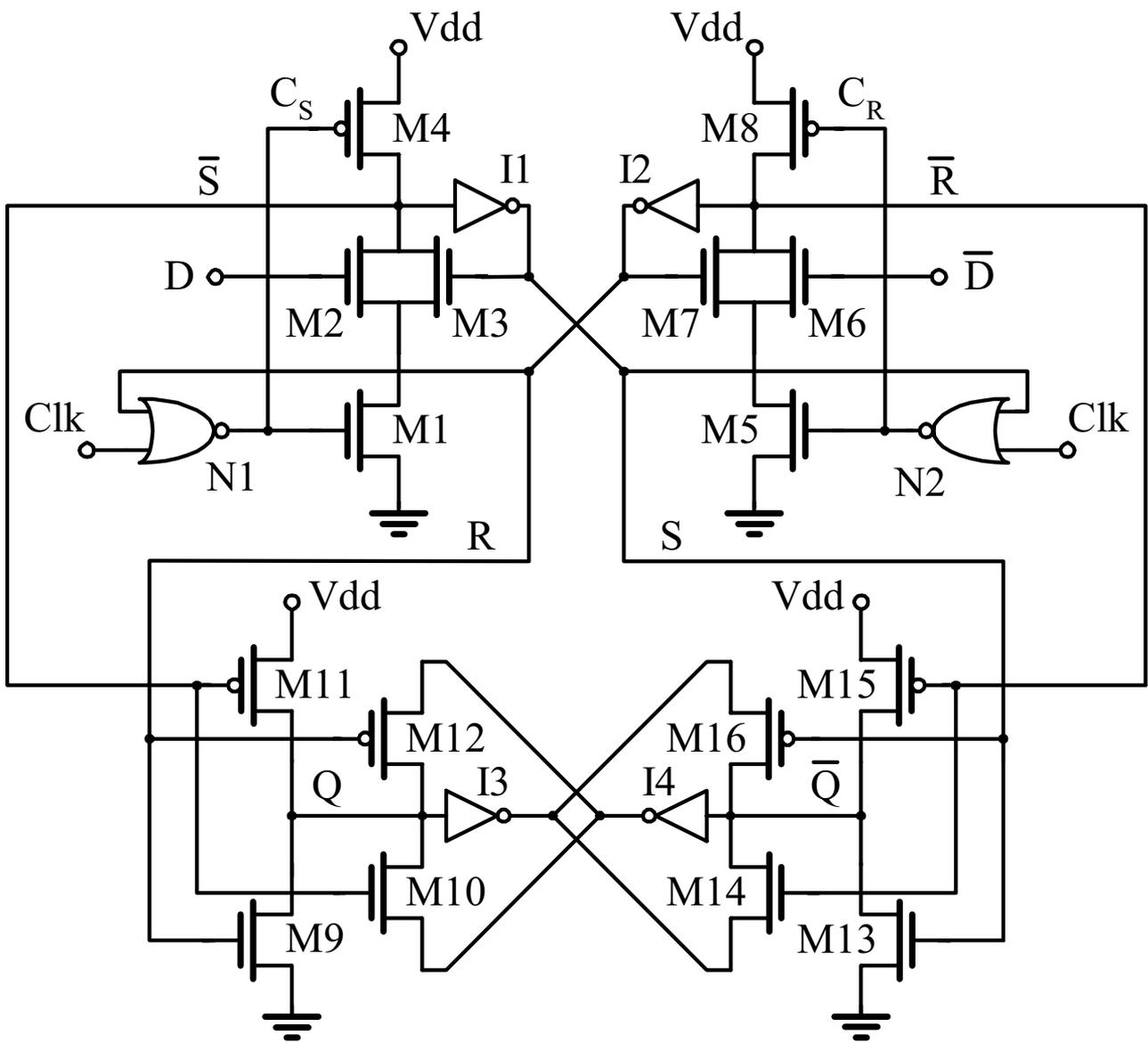
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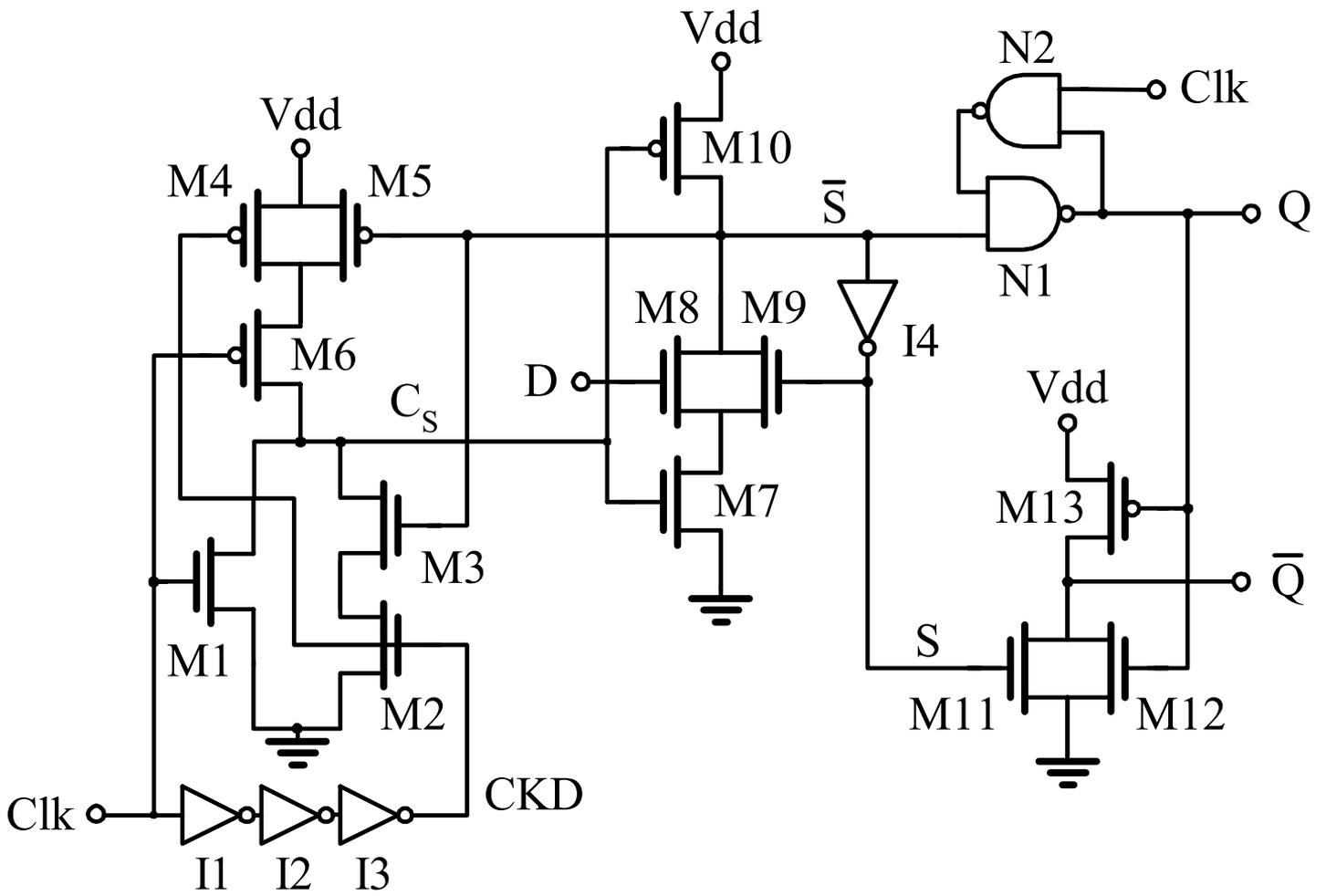
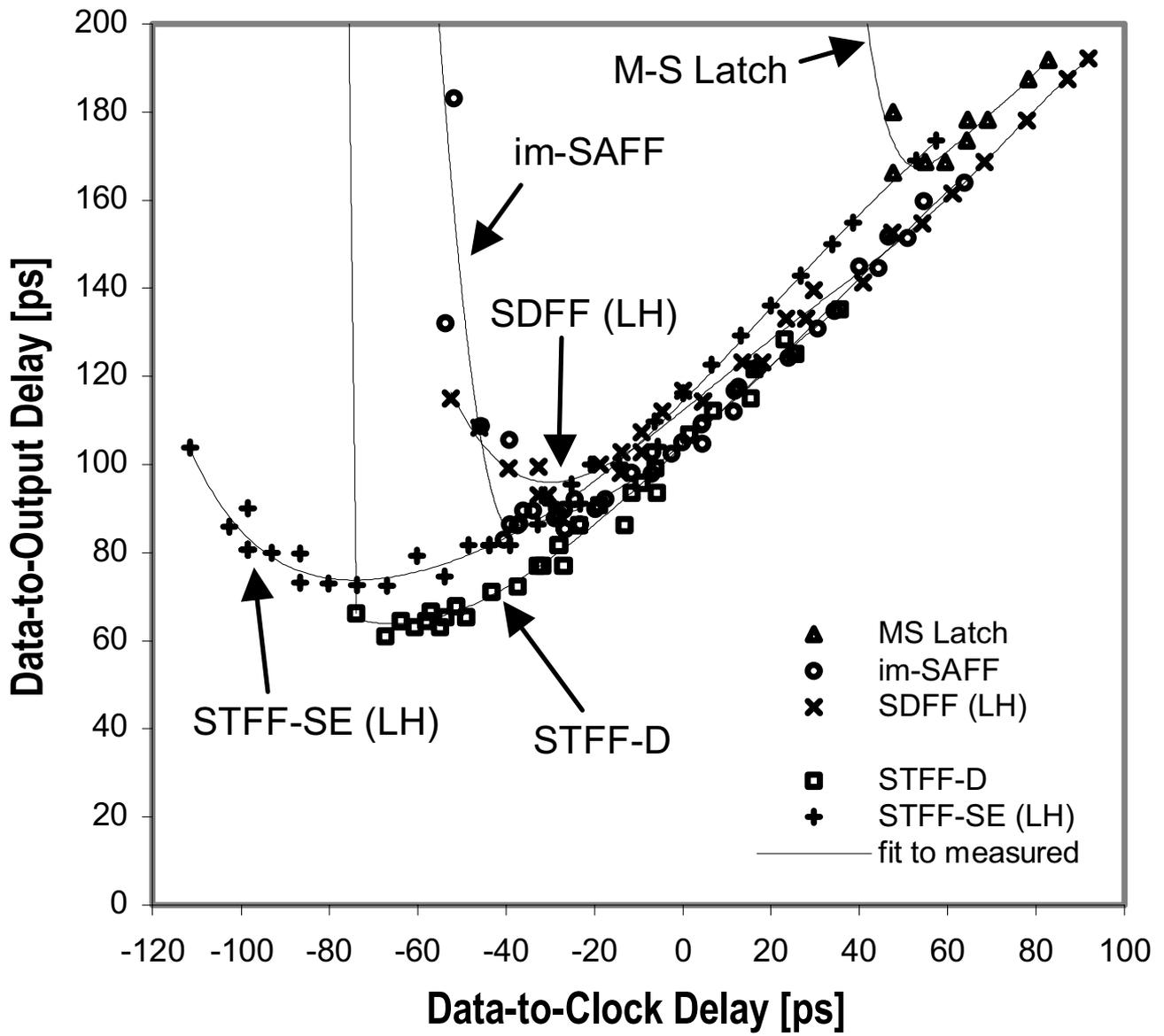**Figure 19.5.3: Single-Ended Skew Tolerant Flip-Flop (STFF-SE).**

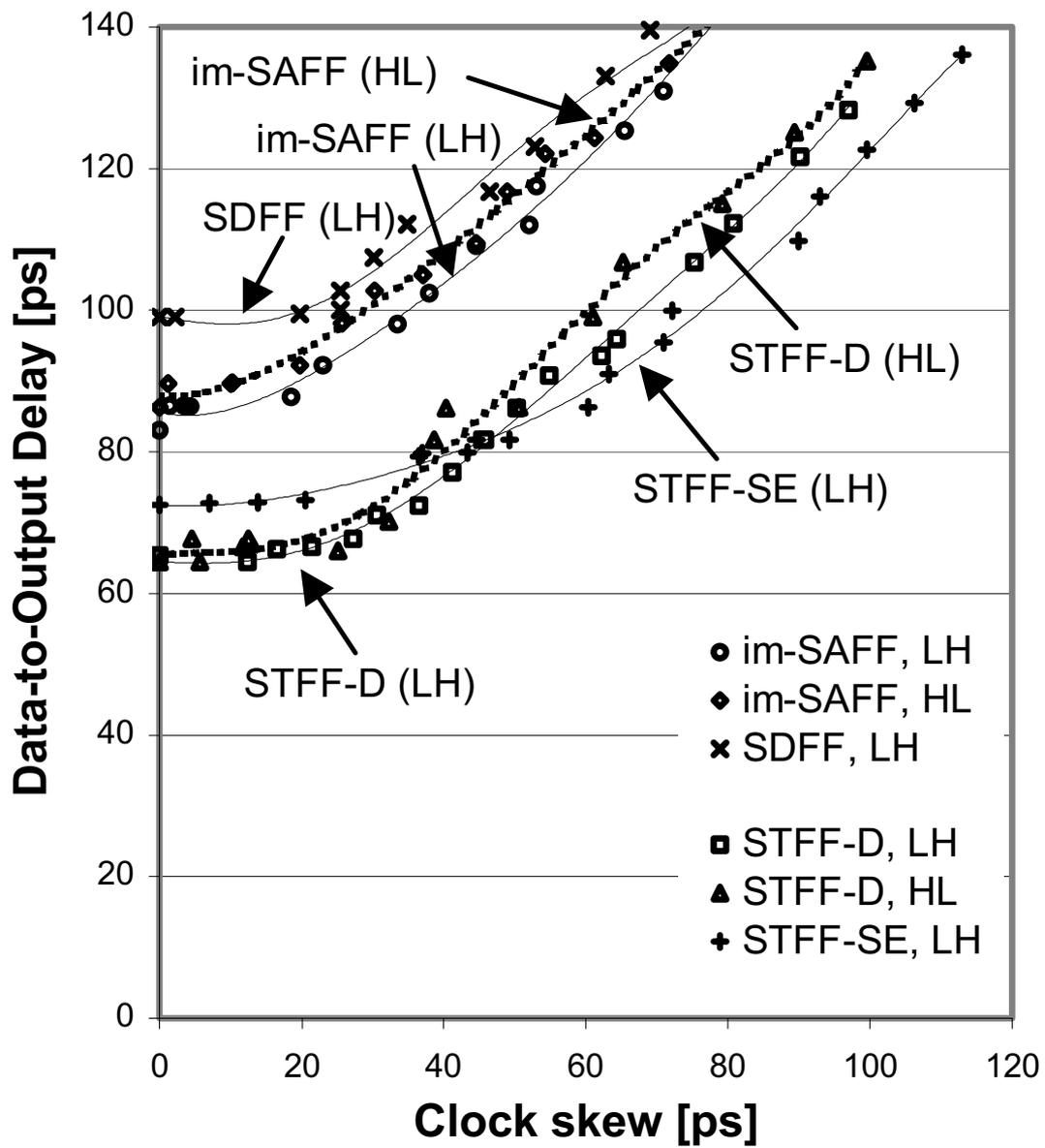Figure 19.5.4: Data to output delay comparison.

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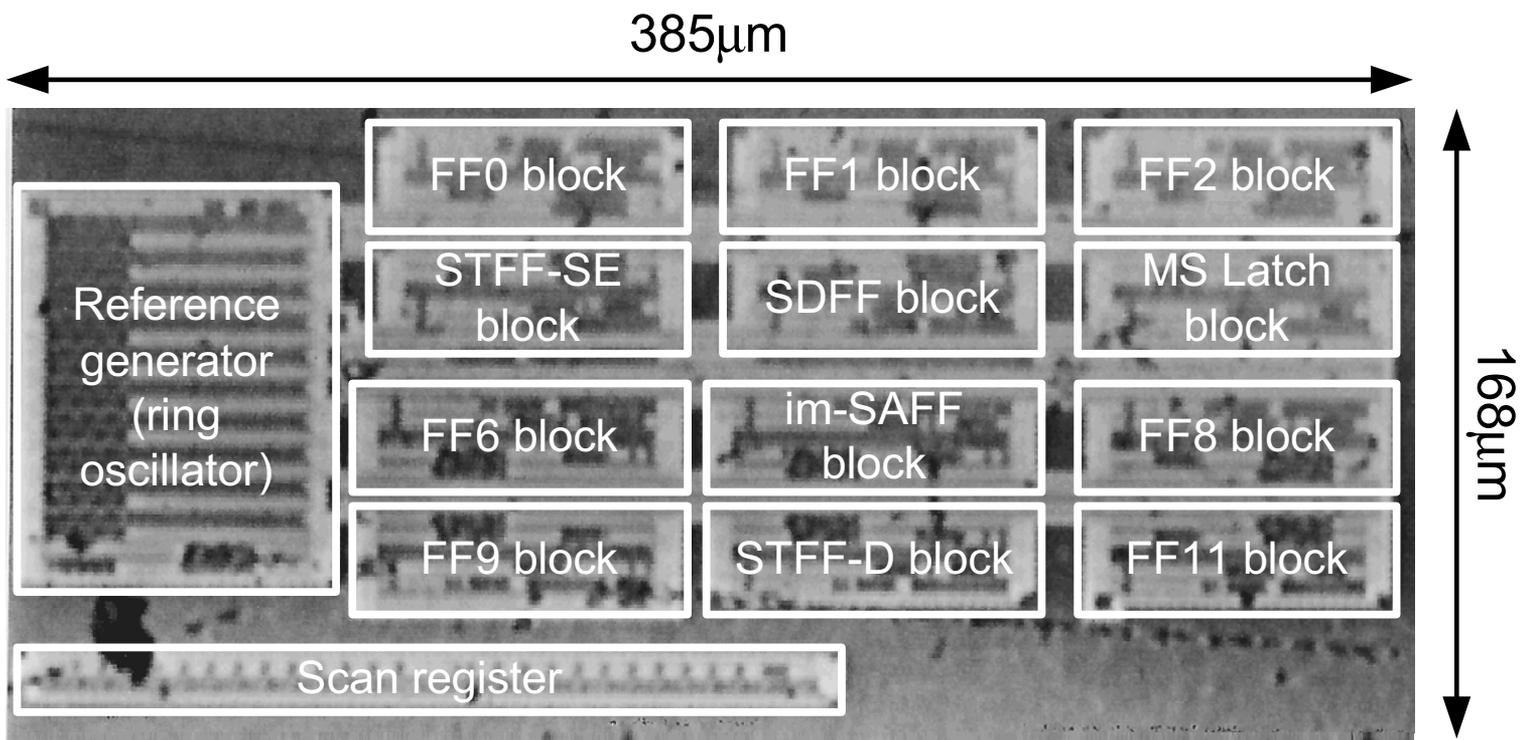im-SAFF block

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