Differential Split-Level CMOS Logic for Subnanosecond Speeds

LEO C. M. G. PFENNINGS, WIM G. J. MOL, JOSEPH J. J. BASTIAENS, AND JAN M. F. VAN DIJK

Abstract —Subnanosecond gate delays (0.8 n) have been measured on complex logic gates (e.g., sum functions of a full adder) designed in the differential split-level (DSL) CMOS circuit technique. This high speed has been achieved by reducing the logic swing (2.4 V) on interconnect lines between logic gates, by using current controlled cascoded cross-coupled NMOS–PMOS loads, by using combined open NMOS drains as outputs, and by employing shorter channel lengths ($L_{eff} = 1 \mu m$) for the NMOS devices in the logic trees with reduced maximum drain–source voltages to avoid reliability problems. Extra ion implantation protects these transistors from punchthrough.

I. Introduction

THE GENERAL rule: "Enhancement Depletion NMOS is faster than CMOS" was a challenge to explore speed improvements in CMOS circuit techniques. Differential split-level (DSL) [1] CMOS logic makes a compromise between the static power dissipation of E/D NMOS and the dynamic power dissipation of CMOS.

This paper will describe the switching behavior and the speed improvements owing to the DSL circuit technique. This circuit technique shows similarity with differential cascode voltage switch logic (CVSL) [2] but the electrical behavior of the DSL circuit technique is essentially different.

The DSL circuit technique was implemented in a double-metal 2.5-μm CMOS n-well process with conventional 2.5-μm projection lithography, except for the polysilicon. In this mask only the gate length of the n-channel transistors in the logic trees is decreased to 1.5 μm ($L_{eff} = 1$ μm), while the other polysilicon details and pitches remain constant. Therefore a stepper exposure is used for the polysilicon definition. An extra deep boron implant protects the short-channel NMOS transistors from punchthrough.

DSL incorporates a reduced maximum drain–source voltage $V_{DS\,max}$ in the logic trees resulting in less hot-electron-induced degradation of these devices. Decreasing $V_{DS\,max}$ reduces the lateral electric field near the drain edge of these NMOS transistors [3], [4]. This allows the use of shorter channel lengths without lifetime reduction.

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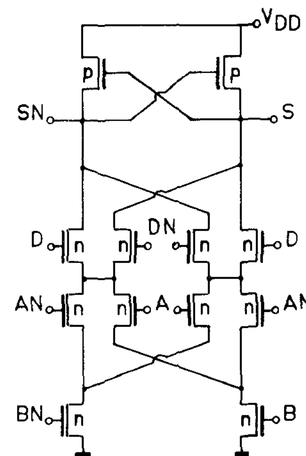

Fig. 1. Sum part of a differential CVSL full adder.

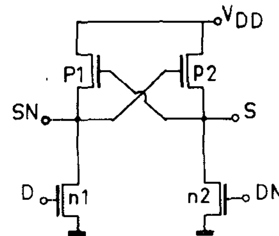

Fig. 2. Differential CVSL basic circuit.

II. Short Summary of CVSL

Fig. 1 shows the circuit diagram of the sum function of a full adder designed in differential cascode voltage switch logic. The cross-coupled PMOS loads and the differential logic NMOS trees are typical for this circuit technique. To explain the switching behavior of the CVSL circuit technique we replace the differential logic NMOS trees by two NMOS transistors as shown in Fig. 2.

Now suppose we switch input D from a low to a high level, starting with input D low and input DN high. Then node SN is at a high level of V_{DD} and node S at a low level of 0 V so PMOS $P1$ is on and $P2$ is off. If we now switch the inputs D and DN then NMOS $N1$ turns on and $N2$ turns off. This is ratioed logic because transistor $N1$ has to discharge node SN, while $P1$ is still on. $P1$ switches off, after $P2$ has switched on and node S has reached a high level. So during switching both $N1$ and $P1$ (or $N2$ and $P2$ depending on the input transition) conduct, causing relatively large current spikes and additional delay.

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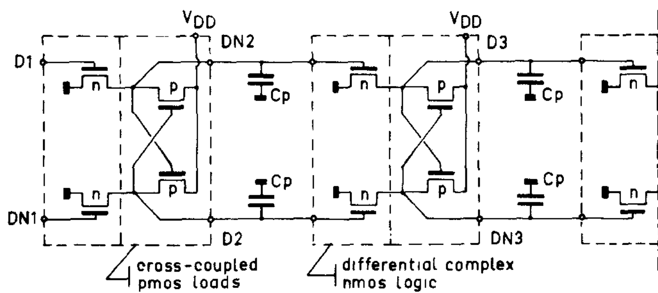

Fig. 3. Serial chain of differential CVSL circuits.

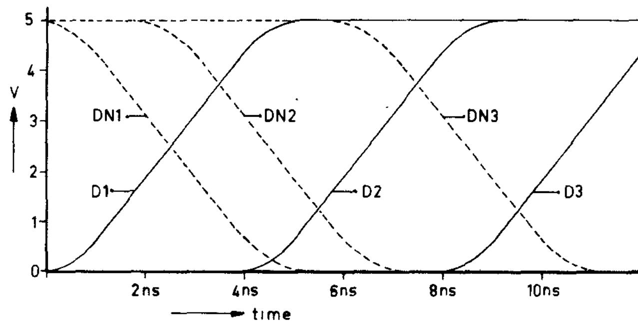

Fig. 4. Switching behavior of the differential CVSL serial chains.

Fig. 3 shows a part of a chain of differential CVSL circuits. The two NMOS transistors of the NMOS logic segments represent the CVS tree combinatorial logic network, i.e., full adder. The capacitances C_p represent the parasitic capacitance between the circuits.

Fig. 4 shows the switching behavior of this chain. It shows that although there is a simultaneous switching of the inputs *D*1 and *DN*1, there is a skew between the complementary output nodes *DN*2 and *D*2, and *DN*3 and *D*3, respectively.

III. Differential Split-Level (DSL) CMOS Logic

The DSL principle is shown in Fig. 5. Two extra NMOS transistors *N*10 and *N*20 are placed between the PMOS part and the logic NMOS part. Their gates are controlled by a reference voltage, which must be equal to half V_{DD} plus the threshold voltage of the NMOS transistors to guarantee optimum circuit operation (see below). The gates of the PMOS transistors *P*1 and *P*2 are now connected to *F* and *FN* instead of the outputs *S* and *SN*. Now we again switch input *D* from a low to a high-level starting with input *D* low and *DN* high. Then node *SN* has a high level of V_{DD} and node *S* has a low level. The reference voltage determines the high-level at node *FN* to be half V_{DD}. Node *F* has a low level of about 100 mV, because PMOS *P*2 is weakly on. This causes static power dissipation. The NMOS transistor *N*10 is cut off, which causes a high impedance to V_{DD} for node *FN* while there is a low impedance to V_{DD} for node *SN*. If we now switch the inputs *D* and *DN* then NMOS *N*1 turns on and *N*2 turns off.

The half V_{DD} level at node *FN* will immediately be discharged and PMOS *P*2 turns more on to its high drive state. At the same time nodes *S* and *F* start rising because PMOS *P*2 was already partly on, causing PMOS *P*1 to switch faster to its low drive state.

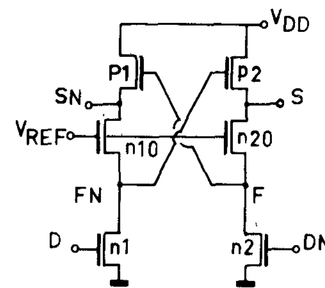

Fig. 5. Differential split-level circuit principle.

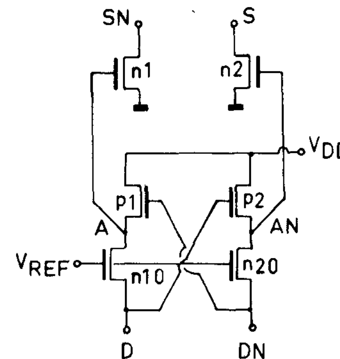

Fig. 6. DSL basic circuit.

Now let us consider ways to improve further the switching speed of this circuit technique. The maximum drain–source voltage of only half V_{DD} on nodes *FN* and *F* allows the channel length of the NMOS logic transistors to be reduced. Because of the low voltage swing on nodes *FN* and *F*, it is preferable to use these nodes as outputs and inputs of the gates, thereby reducing the delay due to wiring capacitance. This technique of separating gates is also used in some bipolar techniques.

Fig. 6 shows the reconfiguration of the DSL circuit. At the inputs *D* and *DN*, we now have current controlled cascoded cross-coupled NMOS–PMOS loads and the outputs *SN* and *S* are the open drains of the logic NMOS transistors. The internal gate signals *A* and *AN* of this figure correspond with the outputs *S* and *SN* of Fig 5.

Application of the differential split-level logic technique in a complete full adder is shown in Fig. 7. At the bottom of this circuit diagram we have three complementary input circuits consisting of cascoded cross-coupled NMOS–PMOS loads. The interconnections between nodes *D*, *DN*, *A*, *AN* and *B*, *BN* of the input circuits and the gates of the logic NMOS trees are not drawn in this diagram.

Fig. 8 shows simulation results for the full adder of Fig. 7. Shown are the inputs *AI* and *ANI*, the internal gate signals *A* and *AN*, and the open drain outputs *S* and *SN*. The inputs and outputs, respectively, are driven and loaded by other full adders. The effective gate lengths of the p-channel transistors are 2.1 μm and of the n-channel transistors 2 μm for the reference transistors and 1 μm for the logic transistors. The delay between *ANI*, *AI* and *SN*,

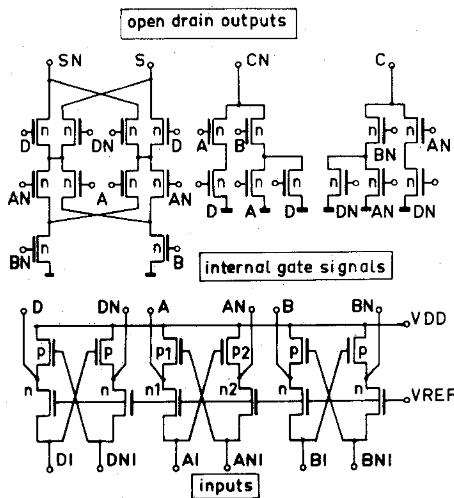

Fig. 7. Complete full adder in DSL.

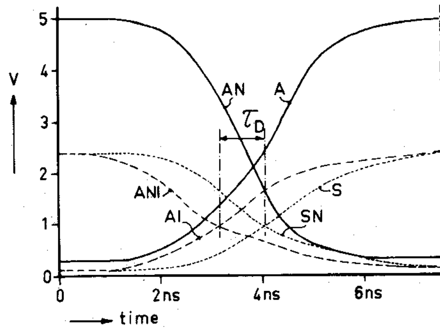

Fig. 8. Timing diagram of a DSL full adder.

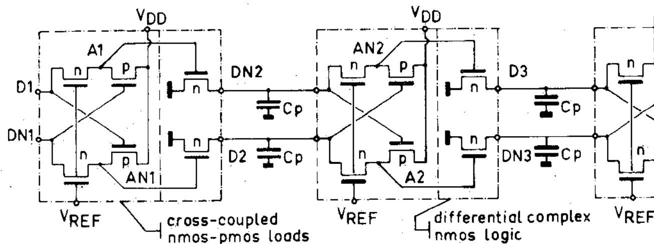

Fig. 9. Serial chain of DSL circuits.

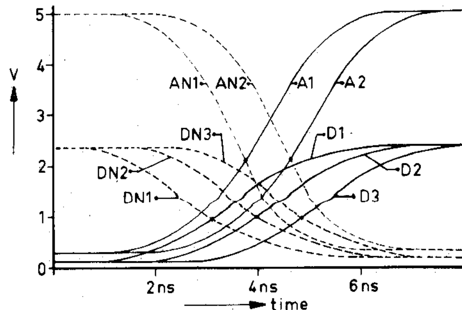

Fig. 10. Switching behavior of the DSL serial chain.

S equals 0.8 ns. It can be seen that complementary signals switch simultaneously.

Fig. 9 shows a part of a DSL CMOS gate chain. The two NMOS transistors of the NMOS logic segments represent the combinatorial logic network, i.e., full adder of Fig. 7. Simulation results of this chain are shown in Fig. 10.

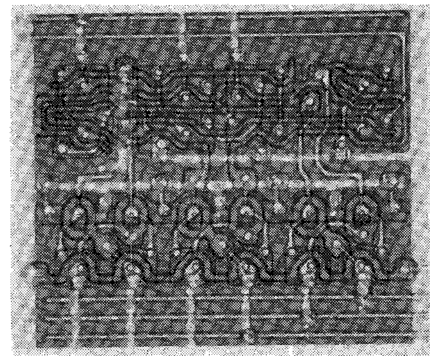

Fig. 11. Photomicrograph of a DSL full adder.

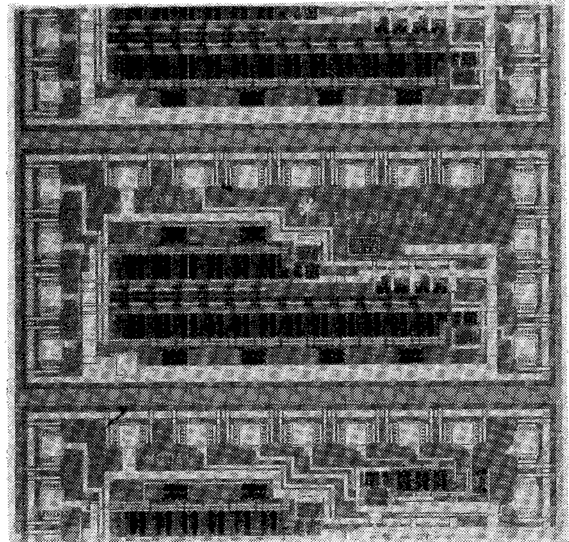

Fig. 12. Photomicrograph of a two-chain test structure.

$D1$, $DN1$, $D2$, $DN2$ and $D3$, $DN3$ are the low-voltage-swing output and input node signals. $A1$, $AN1$ and $A2$, $AN2$ are the internal gate signals with a full V_{DD} swing.

IV. Experimental and Simulation Results

Fig. 11 shows a photomicrograph of a full adder. The lower part of the layout shows the three complementary input circuits with the NMOS reference transistors and the PMOS cross-coupled loads. The upper part shows the NMOS logic trees. The size of the full adder is 142 μm $\times$ 90 μm. The full adder is processed in a 2.5-μm double-metal n-well CMOS process.

Two full adder chains have been implemented on the testchip shown in Fig. 12. This test chip consists of one chain of six and one of twelve full adders in series. Both chains have the same input and output buffer. Since the delay of a full adder is not the same for every input, six of these two-chain test structures have been implemented on a chip to measure the various delays. A differential measurement between the outputs of a two-chain test structure gives the total delay of six full adders.

Fig. 13 shows an oscillogram of this measurement for the sum delay. The output signals are measured with probes with an attenuation factor of 10; the horizontal scale is 5

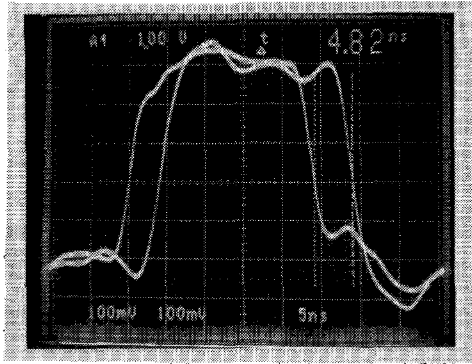
Fig. 13. Sum delay of six full adders.

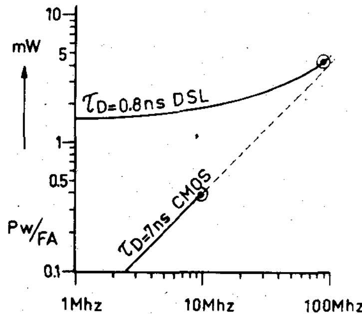

Fig. 14. Power as a function of frequency for DSL and CMOS.

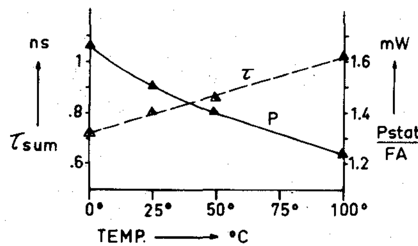

Fig. 15. Sum delay and static power as a function of the temperature.

ns/div. A difference of 4.8 ns between the outputs of the two chains was measured on the test structure, where the S and SN nodes are connected to the AI and ANI inputs, see Fig. 7. So a propagation delay of 0.8 ns for the sum function of a full adder is obtained. The static power dissipation was 1.5 mW for each full adder at 5 V V_{DD}. Similar test chains have been implemented with conventional static CMOS circuitry.

Fig. 14 shows the simulation results of a comparison of the power dissipation as a function of the frequency for conventional static CMOS and DSL fabricated in the same CMOS process. The power dissipation per full adder is plotted in milliwatts versus the frequency in megahertz. The dots indicate the maximum oscillation frequency of a seven-stage full adder ring oscillator, with both the sum and the carry switching. These maximum operating frequencies are 10 and 89 MHz, respectively, for conventional CMOS and for DSL CMOS. The propagation delay of the DSL full adder is about one tenth that of the conventional CMOS full adder, 0.8–7 ns. The simulated results shown in this graph are in agreement with the measured values. The dynamic power dissipation of the conventional CMOS full adder is 40 μW/MHz while for the DSL full adder 30

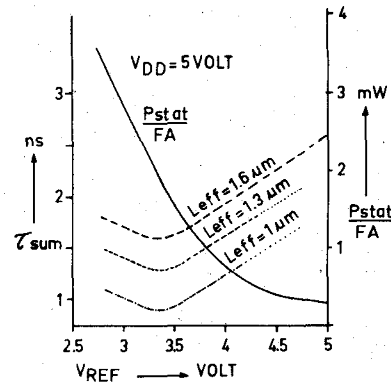

Fig. 16. Influence of V_{ref} on T_{sum} and P_{stat}.

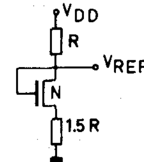

Fig. 17. Reference voltage circuit diagram.

μW/MHz is obtained. The dynamic power dissipation for the differential CVSL full adder was 80 μW/MHz with a propagation delay of 4 ns (not shown in the graph).

However, a disadvantage of the DSL full adder is its static power dissipation of 1.5 mW. Both the static power dissipation and the sum propagation delay depend on the operating temperature. Fig. 15 shows these simulated relations.

Fig. 16 shows the measured influence of the reference voltage on the sum propagation delay and the static power dissipation of the full adder, at a fixed $V_{DD} = 5$ V. The channel length of the NMOS transistors of the differential logic trees affects neither the static power dissipation nor the optimum reference voltage, which equals half the V_{DD} voltage plus the threshold voltage of the NMOS reference transistor. The static power dissipation is proportional to $(V_{DD} - V_{\text{ref}} + V_{tn} + V_{tp})^2$. Fig. 17 shows a simple example of a V_{ref} circuit for a 5 V $\pm$ 20-percent V_{DD}. The resistors can be polysilicon resistors. The cross talk from the inputs on the reference NMOS transistors does not affect the V_{ref}, because the inputs are complementary.

Experiments and simulations show that the decrease of the propagation delay by a factor of ten is the result of several steps: a factor of two is obtained by the use of differential logic trees (NMOS mostly) while application of the DSL circuit technique yields another factor of two. A factor of 2.5 is further obtained by the shorter channel length of the NMOS transistors in the logic trees.

V. Technology

The DSL circuits have been fabricated in a 2.5-μm n-well double-metal CMOS process (Table I). A -2.5-V back-bias voltage was used to improve the performance of the 1-μm L_{eff} logic NMOS transistors.

Fig. 18 shows measurements of the punchthrough voltage (VPT) [5], [6] of the n-channel transistors as a function

TABLE I
SUMMARY OF PROCESS—RELATED INFORMATION

■ LITHOGRAPHY:	CONVENTIONAL EXPOSURE EXCEPT POLYSILICON STEPPER EXPOSURE
■ TECHNOLOGY	2.5μm DOUBLE METAL N-WELL CMOS
■ GATE LENGTH.	
P-CHANNEL	3μm Leff=2.1μm
N-CHANNEL	2.5μm Leff.=2.0μm
N-CHANNEL (LOGIC TREES)	1.5μm Leff.=1.0μm
■ GATE OXIDE	500A°
■ FIELD OXIDE	6000A°
■ THRESHOLD VOLTAGES:	
V_{TP} 20/3	-1.1 V.
V_{TN} 20/2.5	1.0 V (V_{BS}=-2.5 V)
■ DESIGN RULE PITCHES	INCLUDING CONTACTS
METAL I	7.5μm
METAL II	8μm
POLYSILICON	8.75μm

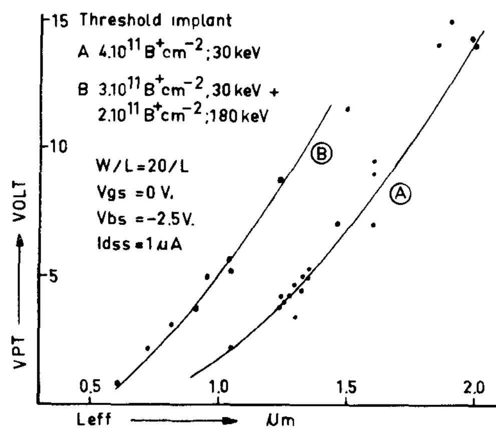

Fig. 18. Punchthrough voltage versus channel length.

of the effective channel length for two different threshold correction implants. The punchthrough voltage of the NMOS transistors is defined here as the drain–source voltage at which the drain source current of a MOSFET with grounded gate equals 1 μA ($W/L = 20/L$). Such a leakage current is allowed in the DSL circuit technique. For our 2.5-μm n-well CMOS process the threshold correction implant is 4.10^{11} B^+ cm^{-2} at 30 keV, see curve A. Curve B shows the result of a modified implant. The deep implant at 180 keV suppresses the bulk punchthrough and the increased total dose will also increase the surface concentration and thereby suppresses the surface punchthrough as well. The 1-μm device from curve B has a VPT of 5 V which corresponds with a maximum power supply voltage of 10 V in the circuitry.

It is well known that parameters like threshold voltage and transconductance of short-channel transistors may degrade because of hot-electron effects [7], [3], [4]. This degradation depends on V_{ds} and V_{gs}. The worst-case operating condition for this degradation occurs at $V_{gs} = 1/2$ V_{ds}.

Fig. 19 shows the measured lifetime of such a 1-μm NMOS transistor as a function of the drain–source voltage. The lifetime is defined as the time until a threshold shift of 100 mV appears. This curve shows that a transistor with a $L_{eff} = 1$ μm used in the differential logic trees will not suffer from hot-electron degradation. Even at power-

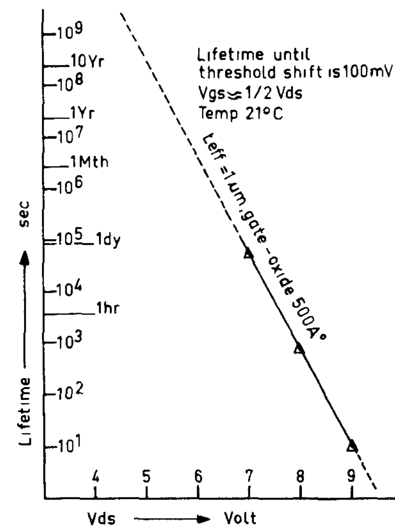

Fig. 19. Lifetime NMOS with $L_{eff} = 1$ μm.

supply voltages of 10 V the maximum V_{ds} will still be only 5 V resulting in a lifetime in excess of 10 years.

VI. APPLICATIONS

The DSL circuit technique is advantageous in high-speed complex logic circuits, i.e., multipliers, comparators, error-correcting circuits etc. In applications where the data rate is high, standard CMOS has a high dynamic power dissipation, see Fig. 14. In that case DSL compares favorably with its power-delay product.

The conversion from standard CMOS logic circuits into DSL and vice versa is straight forward. The gates of the NMOS logic transistors of the first DSL gate can simply be driven by the full V_{DD} swing of standard CMOS. For the conversion back to standard CMOS the internal node of the last DSL gate is used to drive a standard CMOS gate, because this node has a full V_{DD} swing.

Shorter channel lengths of the NMOS transistors in the logic trees, possible because of the reduced drain source voltage, can be used in every CMOS process, down to the limits of the lithography. Fig. 16 illustrates the achievable gain for different channel lengths.

In the near future electron beam exposure could be used for the submicrometer gate length in a stepper process after down scaling.

VII. CONCLUSION

The differential split-level (DSL) CMOS circuit technique has about $10\times$ shorter propagation delay as compared to conventional CMOS in the same process, but at the cost of static power dissipation. DSL can be used in a conventional process in combination with conventional as well as other CMOS techniques on the same chip to combine fast subnanosecond and slower circuitry.

Differential split-level CMOS logic is a circuit technique which allows, in any given technology, shorter channel length owing to a reduced drain–source voltage.

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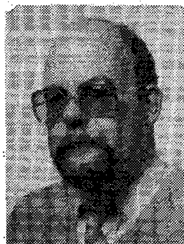

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