SESSION I: CUSTOM AND SEMI-CUSTOM DESIGN TECHNIQUES

WAM 1.3: Cascode Voltage Switch Logic: A Differential CMOS Logic Family

Lawrence G. Heller, William R. Griffin
IBM General Technology Division
Essex Junction, VT

James W. Davis, Nandor G. Thoma
IBM System Products Division
Boca Raton, FL

IMPORTANT CRITERIA for choosing a suitable VLSI logic family include power, delay, logic circuit density, device/process complexity, and compatibility with design automation tools. This paper will describe a differential CMOS logic family – Cascode Voltage Switch Logic (CVSL).

Logic design leverage is achieved in CVSL by cascoding differential pairs of MOS devices into powerful combinational logic tree networks capable of processing complex Boolean logic functions within a single circuit delay. Logic trees with N-high cascoding of differential pairs of NMOS devices are capable of processing Boolean functions with up to (2^N-1) input variables. CVSL has been found to offer a performance advantage of up to 4X compared to CMOS/NMOS primitive NAND/NOR logic families, while maintaining the expected low power characteristics of CMOS circuitry. Potentially, CVSL is twice as dense as primitive NAND/NOR logic, and is compatible with existing design automation tools. Combinational logic trees can be designed in cascoded high-peformance NMOS devices with unstacked PMOS devices used sparingly as pull-up devices in load and buffer circuitry. Optimization of the PMOS devices and the criticality of the PMOS to NMOS spacing can therefore be relaxed, relieving the device/process complexity burden for CVSL designs.

The CVSL circuit concept, in its differential form, is illustrated in Figure 1. Depending on the differential inputs, either node N1 or node N2 is pulled down by the NMOS combinational logic tree network. Regenerative action sets the PMOS latch to static outputs $Q,\overline{Q}$ of full differential V_H and ground logic levels. The logic trees are free of direct current after the latch sets. Since the inputs drive only the NMOS tree devices, input gate capacitance loading is typically a factor of 3X smaller than CMOS circuits that require complementary N-channel and P-channel devices to be driven.

The logic trees networks can be designed automatically using existing logic minimization algorithms[1]. An example of the efficiency of a differential CVSL circuit, requiring 12 devices, is shown in Figure 2. Device redundancy is naturally reduced by the functional power of the differential logic trees. Implementation of the same Boolean function in primitive CMOS NAND gates, as indicated in Figure 3, required 5 NAND gates and 28 devices, not counting the additional inverters to provide the complementary inputs. It will be noted that performance leverage in CVSL is enhanced by a reduction in the number of circuit delays compared to primitive logic. The Boolean function Q can also be implemented with 16 devices in a cascoded fully CMOS circuit.

The differential version of Figure 2, however, requires 6 fewer large P-channel devices and has considerably less input capacitance.

An experimental masterslice chip, personalized at the metal and contact levels, has been designed. The chip contains 10,880 *brickwalled* NMOS differential pairs, forming 1088 CVSL trees. The image design is compatible with existing automatic placement[2] and wiring algorithms. A photomicrograph of the chip, implemented in a 2μm CMOS technology, is shown in Figure 4. The macro in the upper right-hand corner contains 150 CVSL logic trees, which were designed top-down and automatically placed and wired from a high level language description. Other experiments include a 4b carry look-ahead ALU and several ring oscillators. Delays in the ring oscillators loaded with 0.3pF of wiring capacitance were measured in the 1 to 2ns range.

Performance of the circuit of Figure 1 is limited by the set time of the PMOS latch. A high-performance clocked CVSL circuit is illustrated in Figure 5. The outputs $Q,\overline{Q}$ are precharged low when the clock phase PC is low and data are propagated in a *domino* mode[3] when PC goes high. Feedback devices T1, T2 hold the internal nodes N1, N2 statically high prior to switching within the logic tree. The feedback devices reduce charge sharing noise within the tree and improve the noise margin, with only a small sacrifice in performance. During switching either N1 or N2 is pulled down and either device T1 or T2 is shut off. No direct current flows after switching. The logic invert function is implicit in this clocked differential CVSL circuit, a clear advantage over other incomplete domino type logic families. All logic functions can be implemented, including, for example, the XOR. A 4-way clocked XOR is illustrated in Figure 6.

Acknowledgments

The authors would like to acknowledge the work of R.S. Chelemer and J.J. Preli for their automatic placement and wiring support, the logic synthesis effort of R.D. Kilmoyer, and many others for helpful discussions.

[1] Brayton, R.K. and McMullen, C., "Decomposition and Factorization of Boolean Expressions," *Proc. IEEE ISCA*, Rome, Italy; May, 1982.

[2] Kirkpatrick, S., Gelatt, Jr., C.D. and Vecchi, N.P., "Optimization by Simulated Annealing", *Science*; May 13, 1983.

[3] Krambeck, R.H., Lee, C.M. and Law, H.S., "High-Speed Compact Circuits with CMOS," *IEEE J. Solid State Circuits*, Vol. SC-17, No. 3; June, 1982.

0193-6530/84/0000-0016$01.00 © 1984 IEEE

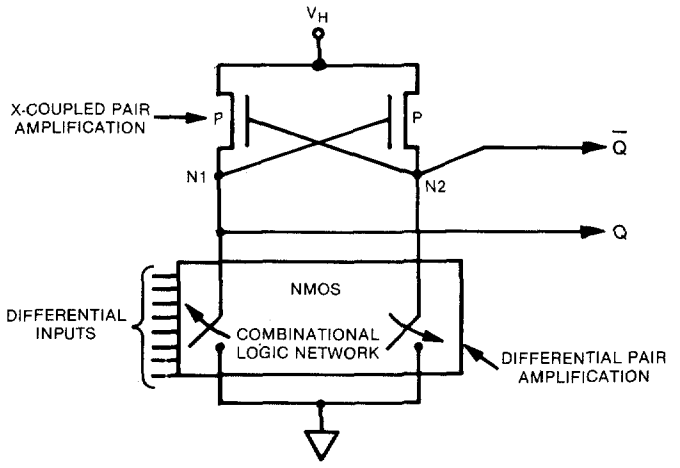

FIGURE 1—Basic CVSL circuit.

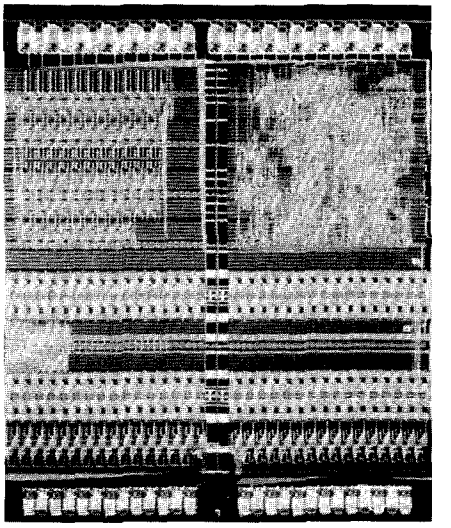

FIGURE 4—Photomicrograph of masterslice chip.

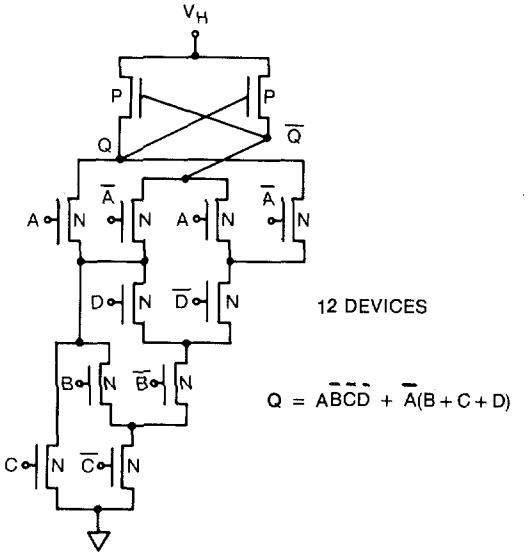

FIGURE 2—CVSL implementation of Q.

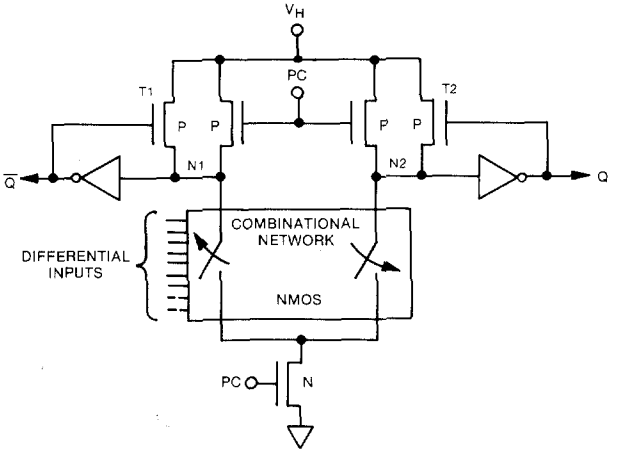

FIGURE 5—Clock CVSL.

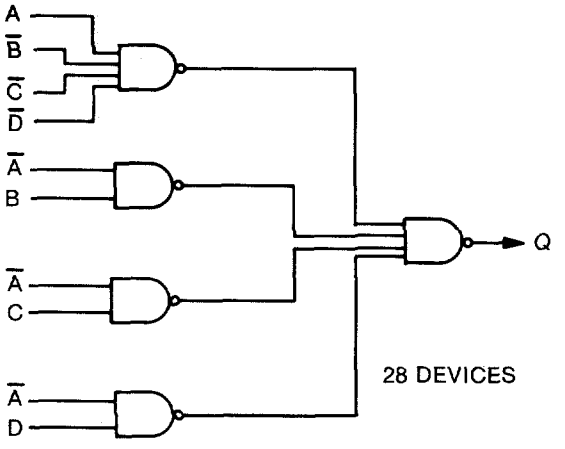

FIGURE 3—CMOS NAND implementation of Q.

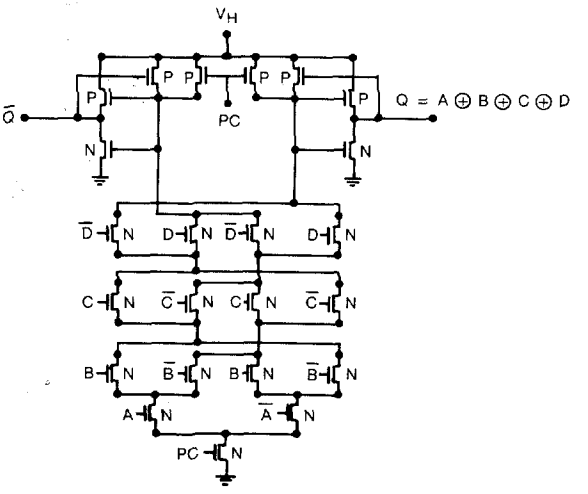

FIGURE 6—Clocked CVSL 4-way XOR.