DC INITIALIZATION PROBLEM WITH BERKELEY'S 65-nm MODEL

Some of you had problems with SPICE. The .measure statements sometimes returned bad data. I think the errors are due to DC initialization that SPICE has with Berkeley's 65-nm model file. If you looked at the waveform (that gives bad measurements), you will find that some circuit nodes are initialized at 1.8V or some unreasonable values. These wrong initializations will cause false signal transitions in your circuits and therefore affect your .measure statements.

To avoid it, you can do the following:

1. Be mindful about what your results should be;

2. If something seem wrong, check your waveforms and manually measure your results;

3. May use .ic statements in your circuits to avoid DC initialization problems (*may not solve it*).

For your reference, I attach a sample circuit file in this email. It's for finding optimal P/N ratio. The circuit will sweeps the P/N ratio and measure L→H and H→L delays. Please check my .ic statements for the syntax. Simulate the circuit with and without these .ic statements and verify the output waveforms, you'll see the difference.

```
* EEC280 - Fall 2004
* SPICE netlist for finding optimal P/N ratio
* Note: Optimal P/N ratio <=> Equal L->H and H->L delays

.param lambda=32.5nm

.include '65nm_nominal.lib'
```

```
* Parameters
* ----------
.param Wmin='4*lambda'

* Three terminal FET macros
* -------------------------
.macro nfet s g d Le='2*lambda' Wi=Wmin
MN0 s g d gnd NMOS L=Le W=Wi AS='5*lambda*Wi' PS='2*5*lambda+Wi'
+ AD='5*lambda*Wi' PD='2*5*lambda+Wi'
.eom

.macro pfet s g d Le='2*lambda' Wi=Wmin
MP0 s g d vdd PMOS L=Le W=Wi AS='5*lambda*Wi' PS='2*5*lambda+Wi'
+ AD='5*lambda*Wi' PD='2*5*lambda+Wi'
.eom

.subckt invpn in out  Wtot='6*lambda'
.param Wp = 'Wtot*pn/(pn+1)'
.param Wn = 'Wtot/(pn+1)'
MP0 out in vdd vdd PMOS L='2*lambda' W=Wp AS='5*lambda*Wp'
PS='2*5*lambda+Wp'
+ AD='5*lambda*Wp' PD='2*5*lambda+Wp'
MN0 out in gnd gnd NMOS L='2*lambda' W=Wn AS='5*lambda*Wn'
PS='2*5*lambda+Wn'
+ AD='5*lambda*Wn' PD='2*5*lambda+Wn'
.ends

.param pn=1.9

.param h=2

.param vdd=1V
.param vss=0

vdd vdd gnd vdd
vss vss gnd 0
.global vdd vss

vin in vss PULSE (vss vdd 50ps 0 0 200p 400p)

* Test cicruit

* On path gates
x1 in out11 invpn  m=1

x2 out11 out21 invpn m=1

* Gate under test
x3 out21 out31 invpn m=1

* Off path load
x5 out11 out12 invpn  m='h-1'
x6 out21 out22 invpn  m='h-1'
x7 out31 out32 invpn  m='h'

* Avoid Miller capacitance - load 1
x9  out12 out13 invpn m='h*(h-1)'
```

```
x10 out22 out23 invpn m='h*(h-1)'
x11 out32 out33 invpn m='h*h'

.ic v(out11) = vdd
.ic v(out21) = 0
.ic v(out31) = vdd

.TRAN 2ps 1ns sweep pn 1.5 2.5 0.05

.measure pnr param=pn
.measure tran tplh trig V(out21) val='vdd/2' fall=2
+                  targ V(out31) val='vdd/2' rise=2
.measure tran tphl trig V(out21) val='vdd/2' rise=2
+                  targ V(out31) val='vdd/2' fall=2
.measure tran tp param ='(tplh+tphl)/2'

.OPTIONS POST

.end
```