HSpice Analysis and Optimization

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I. **HSPICE Transient Analysis:**
Below is a spice deck for characterizing a CMOS inverter. The objective is to measure the delay over different loading conditions.

<u>Spice Deck</u>

```
* Inverter characterization
* Include library file: containing CMOS device model
.lib  'PATH/cs90_bulk'  cs90_bulk_tt
.unprot

* Declare global parameters (accessible by all circuit and sub-circuit levels)
.global  lmin

* Define parameters
.param vdd = 1.2                    * Supply voltage, in V

* Gate parameters
.param lmin = 0.11u                 * CMOS channel length (typically minimal), in meter

* Circuit and source controls
.param fo = 2                       * load (or fanout), normalized to the gate size
.param trf = 0                      * initial rise/fall time of the transient source
.param del = 0                      * initial delay time of the transient source
.param per = '100p*fo + 100p'       * signal period, adjusted according to fanout value
                                    * (larger fanout => more gate delay => more signal period)
                                    * Note: Math expression is bounded by single quotes

* Source declaration
vdd   vdd  0    vdd                 * syntax: vname  pos_node  neg_nod  voltage_value
vd    vd   0    vdd
vs    vs   0    0
vin   in   0    PULSE  0  vdd  'del'  'trf'  'trf'  'per/2-trf'  'per'
                * PULSE syntax:  val1  val2  delay  1to2time  2to1time  pulsewidth  period

* Subcircuit: Inverter
.subckt cmosinv  in  out  vd  vs
* Circuit detail
mp   out  in  vdd  vdd  pfet90  l=lmin  w=2.5u
mn   out  in  0    0    nfet90  l=lmin  w=1.0u
*
.ends cmosinv

* Test circuit:
* Note: all inverters have the same fanout, fo – except those at the end
* Stage 1:
xiv1     in      out1     vd     vs     cmosinv
```

```
*
* Stage 2:
xiv2     out1    out2    vd    vs    cmosinv
xload21  out1    load21  vd    vs    cmosinv  m='(fo-1)'
xload22  load21  load22  vd    vs    cmosinv  m='(fo*(fo-1))'
*
* Stage 3:
xiv3     out2    out3    vdd   vss   cmosinv
xload31  out2    load31  vd    vs    cmosinv  m='(fo-1)'
xload32  load31  load32  vd    vs    cmosinv  m='(fo*(fo-1))'
*
* Stage 4:
xiv4     out3    out4    vd    vs    cmosinv  m='fo'
xload41  out4    load41  vd    vs    cmosinv  m='fo*fo'

* Analysis options:
*     brief:      show short post-simulation output
*     nomod:      do not list device model
*     nowarn:     ignore warnings
*     post:       output simulation data (such as *.tr0)
*     auto-stop:  allow early termination of simulation if all measurements have been made
.options brief nomod nowarn post autostop=1

* Transition time: step, range
.tran  10p  '4*per'

* Output used parameters
.measure pfo     param='fo'

* Measure delays
.measure TRAN  td_f   TRIG   v(out2)   val='vdd/2'   rise=2
+                     TARG   v(out3)   val='vdd/2'   fall=2
.measure TRAN  td_r   TRIG   v(out2)   val='vdd/2'   fall=2
+                     TARG   v(out3)   val='vdd/2'   rise=2
* Measure rise/fall times
.measure TRAN  trout  TRIG   v(out3)   val='vdd*0.1'  rise=2
+                     TARG   v(out3)   val='vdd*0.9'  rise=2
.measure TRAN tfout   TRIG   v(out3)   val='vdd*0.9'  fall=2
+                     TARG   v(out3)   val='vdd*0.1'  fall=2

* Measure energy provided/consumed by the supplies
.measure TRAN qvs     integ  i(vss)  from  'per'  to  '2*per'
.measure  evss  param='vdd*qvs'
.measure TRAN qvd     integ  i(vdd)  from 'per'  to  '2*per'
.measure  evdd  param='vdd*qvd'

* Changing fanout parameter and resimulate
.alter
.param  fo = 3
.alter
.param  fo = 4
.alter
.param  fo = 6
.alter
.param  fo = 8
.end
```

II. Hspice Circuit Parameterization

Circuits can also be parameterized to give the user more flexibility and control. The syntax is illustrated below.

Sub-circuit parameterization:

```
(…)
.global  lmin, pn
* Subcircuit: Inverter
.subckt cmosinv  in  out  vd  vs  wpn=wt
*
* Local parameters: computable from passing or global parameters
.param wpi='wpn*pn/(pn+1)'
.param wni='wpn/(pn+1)'
*
* Circuit detail of CMOS inverter
mp    out  in  vdd  vdd  pfet90  l=lmin  w=wpi
+ ad='2*lmin*wpi'  as='2*lmin*wpi'  pd='2*(wpi+2*lmin)'  ps='2*(wpi+2*lmin)'
mn    out  in  0     0      nfet90  l=lmin  w=wni
+ ad='2*lmin*wni'  as='2*lmin*wni'  pd='2*(wni+2*lmin)'  ps='2*(wni+2*lmin)'
*
.ends cmosinv
(…)
```

Sub-circuit calling:

```
(…)
xiv3    out2    out3    vdd    vss    cmosinv   wt=wtot
xiv4    out3    out4    vdd    vss    cmosinv   wt=wtot  m='fo'
(…)
```

III. Hspice Optimization

Optimization of slff using Hspice

```
 .option probe = 0

 ******************************************************
 * parameters for area and perimeter drain and source.

 .param vdd=5.0

 .param le=0.5u
 .param wmin=0.5u
 .param wmax=50u

 .param per=2n
 .global vdd gnd

.param delta=le

 .param wn1          = optw(21.875u, wmin, wmax, delta)
 .param wn3          = optw(25u, wmin, wmax, delta)
 .param wp1          = optw(21.875u, wmin, wmax, delta)
 .param wp2          = optw(21.875u, wmin, wmax, delta)
 .param wp4          = optw(14u, wmin, wmax, delta)

 ****
.param wn2=wn1
.param wn4=wn3
.param wn5=wn3

.param wp3=wp2
.param wp5=wp4

.model opt1 opt relin=1e-5 relout=1e-5 itropt=40


 ******************************************************
 * voltage sources

 .param sutime=110p

vdd     vdd  gnd   vdd

Vclk    clkin gnd pulse 0 vdd 'per/2' 100p 100p 'per/2' per

Vdin    din   gnd pulse 0 vdd 'per/2-sutime' 100p 100p 'per*2-100p' 'per*4'
vdinc   dinc  gnd pulse vdd 0 'per/2-sutime' 100p 100p 'per*2-100p' 'per*4'


 ******************************************************
 * initial conditions

 .ic v(q)=0
 .ic v(qb)=vdd
```

```
******************************************************
* subcircuits

.subckt cmosinv in out wploc=wpinv wnloc=wninv

    m1    out in  vdd  vdd pch l=le w=wploc
    m2    out in  gnd    gnd   nch l=le w=wnloc

.ends cmosinv

*******************************************************

.subckt flipflop clk d db q qb

        Mn1     n1 d gnd gnd nch l=le w=wn1
        Mn2     n2 db gnd gnd nch l=le w=wn2
        Mn3     n3 clk gnd gnd nch l=le w=wn3
        Mn4     qb n2 n3 gnd nch l=le w=wn4
        Mn5     q n1 n3 gnd nch l=le w=wn5

        Mp1     p1 clk vdd vdd pch l=le w=wp1
        Mp2     n1 n2 p1 vdd pch l=le w=wp2
        Mp3     n2 n1 p1 vdd pch l=le w=wp3
        Mp4     qb q vdd vdd pch l=le w=wp4
        Mp5     q qb vdd vdd pch l=le w=wp5

.ends flipflop

*******************************************************


******************************************************
* instances
*

* sum logic


xflipflop clk d db q qb flipflop

xinv11 din   din2  cmosinv wploc=7.5u wnloc=3.75u
xinv12 din2  d     cmosinv wploc=7.5u wnloc=3.75u
xinv21 dinc  din2b cmosinv wploc=7.5u wnloc=3.75u
xinv22 din2b db    cmosinv wploc=7.5u wnloc=3.75u
xinv31 clkin clk2  cmosinv wploc=15u wnloc=7.5u
xinv32 clk2  clk   cmosinv wploc=15u wnloc=7.5u

* load

xinvloadq  q  qload  cmosinv wploc=2.5u wnloc=1.25u m=14
xinvloadqb qb qbload cmosinv wploc=2.5u wnloc=1.25u m=14

****************************************************
```

```
*****************************************************
* dummy cell

 xinv11d din    din2d   cmosinv wploc=7.5u wnloc=3.75u
 xinv12d din2d  dd      cmosinv wploc=7.5u wnloc=3.75u

 xinv21d dinc   dinc2d  cmosinv wploc=7.5u wnloc=3.75u
 xinv22d dinc2d dcd     cmosinv wploc=7.5u wnloc=3.75u

 xinv31d clkin  clk2d   cmosinv wploc=15u wnloc=7.5u
 xinv32d clk2d  clkd    cmosinv wploc=15u wnloc=7.5u
***************************************************


***************************************************
* tran statement

.tran  10p '8*per' sweep optimize=optw results=pdp model=opt1

***************************************************

*
* 0.5um CMOS Models
*
.MODEL nch NMOS LEVEL=3 PHI=0.700000 TOX=9.6000E-09 XJ=0.200000U TPG=1
+ VTO=0.6684 DELTA=1.0700E+00 LD=4.2030E-08 KP=1.7748E-04
+ UO=493.4 THETA=1.8120E-01 RSH=1.6680E+01 GAMMA=0.5382
+ NSUB=1.1290E+17 NFS=7.1500E+11 VMAX=2.7900E+05 ETA=1.8690E-02
+ KAPPA=1.6100E-01 CGDO=4.0920E-10 CGSO=4.0920E-10
+ CGBO=3.7765E-10 CJ=5.9000E-04 MJ=0.76700 CJSW=2.0000E-11
+ MJSW=0.71000 PB=0.9900000

.MODEL pch PMOS LEVEL=3 PHI=0.700000 TOX=9.6000E-09 XJ=0.200000U TPG=-1
+ VTO=-0.9352 DELTA=1.2380E-02 LD=5.2440E-08 KP=4.4927E-05
+ UO=124.9 THETA=5.7490E-02 RSH=1.1660E+00 GAMMA=0.4551
+ NSUB=8.0710E+16 NFS=5.9080E+11 VMAX=2.2960E+05 ETA=2.1930E-02
+ KAPPA=9.3660E+00 CGDO=2.1260E-10 CGSO=2.1260E-10
+ CGBO=3.6890E-10 CJ=9.3400E-04 MJ=0.48300 CJSW=2.5100E-10
+ MJSW=0.21200 PB=0.930000

.measure tran tdq_lh trig v(d) val='vdd/2' td='4*per' rise=1 targ v(q)
          + val='vdd/2' rise=1

.measure tran tdq_hl trig v(d) val='vdd/2' td='4*per' fall=1 targ v(q)
          + val='vdd/2' fall=1

.measure tran tdqb_lh trig v(d) val='vdd/2' td='4*per' fall=1 targ v(qb)
          + val='vdd/2' rise=1

.measure tran tdqb_hl trig v(d) val='vdd/2' td='4*per' rise=1 targ v(qb)
          + val='vdd/2' fall=1

.measure tran tdbq_lh trig v(db) val='vdd/2' td='4*per' fall=1 targ v(q)
          + val='vdd/2' rise=1

.measure tran tdbq_hl trig v(db) val='vdd/2' td='4*per' rise=1 targ v(q)
```

```
            + val='vdd/2' fall=1

.measure tran tdbqb_lh trig v(db) val='vdd/2' td='4*per' rise=1 targ v(qb)
            + val='vdd/2' rise=1

.measure tran tdbqb_hl trig v(db) val='vdd/2' td='4*per' fall=1 targ v(qb)
            + val='vdd/2' fall=1

.measure tran tclkq_lh trig v(clk) val='vdd/2' td='4*per' rise=1 targ v(q)
            + val='vdd/2' rise=1

.measure tran tclkq_hl trig v(clk) val='vdd/2' td='4*per' rise=3 targ v(q)
            + val='vdd/2' fall=1

.measure tran tclkqb_lh trig v(clk) val='vdd/2' td='4*per' rise=3 targ v(qb)
            + val='vdd/2' rise=1

.measure tran tclkqb_hl trig v(clk) val='vdd/2' td='4*per' rise=1 targ v(qb)
            + val='vdd/2' fall=1

.measure tran powinv12d avg P(xinv12d)
.measure tran powinv22d avg P(xinv22d)
.measure tran powinv32d avg P(xinv32d)

.measure tran powff avg P(xflipflop)

.measure tran powinv12 avg P(xinv12)
.measure tran powinv22 avg P(xinv22)
.measure tran powinv32 avg P(xinv32)
.measure tran pow param='(powff+powinv12-powinv12d+powinv22-powinv22d+powinv32-
powinv32d)'

.measure tran tdd param='max(max(tdq_lh, tdq_hl), max(tdqb_lh, tdqb_hl))'
.measure tran tdb param='max(max(tdbq_lh, tdbq_hl), max(tdbqb_lh, tdbqb_hl))'
.measure tran td  param='max(tdd, tdb)'
.measure tran pdp param='pow*td'                    goal < 14f

 .option acct opts nomod nopage probe post ingold=2 tnom=25 warnlin=10

.options post
.probe v(din), v(dcin), v(clkin), v(d), v(db), v(clk), v(q), v(qb)

 .end
```

IV. Optimization of 16-bit RCA using HSPICE (at the FA level)

```
* CS90 file processed by fla_estcaps version 3.3 on Wed Oct  8 23:26:01 2003
* Netlist view = schematic
*******************************************************
* hnlHspice(Opus): 3.63
* Hierarchical hspice netlist for circuit :
* rcab64
* Created : Oct  8 23:26:00 2003   By : xiaoyan
*******************************************************

.options brief nomod
.lib '/cad/techdata/avanti/hspice/cs90_bulk' cs90_bulk_tt
.options brief=0

.param vdd = 1.2
vdd vdd vss vdd
vss vss gnd 0

.param mmin = 1
.param mmax = 30
.param delta = 1
.model opt1 opt relin=1e-5 relout=1e-5 itropt=40



.param ws0331 = optw( 5, mmin, mmax, delta )
.param ws0321 = optw( 5, mmin, mmax, delta )

.param ws0311 = optw( 5, mmin, mmax, delta )
.param ws0301 = optw( 5, mmin, mmax, delta )

.param ws0231 = optw( 5, mmin, mmax, delta )
.param ws0221 = optw( 5, mmin, mmax, delta )

.param ws0211 = optw( 5, mmin, mmax, delta )
.param ws0201 = optw( 5, mmin, mmax, delta )

.param ws0131 = optw( 5, mmin, mmax, delta )
.param ws0121 = optw( 5, mmin, mmax, delta )

.param ws0111 = optw( 5, mmin, mmax, delta )
.param ws0101 = optw( 5, mmin, mmax, delta )

.param ws0031 = optw( 5, mmin, mmax, delta )
.param ws0021 = optw( 5, mmin, mmax, delta )

.param ws0011 = optw( 5, mmin, mmax, delta )
.param ws0001 = optw( 5, mmin, mmax, delta )



xadriver10 ab[10] a[10] driver m=5
xadriver11 ab[11] a[11] driver m=5
xadriver12 ab[12] a[12] driver m=5
```

```
xadriver13 ab[13] a[13] driver m=5
xadriver14 ab[14] a[14] driver m=5
xadriver15 ab[15] a[15] driver m=5
xadriver0 ab[0] a[0] driver m=5
xadriver1 ab[1] a[1] driver m=5
xadriver2 ab[2] a[2] driver m=5
xadriver3 ab[3] a[3] driver m=5
xadriver4 ab[4] a[4] driver m=5
xadriver5 ab[5] a[5] driver m=5
xadriver6 ab[6] a[6] driver m=5
xadriver7 ab[7] a[7] driver m=5
xadriver8 ab[8] a[8] driver m=5
xadriver9 ab[9] a[9] driver m=5

vadrive10 ab[10] vss 0
vadrive11 ab[11] vss 0
vadrive12 ab[12] vss 0
vadrive13 ab[13] vss 0
vadrive14 ab[14] vss 0
vadrive15 ab[15] vss 0
vadrive0 ab[0] vss pwl 0 vdd 50p 0
vadrive1 ab[1] vss 0
vadrive2 ab[2] vss 0
vadrive3 ab[3] vss 0
vadrive4 ab[4] vss 0
vadrive5 ab[5] vss 0
vadrive6 ab[6] vss 0
vadrive7 ab[7] vss 0
vadrive8 ab[8] vss 0
vadrive9 ab[9] vss 0


xbdriver10 bb[10] b[10] driver m=5
xbdriver11 bb[11] b[11] driver m=5
xbdriver12 bb[12] b[12] driver m=5
xbdriver13 bb[13] b[13] driver m=5
xbdriver14 bb[14] b[14] driver m=5
xbdriver15 bb[15] b[15] driver m=5
xbdriver0 bb[0] b[0] driver m=5
xbdriver1 bb[1] b[1] driver m=5
xbdriver2 bb[2] b[2] driver m=5
xbdriver3 bb[3] b[3] driver m=5
xbdriver4 bb[4] b[4] driver m=5
xbdriver5 bb[5] b[5] driver m=5
xbdriver6 bb[6] b[6] driver m=5
xbdriver7 bb[7] b[7] driver m=5
xbdriver8 bb[8] b[8] driver m=5
xbdriver9 bb[9] b[9] driver m=5

xbdrivercin cinb cin driver m=5
vcinb cinb vss vdd


vb1vdd bb[10] vss vdd
vb11 bb[11] vss vdd
vb12 bb[12] vss vdd
```

```
vb13 bb[13] vss vdd
vb14 bb[14] vss vdd
vb15 bb[15] vss vdd
vbvdd bb[0] vss 0
vb1 bb[1] vss vdd
vb2 bb[2] vss vdd
vb3 bb[3] vss vdd
vb4 bb[4] vss vdd
vb5 bb[5] vss vdd
vb6 bb[6] vss vdd
vb7 bb[7] vss vdd
vb8 bb[8] vss vdd
vb9 bb[9] vss vdd

.global vdd vddr vss

.subckt driver a z
mni0_n0 z a vss vss nfet90 l=0.11u w=0.32u as= 0.12p ps= 1.36u ad= 0.12p pd=
+ 1.36u
mpi0_p0 z a vdd vdd pfet90 l=0.11u w=0.48u as= 0.17p ps= 1.68u ad= 0.17p pd=
+ 1.68u
ca          a           vss   0.630f
cz          z           vss   0.581f
.ends driver
.subckt mux in0 in1 s z wmn = wm
mni2_n0 net4 s vss vss nfet90 l=0.11u w=0.5u as= 0.18p ps= 1.72u ad= 0.18p pd=
+ 1.72u m=2
mpi2_p0 net4 s vdd vdd pfet90 l=0.11u w=1u as= 0.36p ps= 2.72u ad= 0.36p pd=
+ 2.72u m=2
mni1_n0 z net4 in0 vss nfet90 l=0.11u w=0.5u as= 0.18p ps= 2.72u ad= 0.09p pd=
+ 0.86u m='wmn'
mpi1_p0 z s in0 vdd pfet90 l=0.11u w=0.5u as= 0.18p ps= 2.72u ad= 0.09p pd=
+ 0.86u m='wmn'
mni0_n0 z s in1 vss nfet90 l=0.11u w=0.5u as= 0.18p ps= 2.72u ad= 0.09p pd=
+ 0.86u m='wmn'
mpi0_p0 z net4 in1 vdd pfet90 l=0.11u w=0.5u as= 0.18p ps= 2.72u ad= 0.09p pd=
+ 0.86u m='wmn'
cin1        in1         vss   0.606f
cz          z           vss   1.026f
cs          s           vss   1.243f
cnet4       net4        vss   1.151f
cin0        in0         vss   0.606f
.ends mux

.subckt xor a b z wmn = wm
mni2_n0 z net040 vss vss nfet90 l=0.11u w=0.5u as= 0.18p ps= 1.72u ad= 0.18p
+ pd= 1.72u
mpi2_p0 z net040 vdd vdd pfet90 l=0.11u w=1u as= 0.36p ps= 2.72u ad= 0.36p pd=
+ 2.72u
mni1_n0 net8 b vss vss nfet90 l=0.11u w=0.5u as= 0.18p ps= 1.72u ad= 0.18p pd=
+ 1.72u
mpi1_p0 net8 b vdd vdd pfet90 l=0.11u w=2u as= 0.72p ps= 4.72u ad= 0.72p pd=
+ 4.72u
mni0_n0 net7 a vss vss nfet90 l=0.11u w=0.5u as= 0.18p ps= 2.72u ad= 0.09p pd=
+ 0.86u m=2
mpi0_p0 net7 a vdd vdd pfet90 l=0.11u w=1u as= 0.36p ps= 2.72u ad= 0.36p pd=
```

```
+ 2.72u m=2
mn1 net040 net8 net7 vss nfet90 l=0.11u w=0.5u as= 0.09p ps= 0.86u ad= 0.09p
+ pd= 0.86u m='wmn'
mn0 net040 b a vss nfet90 l=0.11u w=0.5u as= 0.18p ps= 2.72u ad= 0.09p pd=
+ 0.86u m='wmn'
ca              a               vss   0.978f
cb              b               vss   1.198f
cz              z               vss   0.671f
cnet040         net040          vss   1.182f
cnet7           net7            vss   0.886f
cnet8           net8            vss   1.045f
.ends xor

.subckt rcab a b cin cout s w1=ws1
xi1 a cin net014 cout mux wm=w1
xi0 b a net014 xor wm=w1
xi2 net014 cin s xor wm=w1
cload s vss 20f
.ends rcab

.subckt rcab4 a[3] a[2] a[1] a[0] b[3] b[2] b[1] b[0] cin cout s[3] s[2] s[1]
+ s[0] ws31=wss31 ws21=wss21 ws11=wss11 ws01=wss01
xi3 a[3] b[3] net10 cout s[3] rcab w1=ws31
xi2 a[2] b[2] net15 net10 s[2] rcab w1=ws21
xi1 a[1] b[1] net20 net15 s[1] rcab w1=ws11
xi0 a[0] b[0] cin net20 s[0] rcab w1=ws01
.ends rcab4

.subckt rcab16 a[15] a[14] a[13] a[12] a[11] a[10] a[9] a[8] a[7] a[6] a[5]
+ a[4] a[3] a[2] a[1] a[0] b[15] b[14] b[13] b[12] b[11] b[10] b[9] b[8] b[7]
+ b[6] b[5] b[4] b[3] b[2] b[1] b[0] cin cout s[15] s[14] s[13] s[12] s[11]
+ s[10] s[9] s[8] s[7] s[6] s[5] s[4] s[3] s[2] s[1] s[0]
+ wsss331=ws331 wsss321=ws321 wsss311=ws311 wsss301=ws301
+ wsss231=ws231 wsss221=ws221 wsss211=ws211 wsss201=ws201
+ wsss131=ws131 wsss121=ws121 wsss111=ws111 wsss101=ws101
+ wsss031=ws031 wsss021=ws021 wsss011=ws011 wsss001=ws001
xi3 a[15] a[14] a[13] a[12] b[15] b[14] b[13] b[12] net4 cout s[15] s[14]
+ s[13] s[12] rcab4 wss31=wsss331 wss21=wsss321 wss11=wsss311 wss01=wsss301
xi2 a[11] a[10] a[9] a[8] b[11] b[10] b[9] b[8] net14 net4 s[11] s[10] s[9]
+ s[8] rcab4 wss31=wsss231 wss21=wsss221 wss11=wsss211 wss01=wsss201
xi1 a[7] a[6] a[5] a[4] b[7] b[6] b[5] b[4] net9 net14 s[7] s[6] s[5] s[4] rcab4
+ wss31=wsss131 wss21=wsss121 wss11=wsss111 wss01=wsss101
xi0 a[3] a[2] a[1] a[0] b[3] b[2] b[1] b[0] cin net9 s[3] s[2] s[1] s[0] rcab4
+ wss31=wsss031 wss21=wsss021 wss11=wsss011 wss01=wsss001
.ends rcab16


xi0 a[15] a[14] a[13] a[12] a[11] a[10] a[9] a[8] a[7] a[6] a[5] a[4] a[3]
+ a[2] a[1] a[0] b[15] b[14] b[13] b[12] b[11] b[10] b[9] b[8] b[7] b[6] b[5]
+ b[4] b[3] b[2] b[1] b[0] cin cout s[15] s[14] s[13] s[12] s[11] s[10] s[9]
+ s[8] s[7] s[6] s[5] s[4] s[3] s[2] s[1] s[0] rcab16
+ ws331=ws0331 ws321=ws0321 ws311=ws0311 ws301=ws0301
+ ws231=ws0231 ws221=ws0221 ws211=ws0211 ws201=ws0201
+ ws131=ws0131 ws121=ws0121 ws111=ws0111 ws101=ws0101
+ ws031=ws0031 ws021=ws0021 ws011=ws0011 ws001=ws0001
```

```
.options post
.tran 50p 20n sweep optimize=optw results=edp model=opt1

*** measure statement to measure worst critical path ***
.measure tran tp_s15 trig v(a[0]) val='vdd/2' rise=1 targ v(s[15]) val='vdd/2' fall=1
.measure tran tp_cout trig v(a[0]) val='vdd/2' rise=1 targ v(cout) val='vdd/2' rise=1
.measure tran td param='max(tp_s15, tp_cout)' goal < 3n

.measure tran ivdd avg i(vdd)
.measure tran avgpwr param='ivdd * 1.2'
.measure tran energy param='avgpwr*td'
.measure tran edp param='energy*td'

.option acct opts nomod nopage probe post ingold=2 tnom=25 warnlin=10

.end
```