EEC280 **Fall 2005** **Take Home Exam #3**
Prof. Vojin G. Oklobdzija **Due:November 17, 2005**

State your assumptions for each problem.

Problem 1:
Use the following characterization setup (shown for a NAND2), same setup as Exam 2.

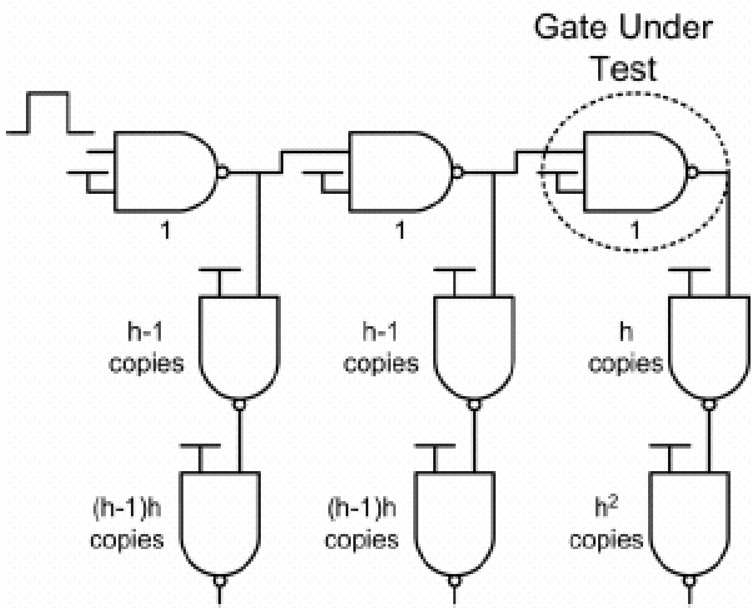

Fig. 1 Characterization Setup

Note: For inverter characterization, replace each gate in the setup with inverters, for NOR2 replace each gate in the setup with NOR2, etc...

Size each gate for equal pull up and pull down resistance.

(a) Characterize the following gates: INV, NAND2, AOI, and OAI using HSPICE. Plot the delay vs. h for each gate and input.

Note: The function for AOI is Z = (C + AB)' , and OAI is Z = ((A+B) C)'

(b) Report *g* and *p* of each gate for each input normalized to τ.

Problem 2:

Using the LE method, size the carry path (Fig. 2) of a 32-bit Kogge-Stone adder using the *g* and *p* values obtained in Problem 1. The values for branching are given in Fig. 2. Report the optimal stage effort (f_{opt}), total delay of the path, and the sizing for each gate.

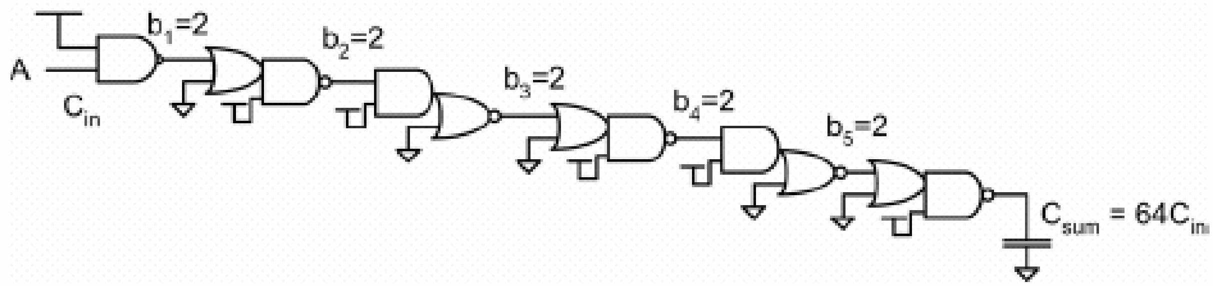

Fig. 2 Critical Carry path of 32-bit Kogge-Stone Adder.

Problem 3:
For this problem use the values of *g* and *p* obtained in problem 1.

(a) Apply LE to the circuit in Fig. 3. You can apply it by hand, using MS-Excel, or using Matlab. Just make sure to accurately account for branching. Assume the optimal solution occurs when the *f* of each gate is equal (by ignoring the parasitic delay difference of paths).

Note: DO NOT USE SIMPLE BRANCHING

Report the sizes for each gate in the circuit, the total delay, and the optimal stage effort (f_{opt}).

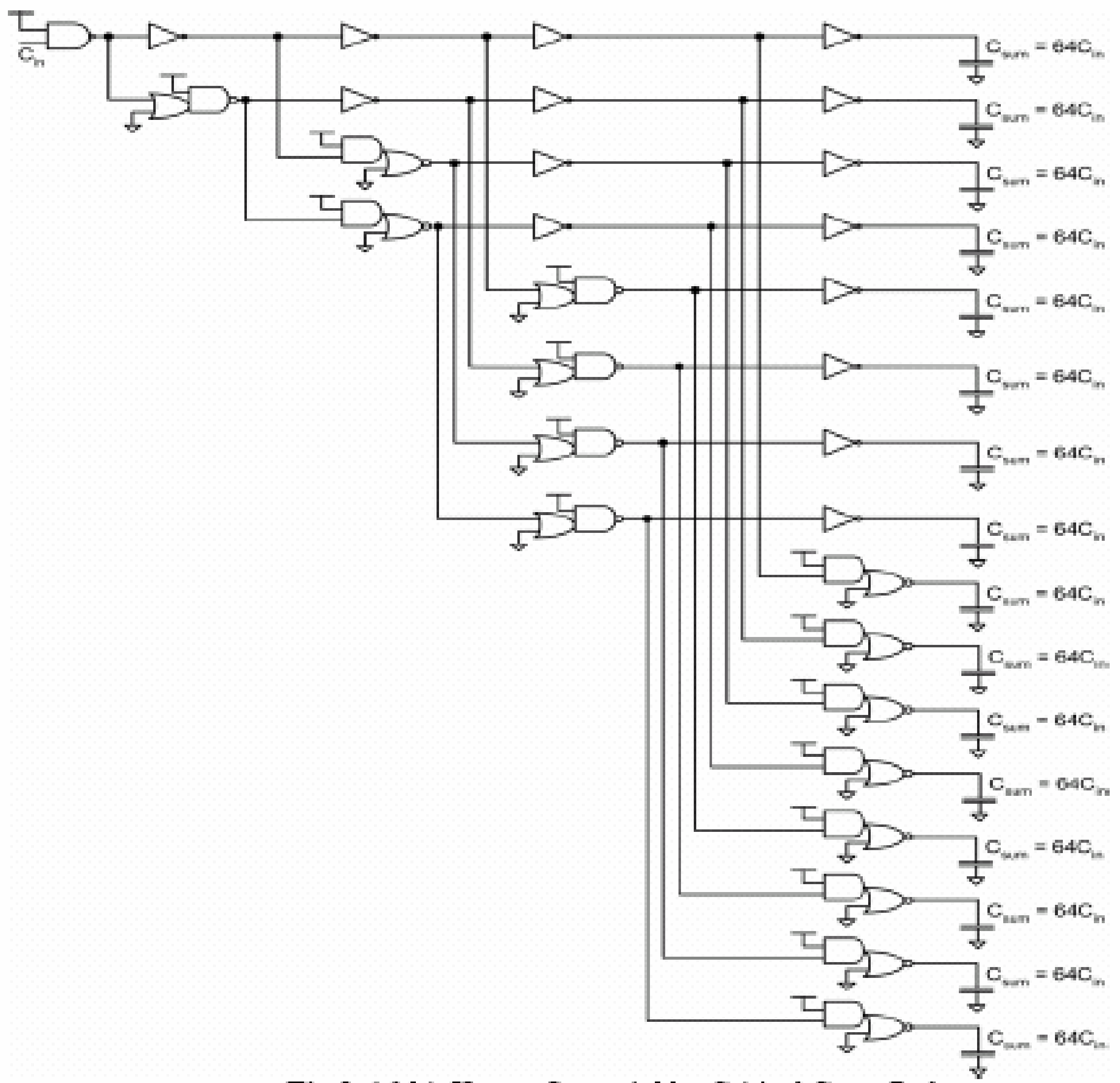

Fig 3. 16-bit Kogge-Stone Adder Critical Carry Path

(b) Simulate the circuit with HSPICE using the sizes you obtained from part (a). Use C_{in} = 4μm of gate capacitance (i.e. a NAND2 with 2μm – NMOS and 2 μm PMOS). Use the test setup shown in Fig. 4, f_{opt} refers to the value of f that you found for optimal delay.

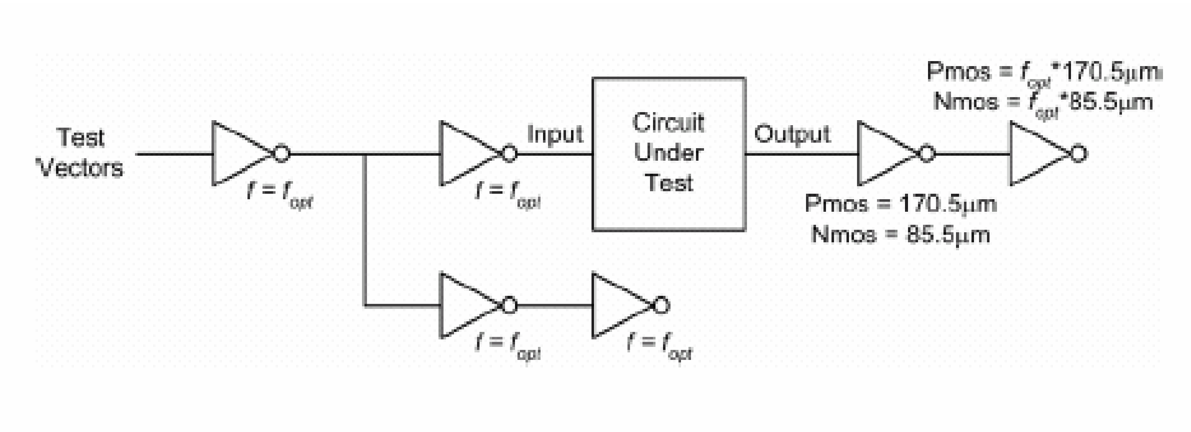

Fig. 4 Test setup for critical path of 16-bit Kogge-Stone Adder