EEC280 **Fall 2005** **Homework #4**
Prof. Vojin G. Oklobdzija **Due: November 29, 2005.**

Problem 1: Two pulsed latches are shown in Figure 1. (taken from UC Berkeley)

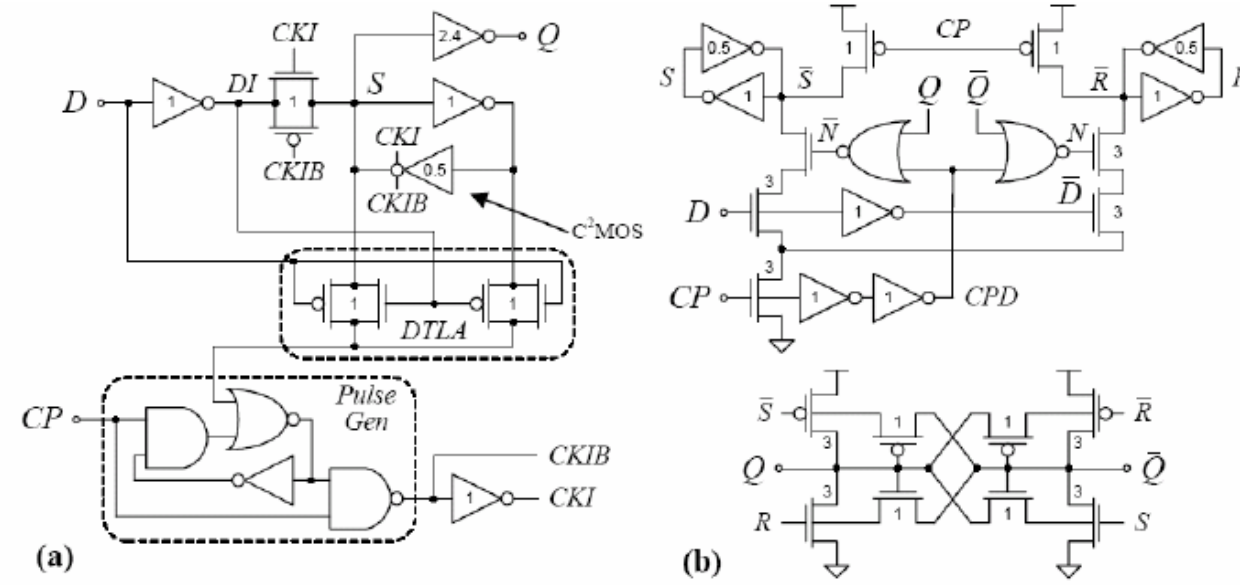


Figure 1.

a) (5pts) Briefly explain how does the circuit from Figure 1a work. What is the function of blocks labeled as *Pulse Gen* and *DTLA*?

b) (4pts) Draw a timing diagram of signals *CKI*, *DI* and *S* over 4 clock cycles for all combinations of *D* and *Q*.

c) (6pts) If the *DTLA* circuit was taken out from the schematic, and its output replaced with a constant logic level, the circuit would still operate as a pulsed latch. Compare the setup and hold times of this new flip-flop to the original one from Figure 1a.

d) (6pts) This latch can sometimes be used in your design to lower the energy dissipation. How would you calculate the switching probability of the input *D* when this flip-flop saves energy as compared to a conventional flip-flop. Label appropriate variables that you use in your calculations.

d) (5pts) Briefly explain how does the pulsed latch from Figure 1b work.

Problem 2: *Timing* (taken from UC Berkeley)

An example pipeline with a loop is shown in Figure 2a. L1 latches are transparent when C1 is high, L2 latches are transparent when C2 is high.

The pipeline is clocked by an asymmetric two-phase clock as shown in Figure 3. The clock edges are ideal and there is no skew or jitter.

Assume that the latches have propagation delays, setup and hold times equal to $t_{C\text{-}Q} = t_{D\text{-}Q} = t_{su} = t_h = 100$ps.

Each of the pipeline stages, S1, S2, S3, S4, S5, and S6 is designed using static logic.

Worst-case propagation delay of logic block S3 is dependent on both of its inputs shown in figure. Propagation delays of each of the combinational logic stages are $t_{S1} = 1$ns, $t_{S2} = 1$ns, $t_{S3} = 1.5$ns, $t_{S4} = 1.5$ns, $t_{S5} = 2$ns, $t_{S6} = 1.2$ns.

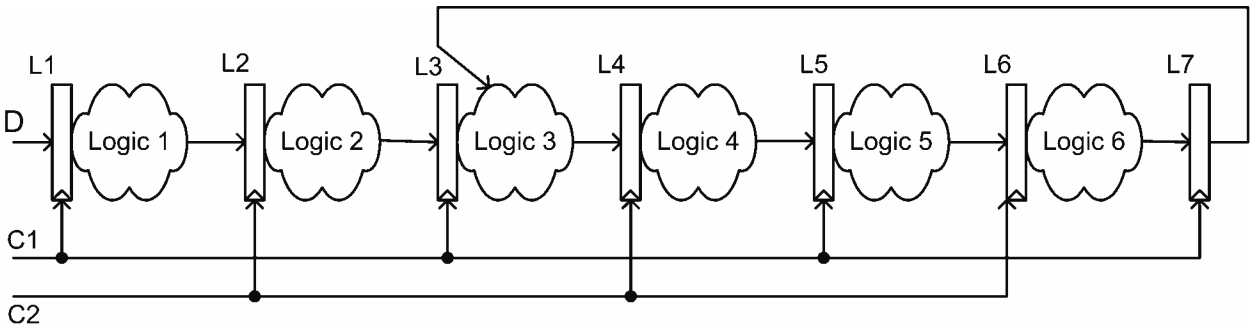


Figure 2 Pipeline system

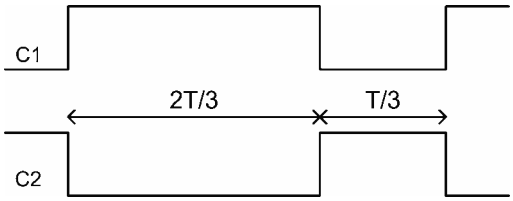


Figure 3 2-phase clock timing

(a) If the input datum D is available 200ps before the falling edge of the clock C1, what is the minimum cycle time of this system? Please show all delay constraints for this system.

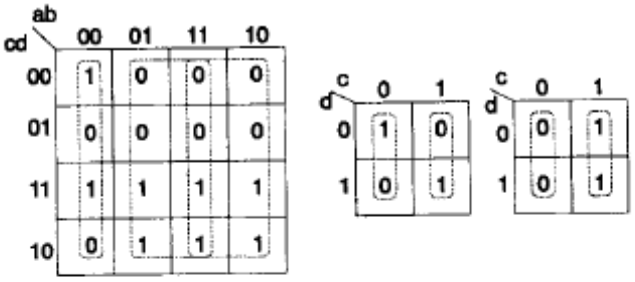
(b) How would a maximum skew of 100ps on both rising and falling edges of the clock affect your answer to question (a)?

(c) What is the minimum clock period if the input datum D arrives 200 ps *after* the falling edge of the clock. Assume zero skew.

Problem 3.

Show that the following implementation of the function given by Karnaugh-maps is incorrect and give the correct solution.

(from paper: F. S. Lai, W. Hwang, "Differential Cascode Voltage Switch with the Pass-Gate (DCVSPG) Logic Tree for High Performance CMOS Digital Systems", Proceedings of the 1993 International Symposium on VLSI Technology, Taipei, Taiwan, June 2-4, 1995)



(a)