

18-747 Lecture 1: Welcome to Modern Processor Design

James C. Hoe
Dept of ECE, CMU
August 27, 2001

Reading Assignments: S&L Ch 1

Announcements: Office hours: MW, 4:30-5:30 PM, or by appointment

No recitation this week

Everyone must hand-in a pre-course survey by noon Thursday

Handouts: Handout #0: Course Survey

Handout #1: Course Info.

Handout #2: Course Syllabus

Copyright 2001, James C. Hoe, CMU and John P. Shen, Intel



CMU 18-747
Lecture 1-2
J. C. Hoe

Course Administrativa

- ◆ Course Webpage: www.ece.cmu.edu/~ece747
- ◆ Teaching Assistants: Aaron Krol
Office Hours: TT 3~4pm, undergraduate lounge
- ◆ Course Secretary: Melissa Puryear
- ◆ Textbooks:
 - J.P. Shen & Mikko Lipasti "Fundamentals of Superscalar Processor Design", McGraw-Hill, 2001
 - M. Johnson "Superscalar Microprocessor Design", Prentice Hall, 1991
- ◆ Exams:
 - Exam 1 - Monday, October 15, 2001, In class
 - Exam 2 - TBD (week of December 3, 2001), In class

Copyright 2001, James C. Hoe, CMU and John P. Shen, Intel

Grading

- ◆ Exams: 2 in class exams
2 x 150 points
- ◆ Homework: 4 problem sets (in groups of 3 ~ 4 students)
4 x 40 points
- ◆ Project: 3 projects (in groups of 3 ~ 4 students)
70, 80, 90 points
- ◆ Total: 700 points

Final letter grades are assigned based on a curve

Copyright 2001, James C. Hoe, CMU and John P. Shen, Intel

Top 10 List: Why am I taking 18-747?

1. "I just need a capstone design course."
2. "I heard 747 was pretty easy, a stroll in the park."
3. "I heard recruiters like to see 747 on your resume."
4. "Well, everybody else was signing up for it."
5. "I heard the prof gives out CPU keychains."
6. "Hey, I thought 347 was cool, so why not 747."
7. "I want to be a CPU designer in industry."
8. "I want to be a lead architect on Intel's next flagship CPU."
9. "It will prepare me for research on modern microarchitecture."
10. "It will broaden my Ph.D. research perspective."

Copyright 2001, James C. Hoe, CMU and John P. Shen, Intel

Historical Perspectives

- ◆ The Decade of the 1970's: *"Birth of Microprocessors"*
 - Programmable Controller
 - Single-Chip Microprocessors
 - Personal Computers (PC)
- ◆ The Decade of the 1980's: *"Quantitative Architecture"*
 - Instruction Pipelining
 - Fast Cache Memories
 - Compiler Considerations
 - Workstations
- ◆ The Decade of the 1990's: *"Instruction-Level Parallelism"*
 - Superscalar, Speculative Microarchitectures
 - Aggressive Compiler Optimizations
 - Low-Cost Desktop Supercomputing

Copyright 2001, James C. Hoe, CMU and John P. Shen, Intel

Evolution of Single-Chip Micros

	1970's	1980's	1990's	2010
Transistor Count	10K-100K	100K-1M	1M-100M	1B
Clock Frequency	0.2-2MHz	2-20MHz	20M-1GHz	10GHz
Instruction/Cycle	< 0.1	0.1-0.9	0.9- 2.0	10 (?)
MIPS/MFLOPS	< 0.2	0.2-20	20-2,000	100,000

Copyright 2001, James C. Hoe, CMU and John P. Shen, Intel

Performance Growth in Perspective

- ◆ Doubling every 18 months (1982-2000):
 - total of 3,200X
 - Cars travel at 176,000 MPH; get 64,000 miles/gal.
 - Air travel: L.A. to N.Y. in 5.5 seconds (MACH 3200)
 - Wheat yield: 320,000 bushels per acre
- ◆ Doubling every 24 months (1971-2001):
 - total of 36,000X
 - Cars travel at 2,400,000 MPH; get 600,000 miles/gal.
 - Air travel: L.A. to N.Y. in 0.5 seconds (MACH 36,000)
 - Wheat yield: 3,600,000 bushels per acre

Unmatched by any other industry!!

[John Crawford, Intel, 1993]

Copyright 2001, James C. Hoe, CMU and John P. Shen, Intel

Convergence of Key Enabling Technologies:

- ◆ CMOS VLSI:
 - Submicron feature sizes: 0.8u -> 0.6u -> 0.3u -> 0.25u -> 0.18u
 - Metal layers: 3 -> 4 -> 5 -> 6 -> 7 (copper)
 - Power supply voltage: 5v -> 3.3v -> 2.4v -> 1.8v
- ◆ CAD Tools:
 - Interconnect simulation and critical path analysis
 - Clock signal propagation analysis
 - Process simulation and yield analysis/learning
- ◆ Microarchitecture:
 - Superpipelined and superscalar machines
 - Speculative and dynamic microarchitectures
 - Simulation tools and emulation systems
- ◆ Compilers:
 - Extraction of instruction-level parallelism
 - Aggressive and speculative code scheduling
 - Object code translation and optimization

Copyright 2001, James C. Hoe, CMU and John P. Shen, Intel

Course Scope

- ◆ ARCHITECTURE (ISA)
 - programmer/compiler view - “Functional appearance to its immediate user/system programmer”
- ◆ IMPLEMENTATION (microarchitecture)
 - processor designer view - “Logical structure or organization that performs the architecture”
- ◆ REALIZATION (Chip)
 - chip/system designer view - “Physical structure that embodies the implementation”

Copyright 2001, James C. Hoe, CMU and John P. Shen, Intel

Course Objectives

- ◆ The “What’s-How’s-Why’s” of Processor Design
 1. Knowledge (“what’s”)
 - Technology
 - Techniques
 2. Design Skills (“how’s”)
 - Critical Issues
 - Trade-off Intuitions
 3. Understanding (“why’s”)
 - Fundamental Principles
 - Deeper Insights

Copyright 2001, James C. Hoe, CMU and John P. Shen, Intel