UNIVERSITY OF CALIFORNIA, DAVIS
Department of Electrical and Computer Engineering

EEC180B **Digital Systems II** **Spring 1999**

Instructor:
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Grading Policy:

Midterm: May 5, 1999	25%
Final Exam	40%
Homework	5%
Quizzes	15%
Laboratory	15%

***Required* Text:** Charles H. Roth, Jr., *Digital Systems Design Using VHDL*, PWS Publishing Company, 1998

Extra Readings: A few selected papers will also be required. These will either be posted on-line or available at Navin's Copy Shop.

***Recommended* Text:** Charles H. Roth, Jr., *Fundamentals of Logic Design*, PWS Publishing Company, 1995

Statement of Course Objectives

The objective of the course is to study advanced digital system design techniques using a hardware description language, VHDL. Computer-aided design (CAD) tools will be used extensively to simulate and synthesize digital systems, which will ultimately be implemented in a Field-Programmable Gate Array (FPGA). The relationship between VHDL constructs and the resulting synthesized hardware will be studied. Advanced design topics include clocking issues, meta-stability and asynchronous inputs to digital systems, and one-hot state encoding for state machines. Class participants are expected to complete several practical designs in laboratory exercises, including arithmetic logic unit (ALU) design, register file design, state machine design, and CPU design.

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ORDERED TOPICS AND PERTINENT TEXT SECTIONS

Topics	Text Sections
Review Material (required EEC180A knowledge): **Text: Roth, *Fundamentals of Logic Design***	
Karnaugh Maps	6.1-6.4, 6.6-6.7
Multi-Level Gate Networks	8.1-8.7
Multiplexers, Decoders, ROM and PLA	9.1-9.7
Combinational Network Design	10.1-10.3
Flip-Flops	11.1-11.9
Counters and Sequential Networks	12.1-12.9
Analysis of Clocked Sequential Networks	13.1-13.4
Derivation of State Graphs and Tables	14.1-14.4
Reduction of State Tables, State Assignment	15.1-15.8
Sequential Network Design	16.1-16.4
Discrete and Integrated Circuit Logic Gates	A.1-A.4
EEC180B Material: (Very tentative - subject to change with only notice in class) **Text: Roth, *Digital Systems Design Using VHDL***	
Logic Design Review, Timing Issues, Tri-State Logic	Ch. 1 (especially 1.10-1.13)
Modeling Digital Systems in VHDL	Ch. 2
Design of Networks for Arithmetic Operations	Ch. 4
State Machine Design	Ch. 5
Additional Topics in VHDL	Ch. 8
Designing with Programmable Logic Devices	Ch. 3
Designing with FPGAs, One-Hot State Assignment	Ch. 6
Design Examples	Ch. 9, 11

Laboratory Projects (tentative)

What?	*When?*	*How much?*
Lab 1, Powerview Tutorial	Week 2 (Starting April 12)	50
Lab 2, Xilinx Tutorial	Week 3 (Starting April 19)	50
Lab 3, Synopsys/Xilinx Tutorial	Week 4 (Starting April 26)	0
Lab 4, ALU Design in VHDL	Week 5 (Starting May 3)	100
Lab 5, State Machine Design in VHDL	Week 6 (Starting May 10)	100
Lab 6, Register File Design in VHDL	Week 7 (Starting May 17)	100
Lab 7, Processor Design in VHDL	Week 8-10 (Starting May 24)	250

- **You will be working *alone* for the first 6 labs. No cooperative effort is allowed in any form.**

- **Lab projects will include a pre-lab assignment, the lab assignment design specifications, and a lab report. The pre-lab assignment and lab report will always be done individually.**

- **The due date for the pre-lab and lab report will be specified in the lab write-up.**