UNIVERSITY OF CALIFORNIA, DAVIS
Department of Electrical and Computer Engineering

EEC180B **DIGITAL SYSTEMS II** **Fall 1999**

Lab 3: Finite State Machine Design

Objective: In this lab you will design and simulate a simple sequential network.

Pre-lab: You must show up to the first lab session with your pre-lab completed. Otherwise, you will not be allowed to proceed with the lab. For pre-lab, do the complete paper design for the problem given below. The paper design must include the following:

- State transition diagram
- State assignments. Explain *how* you selected your state assignments in order to minimize the logic.
- State transition table and JK excitation tables
- K-maps
- Minimized equations

As specified in the problem, your solution is required to be minimal for your state assignment and use 10 or fewer gates and inverters.

I. Finite State Machine Specifications

Problem 16.1 in text (p. 441, Roth, Fundamentals of Logic Design, Fourth Edition)

II. Lab Requirements

1. Design the finite state machine specified above using the Altera Max+Plus II CAD package.

2. Compile your circuit for a Flex 10K device. Verify your sequential circuit by performing a timing simulation using the example input sequence given in the problem specification. Generate a printout of your simulation waveforms. Verify that the correct output sequence is produced.

III. Lab Write-up

Have your TA verify your timing simulation and then sign a verification sheet. For your lab report, include the following:

- Signed TA verification sheet.
- Graded pre-lab assignment
- Schematic of your circuit printed from Max+Plus II.
- Simulation waveforms produced by your timing simulation