UNIVERSITY OF CALIFORNIA, DAVIS
Department of Electrical and Computer Engineering

**EEC180A** **DIGITAL SYSTEMS I** **Fall 1999**

# LAB 1: INTRODUCTION TO THE ALTERA DESIGN SYSTEM

This lab provides an introduction to the Altera MAX+PLUS II design tools. You will use the Altera tools to enter schematics and perform functional and timing simulations. This lab will be done as a self-paced tutorial.

**Preparation:**

Print this lab write-up and read it thoroughly before coming to lab.

## I. Simple Counter Design

STARTING MAX+PLUS II

Altera's MAX+plus II software runs on Windows or UNIX machines.

UNIX -

- Type **setup maxplus2** to configure your environment. (This only needs to be done once.)
- Log out and log in or open a new X-window
- Type **maxplus2 &** to start the program. (For some versions, you would type **max2win &**.)

WINDOWS -

- Double-click on the MAX+plusII icon on the Windows desktop or use the Start menu to locate and start the MAX+plusII software.

USING COMMAND SHORTCUTS

In addition to the pull-down menus, Altera provides many shortcuts for performing common tasks. There is a toolbar with buttons across the top of the screen. In addition, each separate tool has a unique set of buttons along the left side of the screen. Placing the cursor over a button will display the button's function at the lower-left corner of the window. Thus, you can quickly learn the function of each button.

There are also keyboard shortcuts for commonly used commands. These are listed next to the commands in the pull-down menus. Many of these keyboard commands will be familiar, such as Ctrl-C and Ctrl-V for Copy and Paste, respectively.

By clicking the right mouse button, you can bring up a pop-up menu for a third shortcut technique.

## CREATING A SCHEMATIC

You can open a new schematic in at least three ways:

- Select **Graphics Editor** from the MAX+plusII menu, or
  Select **New** from the File menu and choose Graphics Editor file (.gdf) as the file type, or
  Click on the far-left icon on the toolbar and select Graphics Editor file (.gdf) as the file type.

Your new file will be call Untitled-x, where x is some positive integer. You should give your schematic a name and save it in your own working directory, which is probably **not** the default directory. This will let the maxplus2 software know where your files should be stored.

- Create a directory for yourself under C:\USR by using either the md command from a DOS window or Windows Explorer. For example, you may want to save your files in a directory such as C:\USR\YOUR_NAME. On a UNIX machine, create a subdirectory for your design files using the UNIX mkdir command.

- Select **Save As** (File menu); Use the mouse to locate your working directory in the Directories box. Once you have located the directory, give your blank schematic a name. The .gdf extension will be added automatically. This directory will now become your default directory for this session of maxplus2.

## PLACING COMPONENTS

To view the component libraries,

- Double-click the left-mouse button (LMB) on the workspace, or
  Select **Enter Symbol** from the Symbol pull-down menu.

The first directory listed will be your working directory. This is where symbols, which you create, will be stored. At this point, you will not have any symbols in this directory.

The second directory is named prim and contains "Primitive" devices such as the basic logic gates. To view the components available in the prim directory,

- Double-click the LMB on the prim directory in the Symbol Libraries box.

You should see an alphabetical list of the symbols contained in the prim library. You can also double-click on the mf (Macrofunction) and the mega_lpm (Megafunctions/Library of Parameterized Modules) directories. The mf library contains most of the standard 74-series components that are described in various data books.

To place a component, you can type the symbol name in the Enter Symbol dialog box or you can locate the specific symbol in one of the libraries and double-click the LMB on it.

- Bring up the **Enter Symbol** dialog box as described earlier and type **74163** as the Symbol Name. Place the 74163 component in the center of your schematic page. You may want to use the Fit in Window (View menu) option to locate the center of your schematic. Then you can change back to Normal Size (View menu).

- Place an additional 74163 symbol on your schematic in order to build a simple 8-bit counter. One way to do this is to use the Copy and Paste options from the Edit menu.

MAKING CONNECTIONS

There are two methods of drawing a net or bus between two pins.

1) If "Rubberbanding" is on, moving a device so that one pin touches another pin can make a connection. Once this occurs, the pins are connected and moving the devices apart will show a wire or bus. "Rubberbanding" can be turned on or off from the Options menu or using the icons on the left side of the screen. (By placing the cursor over each icon, you can display the function of each icon button at the bottom of the screen.)

2) If "Rubberbanding" is off, a wire must be drawn between the two pins. This is done by moving the cursor to the end of a pin until it changes from an arrow to a +. Dragging the mouse from one pin to another with the LMB pressed will draw a wire.

- Wire the two 74163 components into an 8-bit counter circuit as shown in Figure 1.

- Place **vcc** components on your schematic as needed to complete the circuit.

- Place **input** and **output** components on the schematic as shown in Figure 1.

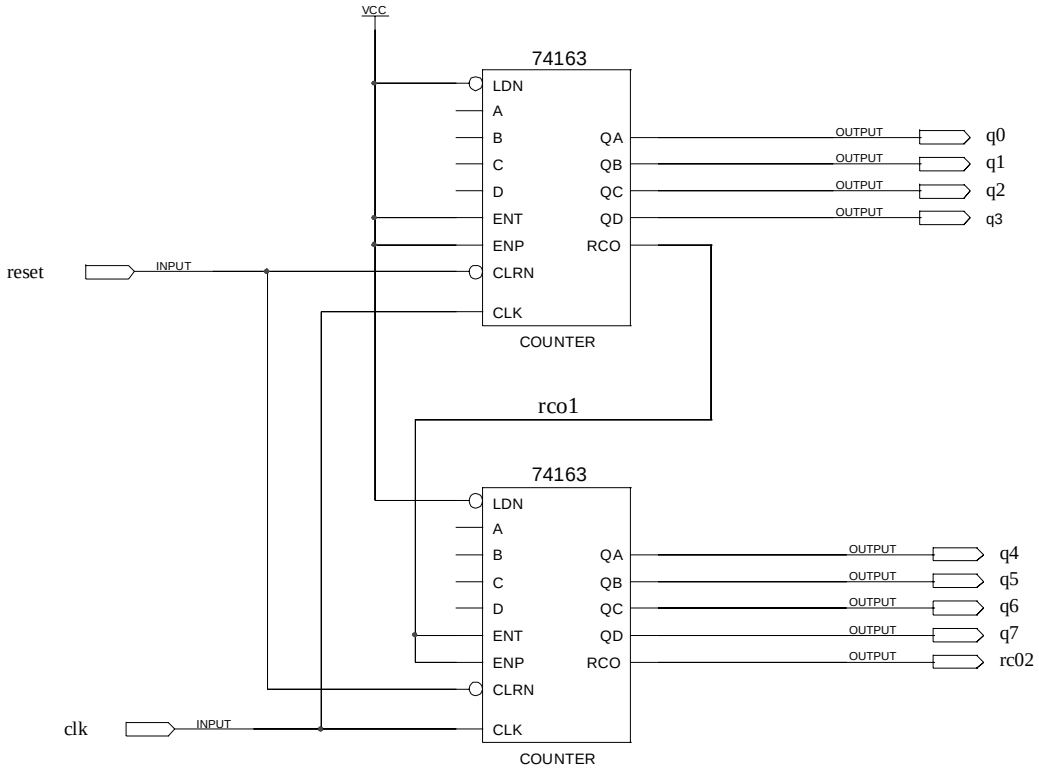


FIGURE 1. Simple 8-bit Counter

## MAKING CONNECTIONS BY NAME

Although it isn't necessary for this counter circuit, you can also make connections by labeling wires with identical signal names. Wires with the same signal name are considered to be connected by the Altera software, as long as the wires are on the same level of hierarchy. Note that a signal name must be very close to the wire that it is naming, otherwise the Altera software will just interpret it as text rather than a valid net name. Thus if you move a signal name too far away from its net, it will cease to be a valid net name. You can check if a wire or bus is labeled by clicking on the wire or bus. If the text is highlighted along with the wire or bus, then it is a valid signal name.

- Label the RCO output which connects to the ENT and ENP inputs of the other 74163 component as "rco1" as shown in Figure 1. We want to label this internal net so that we can view a trace of this signal during simulation.

## LABELING INPUTS AND OUTPUTS

You must label input and output pins for your circuit to compile properly.

- Label the input and output pins by double-clicking the LMB on PIN_NAME and typing the name for each pin as shown in Figure 1.

## SETTING THE PROJECT

Altera uses the concept of a project to organize all the files associated with a specific design. The project name should be the same as the name of the top-level design file.

- Select **Set Project to Current File** (File > Project menu) or use the appropriate icon on the tool-bar to set the project name to the name of your file.

## COMPILING A DESIGN

- Select **Save & Check** (File > Project menu) or the toolbar icon to save your file and check for errors. If your design had an error, highlight the error message and press the LOCATE button to view the location of the error in your design file.

Once your design checks without errors, you are ready to compile your design for simulation. There are two types of simulation which you can perform on your design - functional and timing. The processing for these two types of simulation is different. For functional simulation, all of your original circuit nodes can be preserved in the Simulator Netlist File (.snf). This makes it easier to view specific nodes in your circuit and debug your design. The timing simulation is useful for checking actual circuit timing before your design is programmed into an Altera Programmable Logic Device (PLD). We will start with a functional simulation.

- With the Compiler tool open, select **Functional SNF Extractor** (Processing menu). (The **Timing SNF Extractor** option must be turned off.)

- Under the Processing menu, also select the **Preserve All Node Name Synonyms** option.

- Press the Start button on the Compiler dialog box to compile your design for functional simulation.

WAVEFORM EDITOR

In order to simulate the design, you will use the waveform editor to create input stimulus.

- Select the Waveform Editor (MAX+plusII menu).

- Select **Enter Nodes from SNF** (Node menu). Now you can choose which circuit nodes to observe during simulation. The INPUTS and OUTPUTS boxes should be selected by default. Press the LIST button to view the list of input and output nodes. You will want to view all the input and output nodes in your simulation, so press the => button to copy the list to the Selected Nodes & Groups box. Select the All box and click on List again to view all the Nodes. Find the rco1 Buried node in the list, highlight it, and press the => button to add it to the Selected Nodes & Groups box. Then click OK to close the dialog box.

The waveform editor should now show the signals you selected with default waveforms. Inputs are 0 by default and outputs are X (unknown).

- Select the reset node and click on the "1" icon. The input signal should now be a constant 1. Using the LMB click and drag on the input signal from 100 ns back to time 0. Then click the "0" icon so that the input signal is low for the first 100 ns. The **Grid Size** (Options menu) determines the smallest time interval which can be selected. Set it to 50ns.

- Change the End Time (File Menu) to 26 us in order to simulate a complete cycle of the 8-bit counter as it counts from 00 to FF hex.

- Select the clk node so that the name and signal are highlighted. Then press the right mouse button and select Overwrite > Clock... (This can also be selected using an icon on the left side of the display or using the Edit pull-down menu.). Select OK to overwrite the clock. The clock period should be 100 ns.

We could run the simulation now and view the q0-q7 signal individually. However, since these outputs form an 8-bit counter, it is more convenient to group the signals together and view the count value.

- Highlight q7 to q0 and select **Enter Group** (Node menu). The group name should be q[7..0].

- Select **Save & Simulate** (File > Project menu). The waveform file should be the name of the project with the .scf file extension, which will be added automatically. You should see a functional simulation that shows the operation of the 8-bit counter circuit. Observe when the rco1 and rco2 signals are high. Compare your simulation waveforms to those shown in Figure 2.

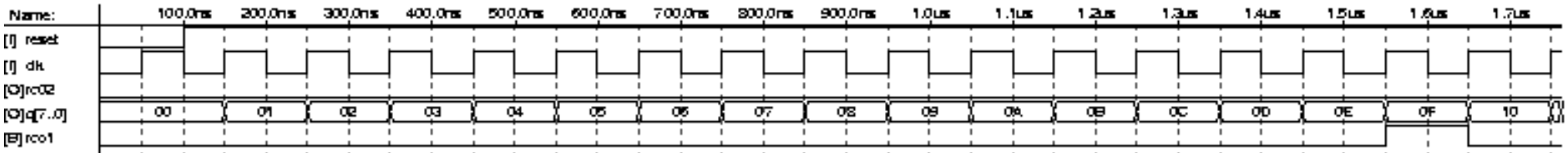


FIGURE 2. FUNCTIONAL SIMULATION

TIMING SIMULATION

You can run a timing simulation easily by re-compiling your design with the **Timing SNF Extractor** compiler option set. The Altera tools will automatically select an Altera device in which to implement the circuit. You can use the same SCF file for the timing simulation. However, buried nodes such as rco1 will not be included in the timing netlist so you will not be able to view it in the timing simulation. What is the delay from the rising clock edge until the count value changes?

## II. Simple Combinational Logic Design

This section will illustrate a technique for simulating combinational circuits. The main issue is entering the different input combinations as easily as possible, without drawing complicated waveforms for each input signal.

SCHEMATIC ENTRY AND COMPILATION

- Using the Graphic Editor, enter the schematic shown in Figure 3. This circuit is a realization of the simple Boolean expression, Y = A*B + /B*C, where "*" indicates the Boolean AND operator, "+" indicates the Boolean OR operator and "/" indicates the Boolean NOT operator. The components needed for the circuit are AND2, NOT, OR2, INPUT and OUTPUT.

- Label the pin names and internal nets as shown in Figure 3.

- Save the design, set the project to the current file and check the design.

- Compile the design for functional simulation by selecting the **Functional SNF Extractor** and the **Preserve All Node Name Synonyms** options from the Processing menu.

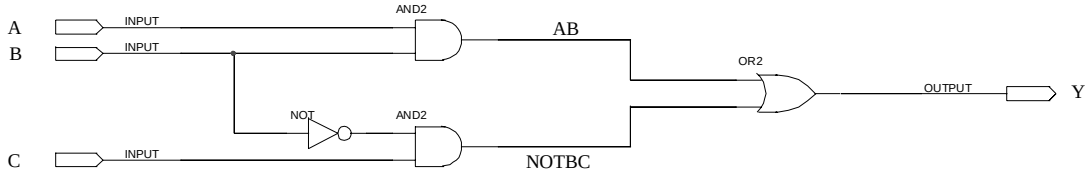


FIGURE 3. SIMPLE COMBINATIONAL CIRCUIT

ENTERING SIMULATION VECTORS

- Open the Waveform Editor and select **Enter Nodes from SNF...** option (Nodes menu). Select the inputs (A, B, and C), the output Y, and the internal signals AB and NOTBC. Recall that to view the internal signals you need to select the All box and then press LIST.

It is easier to enter the simulation input vectors by grouping the inputs rather than by drawing individual waveforms.

- Highlight C, B and A in the Waveform Editor and then select **Enter Group** (Node menu). Give the group a name such as CBA, which identifies the order the signals were grouped. (You can verify the order later.) With the group highlighted, click the right mouse button to bring up a pop-up menu and select Overwrite > Count Value. This will generate all 8 possible input combinations for the input signals. At this point, you can Ungroup your inputs to check that the name accurately reflects the group. For example, when CBA = 1, signals C and B should be 0 and A should be 1. You can simulate with the signals either grouped or ungrouped, whichever you prefer. See Figure 4 for an example simulation output with the input signals ungrouped.

You can also write a text file (.vec) to specify simulation inputs. However, this is beyond the scope of this tutorial. Extensive information is available through the Altera on-line documentation.

## Lab Report

Each individual will be required to submit a lab report. Follow the "Lab Report Information" document, which is posted on the web. Be sure to include the following items in your lab report:

- Lab cover-sheet.
- Altera schematics and simulation waveforms for the two circuits designed.

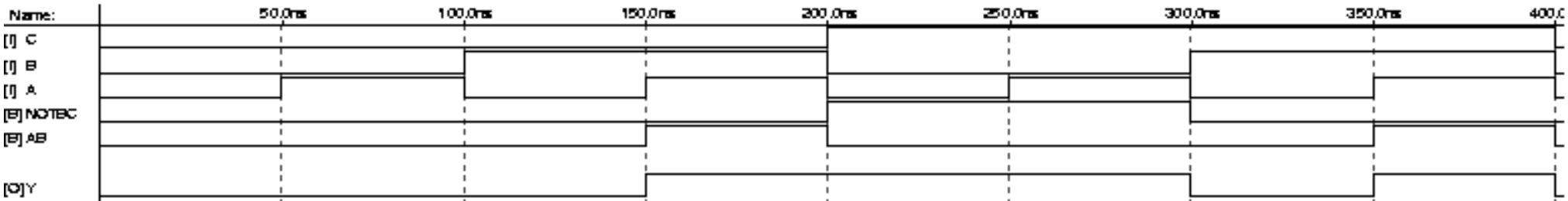


FIGURE 4. SIMULATION OUTPUT (INPUTS UNGROUPED)