UNIVERSITY OF CALIFORNIA, DAVIS
Department of Electrical and Computer Engineering

EEC180B **DIGITAL SYSTEMS II** **Fall 1999**

Labs 5 & 6: Fast ALU

Objective: In this lab project, you will design, simulate and implement a fast ALU. You will exercise your knowledge of various schemes for fast addition and you will analyze your design in order to identify the "critical path" and optimize it. You will simulate and implement your ALU and measure the "critical path". We will rank all the ALUs by their speed and the grades for this lab will be given according to speed. The fastest one in the class will receive 100%, others proportionally less according to how much slower they are from the one on the top.

Pre-lab: You must show up to the lab session with your pre-lab completed. Otherwise, you will not be allowed to proceed with the lab. For pre-lab, do the complete paper design for the problem given below. The paper design must include the following:

- Fast ALU block diagram and clear explanation of the algorithm or combinations of thereof that you are using.
- Detailed logic diagram of your ALU.
- Identify the "critical-path" and predict what the delay of this ALU will be in terms of logic levels.
- Design and explain your test set-up that you will use to measure the "critical path" - i.e. the speed of your ALU.

I. ALU Design

Design a **32**-bit ALU that will perform the arithmetic and logic operations given in Table 1. As mentioned in the objective, you are to optimize your ALU for speed.

Arithmetic Operations	**Operation**
ADD	A+B
ADDC	A+B+Cin
SUB	A-B
SUBC	A-B-Cin
NEG_A	-A
NEG_B	-B
INCR_A	A+1
INCR_B	B+1
DEC_A	A-1
DEC_B	B-1

(Table continued on next page)

Logic Operations	Operation
CMPL_A	$\overline{A}$
CMPL_B	$\overline{B}$
AND	AB
OR	A+B
XOR	$A \oplus B$
SHL_A	2A

Table 1: List of ALU Functions and Operations

II. Verification and Testing

Once you have created the schematic of your design using Max+Plus II, you should perform a simulation to verify that your ALU is functionally correct. That is, you must verify that your ALU performs each of the arithmetic and logic operations specified in Table 1 correctly.

You can also use the Delay Matrix analysis within the Timing Analyzer tool to evaluate the speed of your ALU.

After verifying the functionality of your ALU, you should perform a timing simulation that exercises the critical path. The inputs can be connected to 0 or 1 in a way that activates the critical path for a single input change. The output change at the end of the critical path should be fed back to the input at the beginning of the critical path in order to produce oscillation along the critical path. It may be necessary to invert the final output before connecting to the input at the beginning of the critical path in order to get oscillation. However, the inverter delay can be subtracted from the total delay to get the critical path delay. Connect the final output to an external pin of the Flex 10K20 device, so that you can measure the oscillation frequency when you download your design to the Altera board.

III. Implementing the ALU in an Altera board

After verifying your ALU through simulation, you will download your design to an Altera board. You should target your design for an Altera EPF10K20 device, as in previous labs. The purpose of downloading the design will be to measure the critical path, not to verify the complete functionality, which you did by simulation. Thus, you will just need to measure the oscillation frequency at the external pin that is driven by the output at the end of the critical path. The pins of the Altera Flex 10K20 device are brought out to solder points around the edges of the Altera board. You can use the oscilloscope to measure the frequency of the signal that is connected to your ALU output.

IV. Lab Requirements

1. Design the ALU specified above using the Altera Max+Plus II CAD package.

2. Compile your circuit for a Flex 10K device. Verify your circuit by performing functional and timing simulations. Generate a printout of your simulation waveforms. Verify that the correct ALU operations are performed.

3. Download your design to an Altera board and verify the operation. Demonstrate your circuit to a TA.

V. Lab Write-up

Have your TA verify your timing simulation and then sign a verification sheet. For your lab report, include the following:

- Signed TA verification sheet.
- Graded pre-lab assignment
- Schematic of your circuit printed from Max+Plus II.
- Simulation waveforms produced by your timing simulation
- Description of your test set-up.