UNIVERSITY OF CALIFORNIA, DAVIS
Department of Electrical and Computer Engineering

EEC180B **DIGITAL SYSTEMS II** **Fall 1999**

Lab 4: Display Controller

Objective: In this lab you will design, simulate and implement a finite state machine (FSM) that acts as a display controller.

Pre-lab: You must show up to the first lab session with your pre-lab completed. Otherwise, you will not be allowed to proceed with the lab. For pre-lab, do the complete paper design for the problem given below. The paper design must include the following:

- State transition diagram
- State transition table.
- K-maps
- Minimized equations for flip-flop inputs and state machine outputs. (You can choose to use either D or JK flip-flops.)

I. Finite State Machine Specifications

In this lab, you will design an FSM that will display a given sequential pattern on a 7-segment display. The output pattern to be displayed is selected using 4-bit DIP-switches, which serve as inputs to the FSM. For the purpose of this lab, only three sequential patterns will be displayed and so we will only need to specify three input codes. To understand the output pattern specifications, refer to the names of the segments of the 7-segment display shown in Figure 1. Note that the segments are active-low, meaning that a segment is turned on by a low output.

Input code (switches)	Output sequence	Output pattern description
1001	a, b, c, d, e, f	clockwise loop
0110	a, f, e, d, c, b	counter-clockwise loop
1000	a, f, g, c, d, e, g, b	figure 8

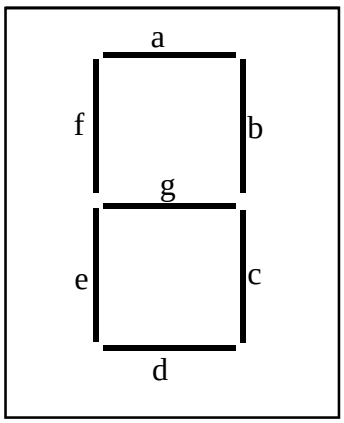

Figure 1: 7-segment display segment names

Pressing the Reset button will initialize the FSM to the start-up state. In the start-up state, no segments on the display should be lit. The inputs from the DIP-switches will then determine which sequential pattern should be displayed on the 7-segment display. When a sequence is being displayed, each segment should be lit in turn for one clock cycle. Once a sequence has completed, it will begin again as long as the input on the DIP-switches has not changed. Otherwise, if a new input is asserted, the new sequence will begin. An entire sequence must complete before a new sequence can begin, even if the DIP-switch inputs change in the midst of an output sequence. If the inputs on the 4-bit DIP-switches do not match any of the three input codes, then the FSM should remain in the start-up state with no segments lit.

II. Implementing the FSM in an Altera board

Based on the 180A Altera Tutorial II, you should be able to implement your circuit on an Altera board. You should target your design for an Altera EPF10K20 device. As in the tutorial lab, you should use one of the push-buttons for your Reset input. You should also use a clock divider circuit, as in the tutorial, in order to generate a reasonable clock frequency. (i.e. The frequency should allow you to see the output sequence clearly.) You can choose 4 of the 8 DIP-switches on the Altera board for your input switches.

III. Lab Requirements

1. Design the finite state machine specified above using the Altera Max+Plus II CAD package.

2. Compile your circuit for a Flex 10K device. Verify your sequential circuit by performing a timing simulation. Generate a printout of your simulation waveforms. Verify that the correct output sequence is produced.

3. Download your design to an Altera board and verify the operation. Demonstrate your circuit to a TA.

IV. Lab Write-up

Have your TA verify your timing simulation and then sign a verification sheet. For your lab report, include the following:

- Signed TA verification sheet.
- Graded pre-lab assignment
- Schematic of your circuit printed from Max+Plus II.
- Simulation waveforms produced by your timing simulation