UNIVERSITY OF CALIFORNIA, DAVIS
Department of Electrical and Computer Engineering

EEC180A **DIGITAL SYSTEMS I**

LAB 6: FLIP-FLOPS AND LATCHES

The purpose of this lab is to introduce the basic building blocks of sequential logic by studying several types of flip-flops and latches.

Hardware Required:

4 pcs.	74LS00	Quad 2-input NAND gate
1 pc.	74LS04	Hex INVERTER
1 pc.	74LS10	Triple 3-input NAND gate

(**Note: you should have all except one 74LS00 from previous labs.)**

Preparation

- Read the *entire* lab handout and the relevant sections of the textbook.
- For the cross-coupled NAND latch described in the lab write-up, construct a truth table which shows all inputs at a given time t and the resulting output a short time ($t+\Delta$) later.
- Based on the circuit in Figure 4, calculate the setup and hold delays, in terms of gate delays, required for proper functioning of the flip-flop. Using the datasheets available on the web, estimate the minimum setup and hold time delays based on the gate delay specifications. Show your calculations and fully justify your answer.

Description

I. Cross-Coupled NAND Latch

a) For the circuit of Figure 1, set up a transition table summarizing the operation of the circuit. (Refer to the text for a format of a transition table description of latch behavior.) In addition, develop the present state/next state table assuming equal delays. (This is a state description of the ideal behavior of the configuration.)

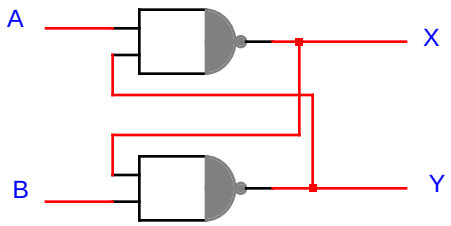

Figure 1

b) Use the circuit to build a bounceless switch shown in Figure 2. Explain why it is bounceless and compare it with a mechanical switch.

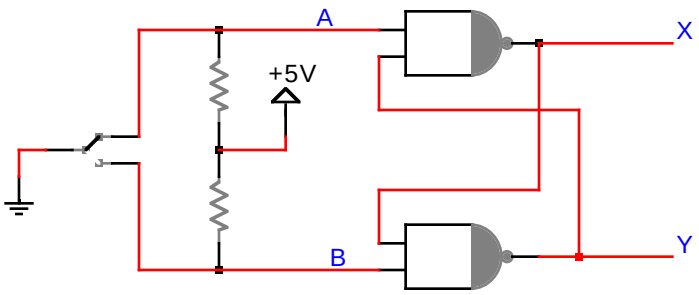

Figure 2

II. Clocked S-R Flip-Flop

Set up the circuit of Figure 3. Make a transition table for the circuit and test it using the bounceless switch as the clock. What constraints must be imposed on the inputs S-R?

a) In what way does the clock change the performance of the S-R latch? How is this useful?

b) Determine the restriction(s) relating to the width of the clock pulse.

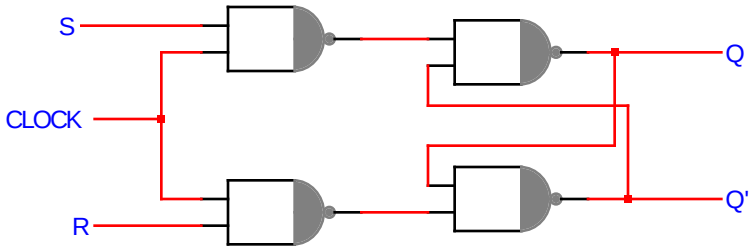

Figure 3

III. Clocked S-R Master-Slave Flip-Flop

Connect two of the clocked S-R flip-flops constructed in Part II. The clock of the second flip-flop (slave) should be the complement of the clock of the first (master).

a) Test the flip-flop using the bounceless switch as a clock. When does the output change values?

b) How does it differ from the clocked S-R flip-flop of Part II?

c) What is the advantage of this over the clocked S-R flip-flop of Part II?

IV. Positive-Edge-Triggered D Flip-Flop

A very common flop-flop in digital systems is the edge-triggered D flip-flop. Set up the circuit of Figure 4. Explain how the circuit operates and why it is "edge-triggered".

a) Test the flip-flop using the bounceless switch as a clock. When does the output change values? Verify that your circuit functions as a D flip-flop.

b) The *setup time* is defined as the time interval during which the data must be stable prior to the active clock transition. The *hold time* is defined as the interval during which a signal must be maintained after the active transition of the clock. From Figure 4, explain the setup and hold times in terms of propagation delays of the gates.

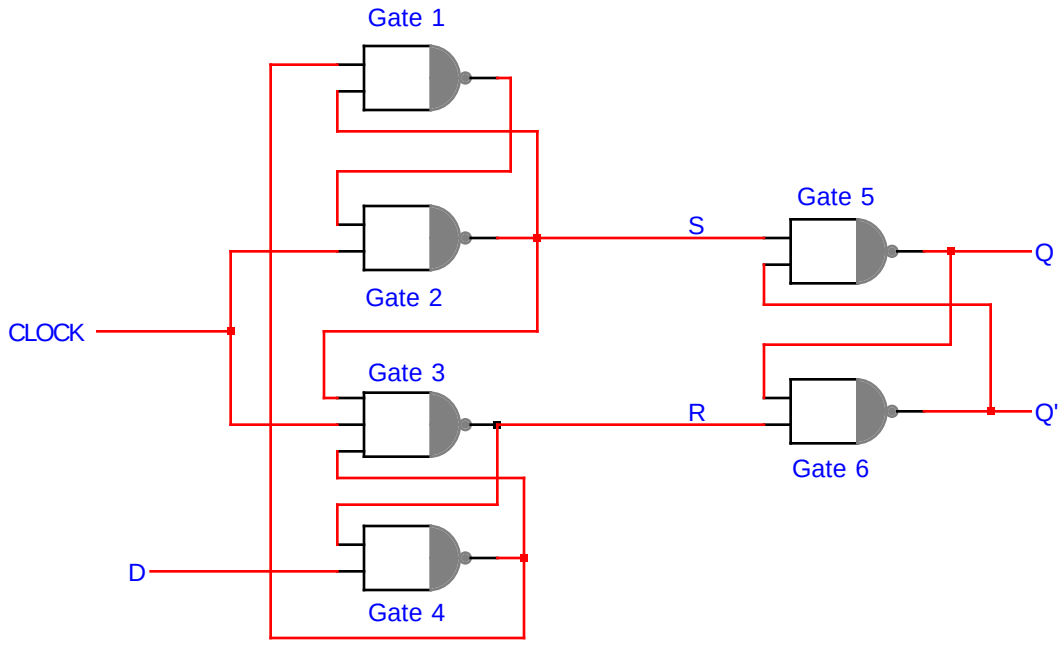

Figure 4 D-type positive-edge-triggered flip-flop

c) Connect a 74LS00 gate as an inverter as shown in Figure 5. Connect the function generator output directly to the D input and the inverted clock signal to the CLOCK input of your D flip-flop. Measure the set-up time on the scope by displaying the D and CLOCK inputs on the two channels. The setup time is measured from the point the D input signal crosses 1.5 V to the point where the rising clock edge crosses 1.5 V. Compare the measured setup time with the setup time calculated in terms of propagation delays in part b.

d) Check the Q output with the D and CLOCK signals generated as shown in Figure 5. What output would you expect in the ideal case of 0 setup time? Is this the actual output value or was there a setup time violation which caused a different value to be latched. If the delay of your 74LS00 is small enough, you should be able to observe a setup time violation.

e) If you observed a setup time violation in part d, add an additional inverter to the CLOCK input to increase the setup time. Check if a setup time violation still occurs. Determine how many inverters are required to meet the setup time.

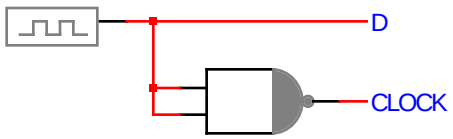

Figure 5 D and CLOCK inputs for measuring setup time

V. D Latch

The circuit shown in Figure 6 represents a D-type latch.

a) Test the latch using the bounceless switch as the enable. When does the output change values? Does the circuit work as you expect?

b) Describe the setup and hold times in terms of propagation delays.

c) (Optional) Do you see a flaw in this design? What kind of problem can result?

d) (Optional) Try to use an inverter to violate the setup time. Describe your results.

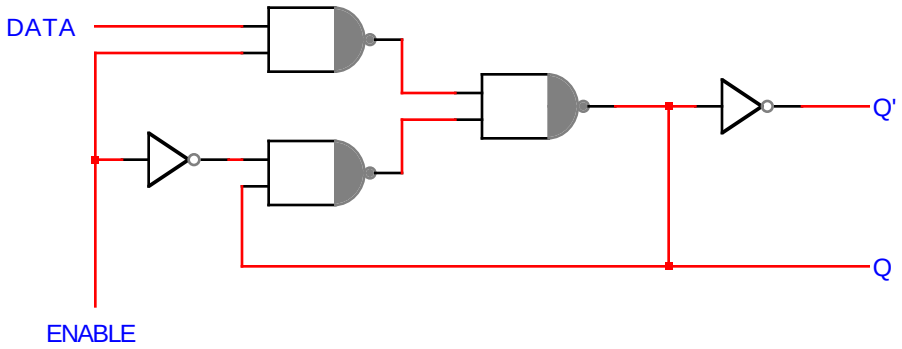

Figure 6 D-type latch

Lab Report

In your report, answer ALL questions in all parts of this handout. Some parts have multiple questions. Other parts require a detailed description or explanation. Be as complete and precise as possible. In addition, turn in your graded pre-lab and TA verification sheet. (The TA will specify which parts he or she will verify.)