EEC180A   **DIGITAL SYSTEMS I**   **Winter 2006**

Lab 6: Counter Design

This lab introduces sequential network design using J-K flip-flops. Since counters are one of the simplest types of sequential networks, counter design is a good starting point in studying sequential circuits.

Hardware Required:

New parts:
2	74LS73A	Dual negative-edge-triggered J-K flip-flops
3	LED & 390 ohm resistor	Current-limiting resistors and LEDs

Parts from previous labs:
2	74LS00	Quad 2-input NAND gates
1	74LS04	Hex inverters (if needed)

Preparation

- Design the sequential networks for the 3-bit counter in part 1. The designs are to be done on paper **before** coming to lab.

Description

1. Design all the sequential networks described below. The designs are to be done on paper **before** coming to lab.
    Design a 3-bit counter which counts in the sequence:
    001, 011, 010, 110, 111, 101, 100, 001, …
    (a) Use clocked D flip-flops.
    (b) Use clocked J-K flip-flops.
    (c) Use clocked T flip-flops.
    (d) Use S-R flip-flops.
    (e) What will happen if the counter of (a) is started in state 000.

2. Enter your design for (b) into Altera and verify it through functional simulation. What happens if the counter of (b) is started in state 000?

3. Build your design for part (b) on your protoboard. Verify your design in the lab. You can use the function generator for the clock signal and display the counter outputs using LEDs. Be sure to use current-limiting resistors (approx 390 - 470 ohms) for lighting the LEDs. Have the TA verify your circuit.

Lab Report

Each individual will be required to submit a lab report. Be sure to include the following items:

- Lab cover sheet with TA verification for circuit performance.
- Graded pre-lab
- Altera schematics and simulation waveforms for the J-K counter.

Grading

Prelab	30 points
Lab Checkoff	60 points
Lab Report	10 points