UNIVERSITY OF CALIFORNIA, DAVIS
Department of Electrical and Computer Engineering

EEC180A **DIGITAL SYSTEMS I** **Winter 2006**

LAB 2: INTRODUCTION TO THE ALTERA DESIGN SYSTEM

This lab provides an introduction to the Altera Quartus II design software. You will use the Altera tools to enter schematics and perform functional and timing simulations. This lab will be done as a self-paced tutorial.

Preparation:

Print this lab write-up and read it thoroughly before coming to lab.

I. Simple Counter Design

STARTING QUARTUS II

The ECE Department has Altera's Quartus II software installed on the Linux and UNIX workstations.

- Type **setup quartus** to configure your environment. (This only needs to be done once.)
- Log out and log in, or open a new X-window
- Type **quartus &** to start the program.
- The first time you start the software, you will be prompted with a "Look and Feel" dialog box. Select the top option, "Quartus II".
- If prompted to automatically look for updates, select "No".
- You will then be prompted to create a new project. Click "Yes". For this first lab, you only need to fill out Page 1/6. Choose a Project directory, something like **eec180a/lab1/**. Then choose a name for the design, like **counter**. Then click "Finish".

WINDOWS -

Altera provides a free web-based version of Quartus II that you can download from:
https://www.altera.com/support/software/download/altera_design/quartus_we/dnl-quartus_we.jsp
Note that the file you must download is greater than 180 MB, so plan accordingly.

USING COMMAND SHORTCUTS

In addition to the pull-down menus, Altera provides many shortcuts for performing common tasks. There is a toolbar with buttons across the top of the screen. In addition, each separate tool has a unique set of buttons along the left side of the screen. Placing the cursor over a button will display the button's function at the lower-left corner of the window. Thus, you can quickly learn the function of each button.

There are also keyboard shortcuts for commonly used commands. These are listed next to the commands in the pull-down menus. Many of these keyboard commands will be familiar, such as Ctrl-C and Ctrl-V for Copy and Paste, respectively.

By clicking the right mouse button, you can bring up a pop-up menu for a third shortcut technique.

CREATING A SCHEMATIC

You can open a new schematic in at least three ways:

- Type CTRL-n, or
- Select **New** from the File menu , or
- Click on the far-left icon on the toolbar

Then select "Block Diagram/Schematic File" from the list, and click "OK".

Your new file will be called Block x.bdf, where x is some positive integer. You should give your schematic a name and save it in your own working directory.

- Select **Save As** (File menu); Use the mouse to locate your working directory in the Directories box. Once you have located the directory, give your blank schematic a name. The .bdf extension will be added automatically. This directory will now become your default directory for this session of quartus.

PLACING COMPONENTS

To view the component libraries,

- Double-click the left-mouse button (LMB) on the workspace, or
  Right-click on the schematic, and select Insert->Symbol.

- On the left hand side, click the + box to view the libraries.

- Double-click on "others", and then "maxplus2".

You should see an alphabetical list of the symbols contained in the maxplus2 library. This library contains most of the standard 74-series components that are described in various data books.

To place a component, you can type the symbol name in the Name dialog box or you can locate the specific symbol in one of the libraries and double-click the LMB on it.

- Select the **74163** as the Symbol Name. Place the 74163 component in the center of your schematic page. You may want to use the Fit in Window (View menu->Zoom) option to locate the center of your schematic. Then you can change back to Normal Size (View menu).

- Place an additional 74163 symbol on your schematic in order to build a simple 8-bit counter. One way to do this is to use the Copy and Paste options from the Edit menu, or the keyboard shortcuts..

MAKING CONNECTIONS

There are two methods of drawing a net or bus between two pins.

1) If "Rubberbanding" is on, moving a device so that one pin touches another pin can make a connection. Once this occurs, the pins are connected and moving the devices apart will show a wire or bus. "Rubberbanding" can be turned on or off from the Options menu or using the icons on the left side of the screen. (By placing the cursor over each icon, you can display the function of each icon button at the bottom of the screen.)

2) If "Rubberbanding" is off, a wire must be drawn between the two pins. This is done by moving the cursor to the end of a pin until it changes from an arrow to a +. Dragging the mouse from one pin to another with the LMB pressed will draw a wire.

- Wire the two 74163 components into an 8-bit counter circuit as shown in Figure 1.

- Place **vcc** components on your schematic as needed to complete the circuit. You'll find vcc in the “primitives->other” library.

- Place **input** and **output** components on the schematic as shown in Figure 1. You'll find input and output components in the “primitives->pin” library.

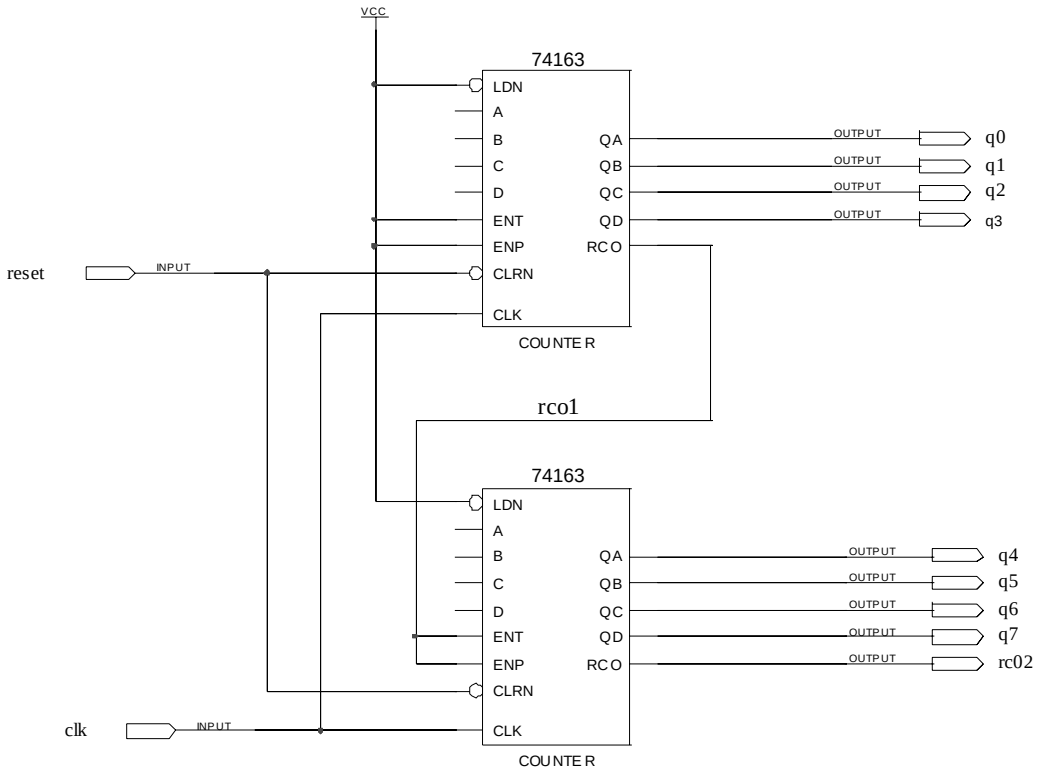

FIGURE 1. Simple 8-bit Counter

MAKING CONNECTIONS BY NAME

Although it isn't necessary for this counter circuit, you can also make connections by labeling wires with identical signal names. Wires with the same signal name are considered to be connected by the Altera software, as long as the wires are on the same level of hierarchy. Note that a signal name must be very close to the wire that it is naming, otherwise the Altera software will just interpret it as text rather than a valid net name. Thus if you move a signal name too far away from its net, it will cease to be a valid net name. You can check if a wire or bus is labeled by clicking on the wire or bus. If the text is highlighted along with the wire or bus, then it is a valid signal name.

- Label the RCO output which connects to the ENT and ENP inputs of the other 74163 component as "rco1" as shown in Figure 1. We want to label this internal net so that we can view a trace of this signal during simulation.

LABELING INPUTS AND OUTPUTS

You must label input and output pins for your circuit to compile properly.

- Label the input and output pins by double-clicking the LMB on PIN_NAME and typing the name for each pin as shown in Figure 1.

COMPILING A DESIGN

- Select **Save** (File menu) or the toolbar icon to save your file.

Once you are ready to compile your design for simulation, there are two types of simulation which you can perform on your design - functional and timing. The processing for these two types of simulation is different. For functional simulation, the timing characteristics of the components in your circuit are not considered. The timing simulation is useful for checking actual circuit timing before your design is programmed into an Altera Programmable Logic Device (PLD). We will start with a functional simulation.

- Open the Simulator tool (Tools->Simulator Tool).

- In the Simulation Mode box, select Functional, the click the Generate Functional Simulation Netlist button. Verify that there are no errors in your design.

WAVEFORM EDITOR

In order to simulate the design, you will use the waveform editor to create input stimulus.

- At the bottom of the Simulator tool, click Open. The Waveform Editor will be opened.

- In the Waveform Editor, Right-click in the left frame. Select “Insert Node or Bus”, then click the Node Finder button.

- In the Node Finder window, select Pins: unassigned in the Filter box, then click the List button. You should see most of your nodes in the Nodes Found box.

- Click the >> button to select all of the nodes.

- You should now have everything except rco1 in the “Selected Nodes” list. To select rco1, choose Device Entry (all Names) in the Filter box, click List again, and add rco1 to the selected nodes list.

The waveform editor should now show the signals you selected with default waveforms. Inputs are 0 by default and outputs are X (unknown).

- Select the reset node and click on the "1" icon. The input signal should now be a constant 1. Using the LMB click and drag on the input signal from 100 ns back to time 0. Then click the "0" icon so that the input signal is low for the first 100 ns. The **Grid Size** (Edit menu) determines the smallest time interval which can be selected. Set it to 50ns.

- Change the End Time (Edit Menu) to 26 us in order to simulate a complete cycle of the 8-bit counter as it counts from 00 to FF hex.

- Select the clk node so that the name and signal are highlighted. Then press the right mouse button and select Value -> Clock... (This can also be selected using an icon on the left side of the display or using the Edit pull-down menu.). Select OK to overwrite the clock. The clock period should be 100 ns.

We could run the simulation now and view the q0-q7 signal individually. However, since these outputs form an 8-bit counter, it is more convenient to group the signals together and view the count value.

- Highlight q7 to q0, right click and select **Group**. The group name should be q[7..0], and the radix should be hexadecimal.

- Save your project. The waveform file should be the name of the project with the .vwf file extension, which will be added automatically.

- From the simulator tool window, verify that the following settings are checked:
  - Run simulation until all vector stimuli are used.
  - Automatically add pins to simulation output waveforms
  - Overwrite simulation input file with simulation results

  Then click the Start button. You should see a functional simulation that shows the operation of the 8-bit counter circuit. Observe when the rco1 and rco2 signals are high. Compare your simulation waveforms to those shown in Figure 2.

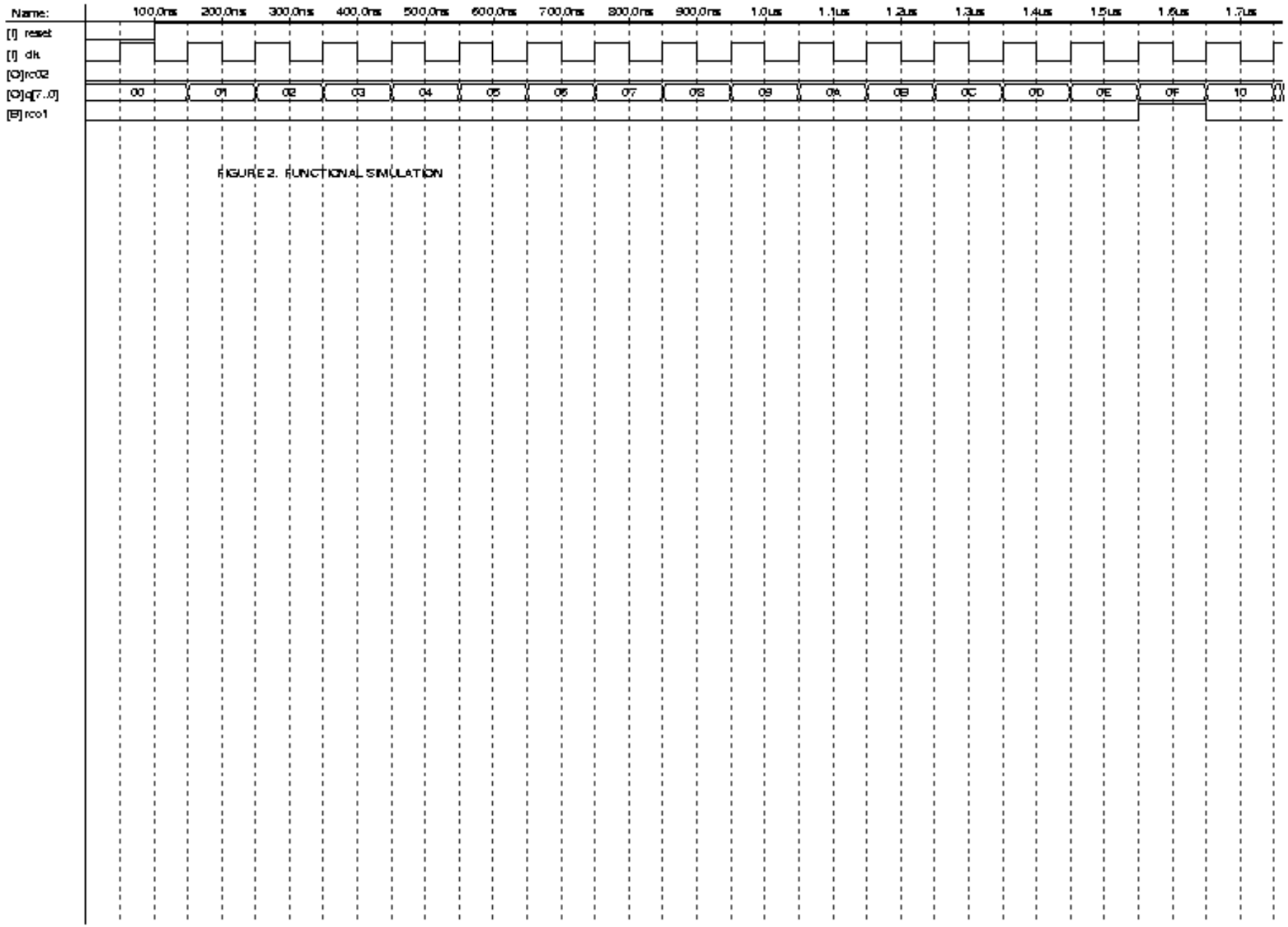

FIGURE 2. FUNCTIONAL SIMULATION

TIMING SIMULATION

You can also run a timing simulation for your design. Open the Compiler Tool (Tools->Compiler Tool), and click the Start button. This will complete all the compilation steps necessary for Timing simulation. Once a full compilation is complete, you can change the simulation mode in the Simulator tool to “Timing”, and rerun the simulation (click Start). The Altera tools will automatically select an Altera device in which to implement the circuit. You can use the same VWF file for the timing simulation. However, buried nodes such as rco1 will not be included in the timing netlist so you will not be able to view it in the timing simulation. What is the delay from the rising clock edge until the count value changes?

II. Simple Combinational Logic Design

This section will illustrate a technique for simulating combinational circuits. The main issue is entering the different input combinations as easily as possible, without drawing complicated waveforms for each input signal.

SCHEMATIC ENTRY AND COMPILATION

- Using the Graphic Editor, enter the schematic shown in Figure 3. This circuit is a realization of the simple Boolean expression, Y = A*B + /B*C, where "*" indicates the Boolean AND operator, "+" indicates the Boolean OR operator and "/" indicates the Boolean NOT operator. The components needed for the circuit are AND2, NOT, OR2, INPUT and OUTPUT.

- Label the pin names and internal nets as shown in Figure 3.

- Save the design, set the project to the current file and check the design.

- You'll want to change the settings on your compiler to **Preserve All Node Name Synonyms.** To do so, click on Assignments->Wizards->Compiler Settings Wizard, and click through to page 2 of 6. For the second question, select “no”, and then click finish.

- **Open the Compiler tool, and run only the Analysis and Synthesis portion of the compilation.**

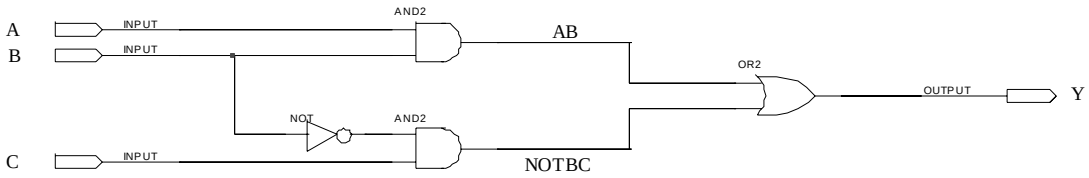

FIGURE 3. SIMPLE COMBINATIONAL CIRCUIT

ENTERING SIMULATION VECTORS

- Open the Simultor tool, select Functional simultion, then click Open to start the Waveform Editor. Select the inputs (A, B, and C), and the output Y.

It is easier to enter the simulation input vectors by grouping the inputs rather than by drawing individual waveforms.

- Highlight C, B and A in the Waveform Editor and then right-click and select **Group**. Give the group a name such as CBA, which identifies the order the signals were grouped. (You can verify the order later.) With the group highlighted, click the right mouse button to bring up a pop-up menu and select Value -> Count Value. This will generate all 8 possible input combinations for the input signals. At this point, you can Ungroup your inputs to check that the name accurately reflects the group. For example, when CBA = 1, signals C and B should be 0 and A should be 1. You can simulate with the signals either grouped or ungrouped, whichever you prefer. See Figure 4 for an example simulation output with the input signals ungrouped.

Lab Report

Each individual will be required to submit a lab report. Follow the "Lab Report Information" document, which is posted on the web. Be sure to include the following items in your lab report:

Lab cover-sheet.
Altera schematics and simulation waveforms for the two circuits designed.

Grading

Lab Checkoff	80 points
Report	20 points
Printout of schematics waveforms (5 points each)	

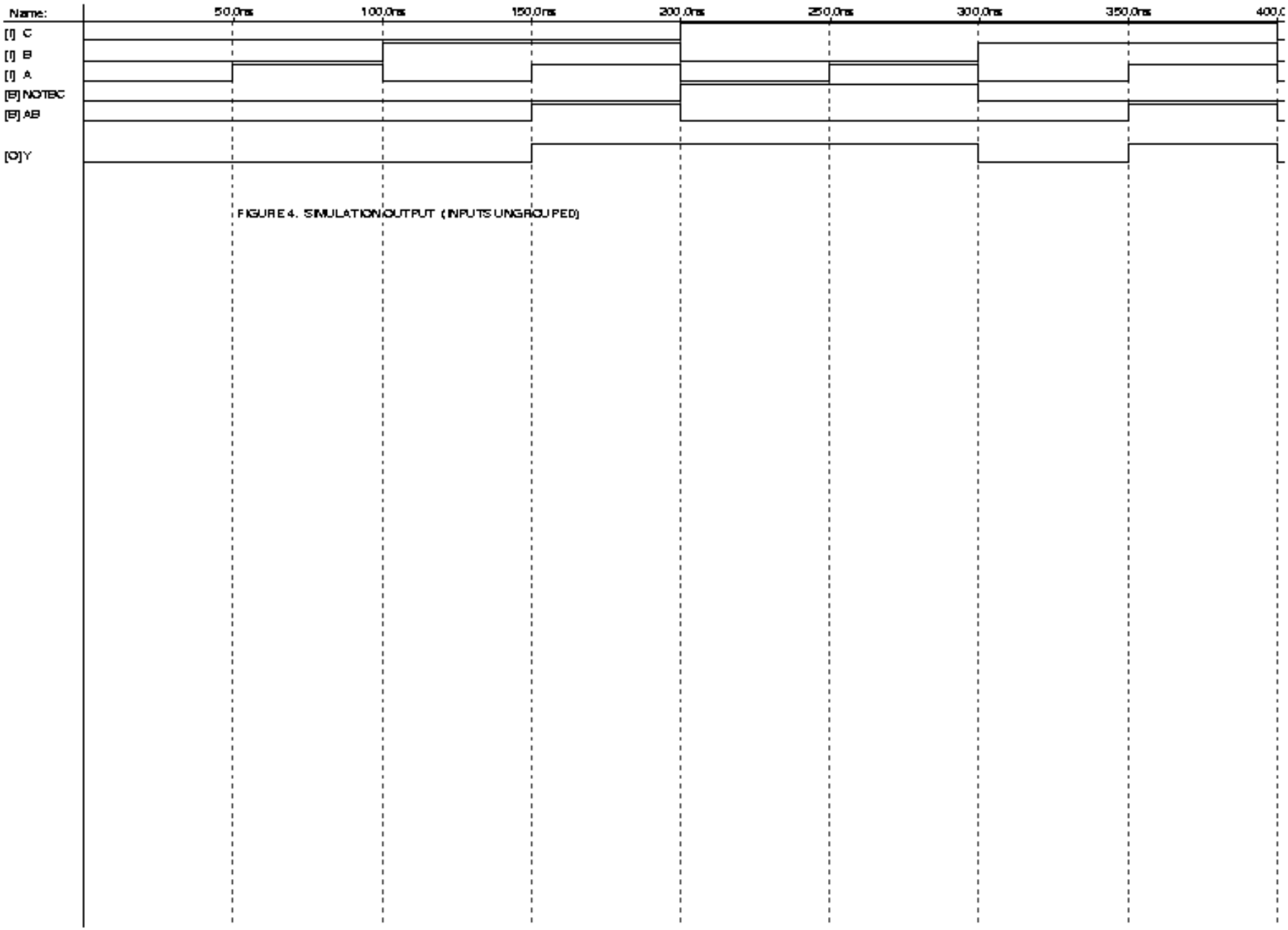

FIGURE 4. SIMULATION OUTPUT (INPUTS UNGROUPED)