

**EEC 118 EXPERIMENT No. 4
MASTER-SLAVE FLIP-FLOP***

I. OBJECTIVE

In this experiment you will build dynamic and a static master-slave latch out of inverters and transistors and measure CLOCK to Q for setup violation. Due to the high threshold voltage of the CD4007 transistors, a 15V power supply is used.

II. DYNAMIC MASTER-SLAVE FLIP-FLOP

- (1) In this experiment you will build dynamic and a static master-slave latch out of inverters and transistors and measure CLK-to-Q for setup violation. Due to the high threshold voltage of the CD4007 transistors, a 15V power supply is used.
- (2) Verify that the circuit operates as a master-slave latch by connecting the D input to the \bar{Q} output. With this connection, the output of the master-slave latch will be the clock divided by 2. Use a 10kHz square wave that goes from 0 to 15V for the clock (CLK). Use $C = 1000 \text{ pF}$. Sketch the CLK, \bar{M} and Q waveforms and measure the delay between the rising edge of the clock and output Q. At what part of the clock waveform is the D input latched? Increase the CLK frequency and measure the delay between the rising edge of the clock and output Q. At what clock frequency the master-slave latch fails? (**NOTE:** To get up to 15V peak-to-peak, you need to set the output impedance of the function generator to High Impedance mode, instead of 50-Ohm mode. In addition, due to the low offset voltage allowable from the function generator, you should use an external DC-supply for the offset voltage.)
- (3) Tie the D input high (connect it to V_{DD}). Sketch the clock CLK and the waveforms at nodes D, Q, X, Y. Use the clock as the trigger signal

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for observing these waveforms. Explain the waveforms and voltage levels.

- (4) Repeat (3) with the D input low (connect it to Gnd).
- (5) With the D input grounded, reduce the clock frequency until you see significant droop in the voltage at node Y. (This clock frequency should be on the order of 1kHz). Continue to decrease the clock frequency until the droop is large enough to cause 'glitches' in the Q output. Sketch the CLK, Y and Q waveforms.
- (6) Change C at node X and Y from 1000pF to 100pF. Record the clock frequency at which significant droop appears at node Y (and glitches appear in the Q output). Repeat this measurement with C = 10pF.

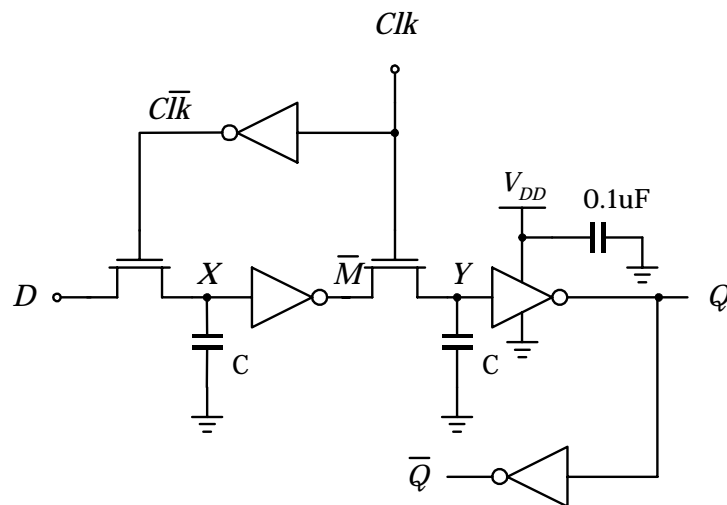


Figure 1.

III. STATIC MASTER-SLAVE FLIP-FLOP

- (1) Add the extra circuitry shown in Figure 2 that will convert the dynamic master-slave latch in Figure 1 to a static master-slave latch. Remember to connect pin 14 of CD4007 to +15V and pin 7 to Gnd.
- (2) Verify that the circuit operates as a master-slave latch by connecting the D input to the \bar{Q} output. Use a 10kHz square-wave that goes from 0 to 10V for the clock (CLK). Use C = 1000p. Sketch the CLK, \bar{M} and Q waveforms and measure the delay between the rising edge of the clock and output Q. At what part of the clock waveform is the D input latched? Increase the CLK frequency and measure the delay between the rising edge of the clock and output Q at each CLK frequency. At what CLK frequency the master-slave latch fail?

- (3) Tie the D input low. Use $C = 1000\text{pF}$. Slow the clock to the same frequency recorded in Step (5) above. Do you see droop at node Y? Try a lower frequency. Do you see droop at node Y? Try $C = 10\text{pF}$. Do you see droop at node Y? Why or why not?
- (4) What are the advantages and disadvantages of the static master-slave latch?

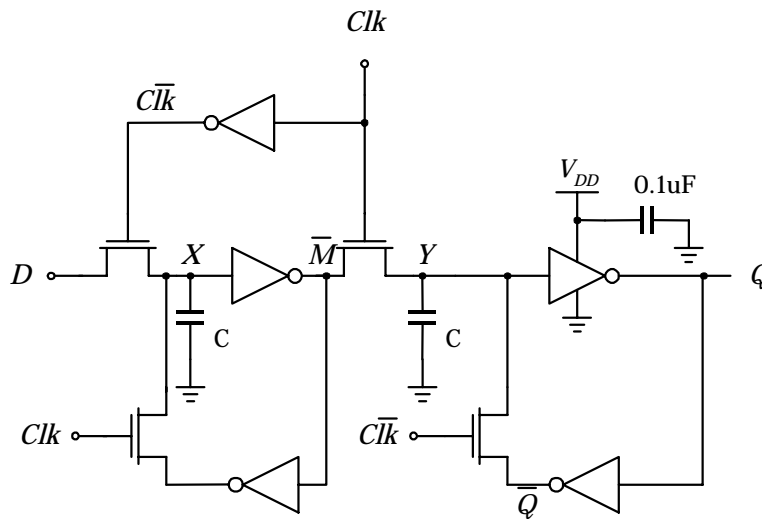


Figure 2.