University of California, Davis
College of Engineering
Department of Electrical and Computer Engineering

EEC 118 EXPERIMENT No. 2
NMOS and PMOS TRANSISTOR PARAMETERS *

I. OBJECTIVE

The objective of this experiment is to determine the electrical parameters of NMOS and PMOS transistors made with a standard metal-gate CMOS process. These parameters will be used for hand calculations of circuit characteristics in later experiments.

II. PRELAB

Before coming to the laboratory, study chapter 2 in textbook to learn the definitions of threshold voltage V_T, device transconductance parameter κ, body coefficient γ, and output conductance parameter λ. Also read "Input protection of MOS Gates" at the end of this lab.

Assumed Data:

Gate Oxide Capacitance C_{ox} = 35 nF/cm^2

$2\,|\phi_F| = 0.6V$

electron mobility μn = 580 cm^2 / V-s

hole mobility μp = 232 cm^2 / V-s

source-drain pn junctions are abru*pt junctions

III. TRANSISTOR PARAMETERS-MEASUREMENT AND CALCULATION

(1) Use the connections shown in Figure 1 to measure drain current I_D as a function of $V_{DS} = V_{GS}$ for V_{DS} = 3, 3.5, 4, 4.5, 5, 5.5, 6, and 6.5 Volts for

* Excerp from Paul Hurst et al's EEC118 Lab Manual, Spring 2001 – printed with Prof Hurst's permission

NMOS devices. Make these measurements at V_{SB} = 0, 2, and 5 Volts, making sure that the body is *negative* with respect to the source.

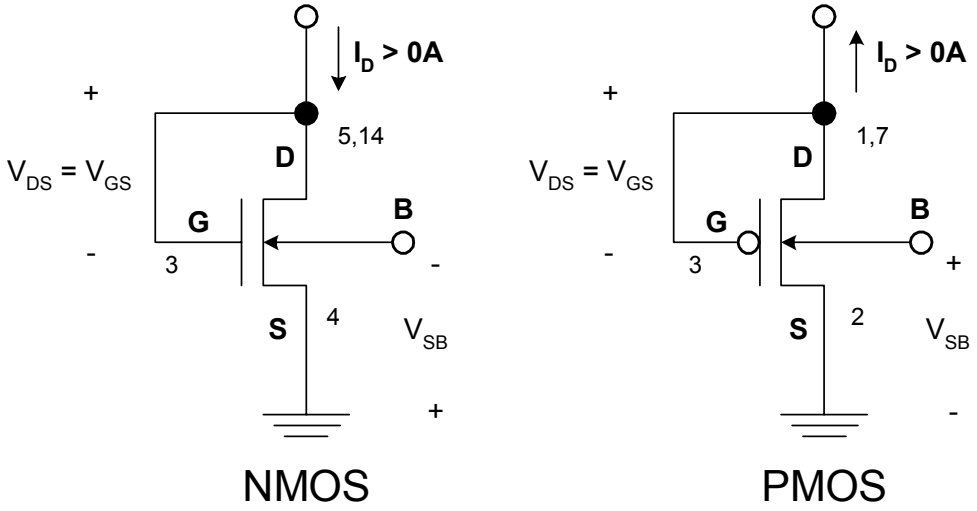

Figure 1.

(2) Repeat Step (1) for a PMOS device. Note that all polarities are reversed! The body is positive with respect to the source. Therefore, V_{DS} should be negative for all measurements.

(3) Plot $\sqrt{I_D}$ vs. $V_{GS} = V_{DS}$ for both devices at three values of body bias. Figure 2 shows sample plots. Draw the best-fit straight line through your data points. From intercepts, determine V_T for $|V_{BS}|$ = 0, 2 and 5 V for each device. From V_{BS} = 0V plot, determine the transconductance parameter $\kappa = \kappa' W/L$. Estimate W/L for both transistors.

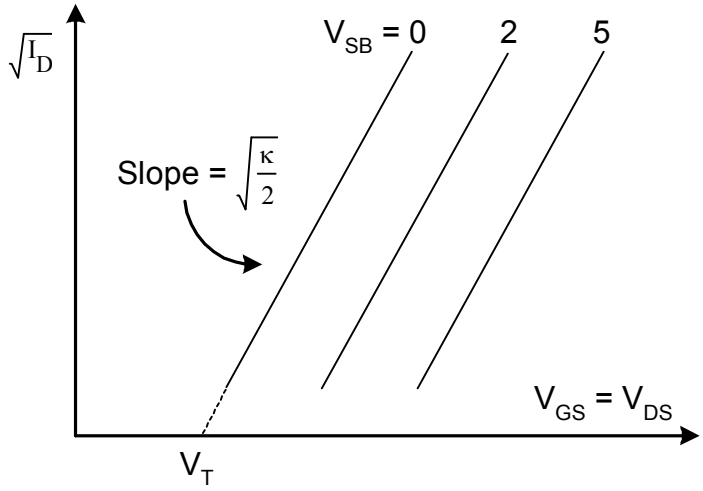

Figure 2.

(4) With V_{BS} = 0V and V_{GS} = 2.5V, measure drain current I_D at V_{DS} = 2, 2.5, 3, 3.5, 4, 4.5, 5, 5.5, and 6 Volts using the connections shown in Figure 3 for both NMOS and PMOS devices.

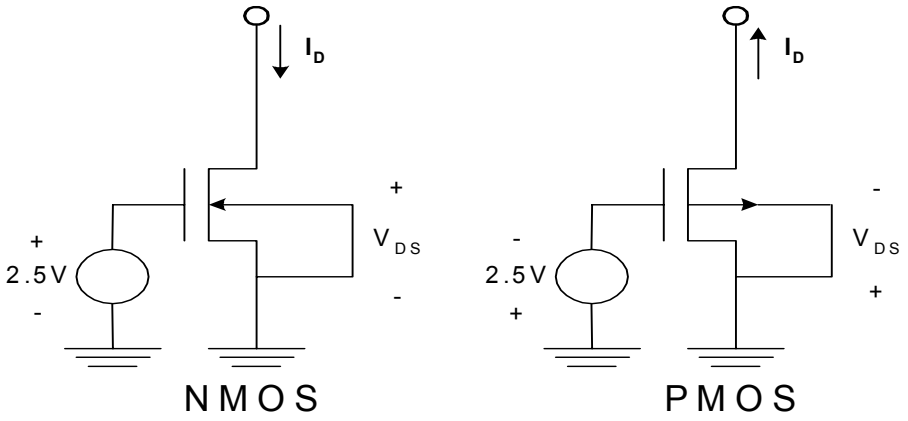

Figure 3.

(5) Using the data from parts (1) and (2), plot V_T vs. $\sqrt{|2\phi_F| + |V_{BS}|} - \sqrt{|2\phi_F|}$. Assuming $|2\phi_F| = 0.6V$ for both transistors, estimate γ_P and γ_N.

(6) Using your data from part (4), plot I_D vs. V_{DS} with V_{BS} = 0V for both devices and determine the channel length modulation factor, λ, from the slopes as shown in Figure 4.

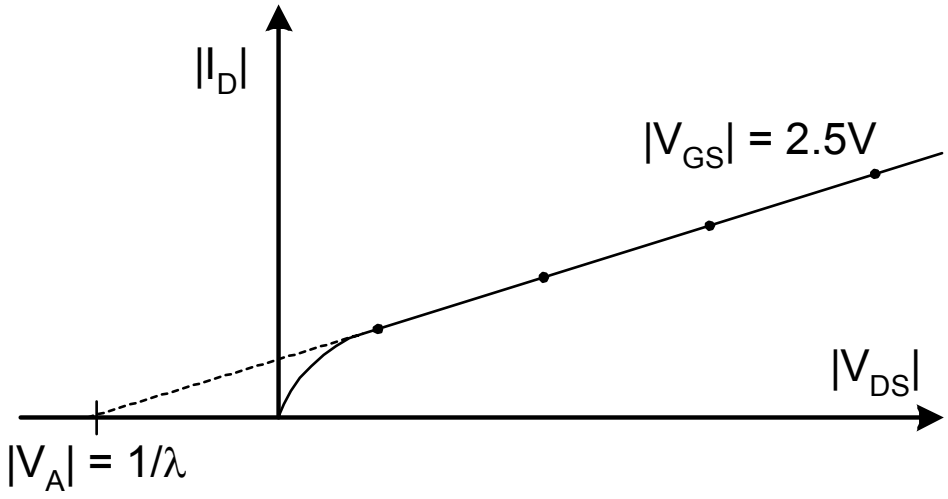

Figure 4.

(7) Use the curve tracer to plot I_D vs. V_{DS} for the NMOS transistor with $V_{BS} = 0$. Sketch the curves in your lab notebook for the region $0 \leq V_{GS} \leq 2.5V$ and $0 \leq V_{DS} \leq 5V$.

(8) Use the curve tracer to plot I_D vs. V_{GS} for the "diode-connected" NMOS transistor as shown in Figure 5. Sketch the curve in your notebook for $0 < V_{GS} < 10V$ with $V_{BS} = 0V$.

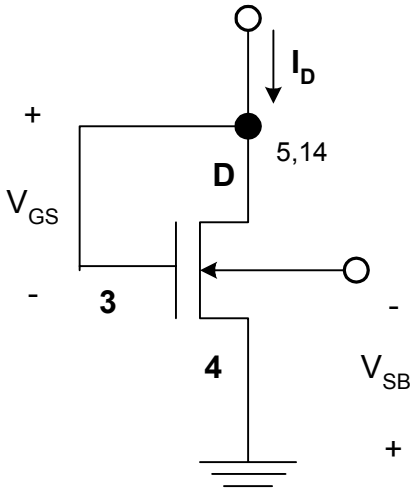

Figure 5.