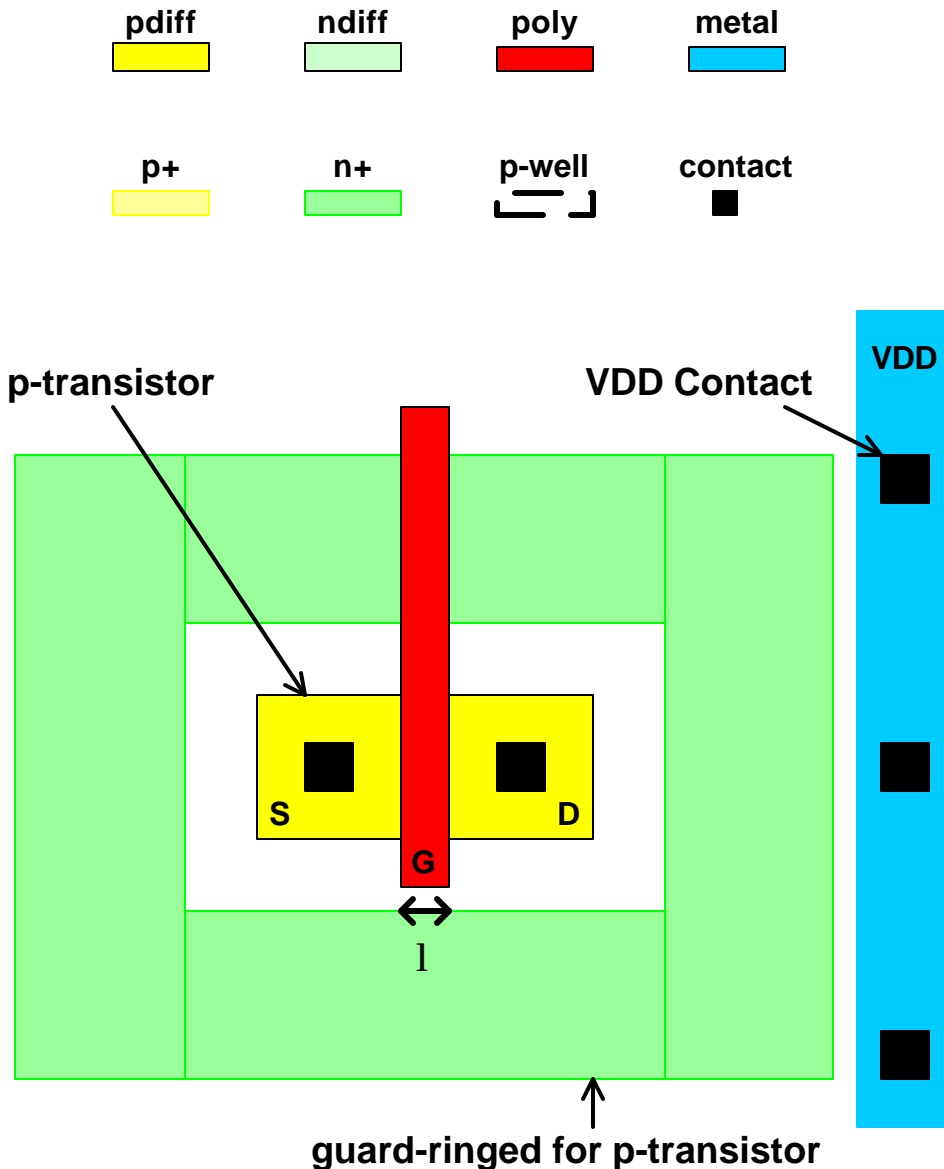
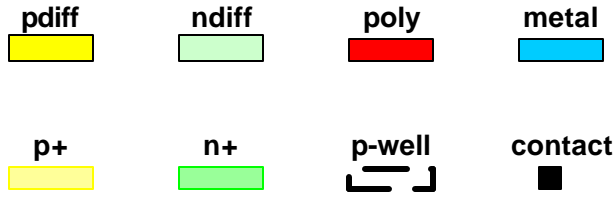


Homework Solution #3

Problem 3.8.1:

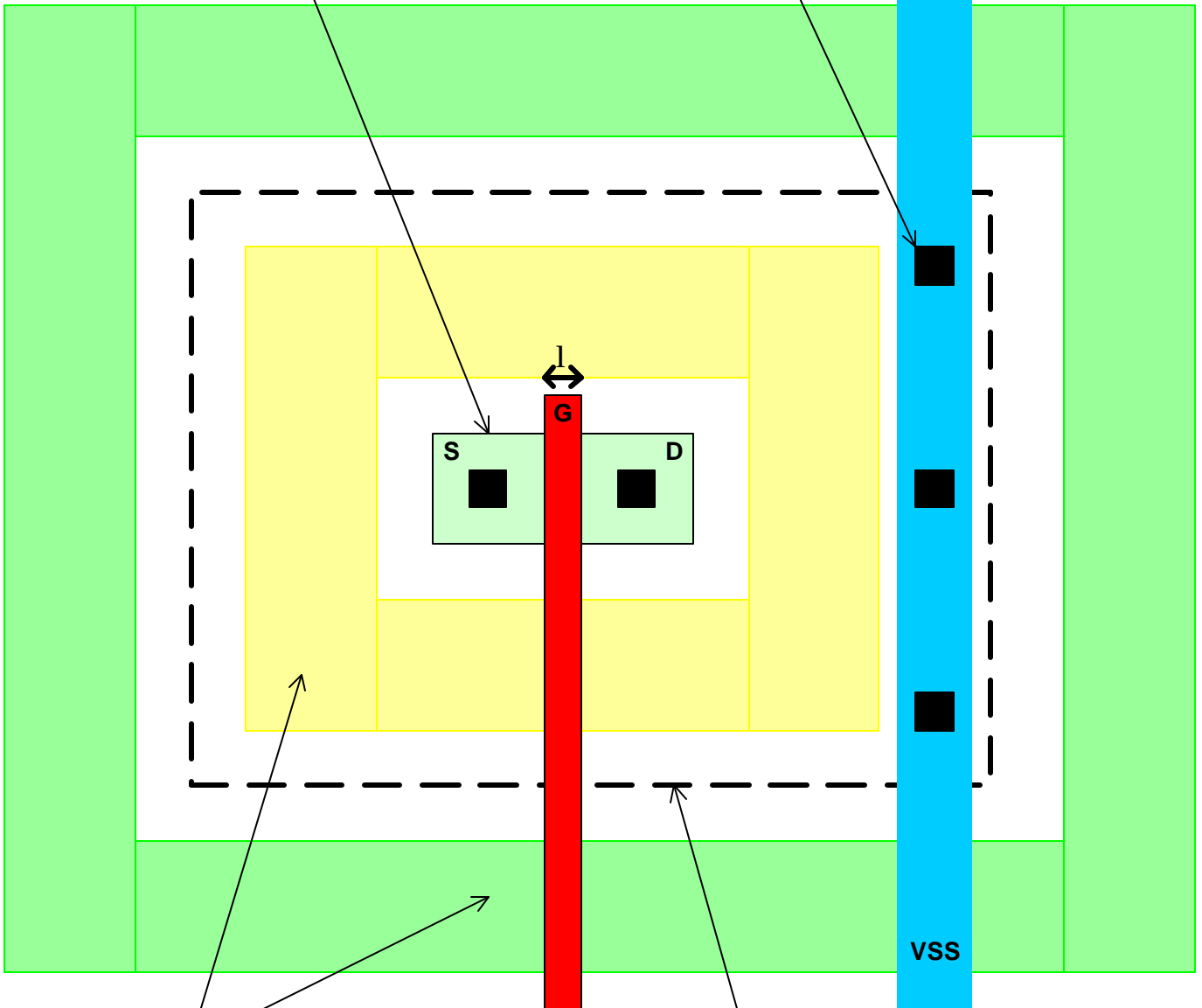
Note: in p-well process, the substrate is n-type.

- (1) VDD contact is needed for the substrate;
VSS contact is needed for the p-well
- (2) Double guard-ringed is applied to n-transistor



p-transistor

VSS Contact

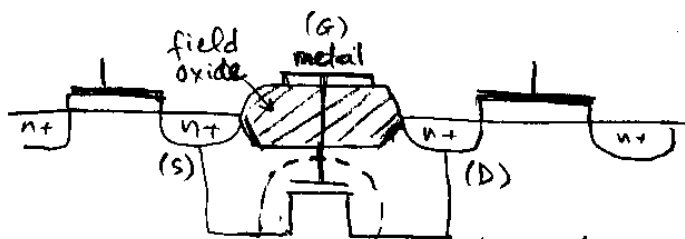


VSS

double guard-ringed for n-transistor

p-well

Problem 3.8.3:



Parasitic channel is reduced by changing its threshold voltage. That can be done by

- Increasing the thickness of field oxide,
- Increasing the impurity concentration under the field oxide

Problem 3.8.4:

A field transistor can be used to prevent overvoltage in a CMOS chip. It is done by controlling the threshold voltage of the field transistor such that the field transistor is ON when voltage exceeds a certain level. That allows the extra charge due to overvoltage to be dumped off the circuit.

Problem 3.8.5:

Substrate and well contacts are important.

- They ensure that the voltages of the substrate and the well are well established to eliminate the body-voltage variation which can affect circuit performance
- They also prevent latch-up when being placed next to potentially affected nodes.

Problem 3.8.6:

A "dummy collector" prevents latchup by reducing the current gain β of the parasitic BJT. It is done by capturing (or recombining) minority carriers and therefore reducing the amount of these carriers injected into the base of the BJT.

therefore reducing the amount of charge collected at the collector.

Problem 3.8.7:

A pull-up resistor for a pad is a p-transistor. It will potentially drive a lot of current and therefore will be subject to a lot of noise. Latchup can occur when this p-transistor couples to nearby n-transistors. So, latchup protection is needed.

With the same reasoning, latch-up protection is needed for the pull-down resistor as well.