Homework Solution # 2

Problem 2.1: Given $K_p = \mu \frac{\epsilon}{t_{ox}} = \mu \cdot \frac{\epsilon}{1.0 \times 10^{-7}} = 10\ \mu A/V^2$

For new $t_{ox} = 800\,\mathring{A}$, $K_p = \mu \cdot \frac{\epsilon}{8.0 \times 10^{-8}} = \mu \cdot \frac{\epsilon}{1.0 \times 10^{-7}} \cdot \left(\frac{1.0 \times 10^{-7}}{8.0 \times 10^{-8}}\right)$

$$= 1.25 \times 10 \mu A/V^2 = 12.5 \mu A/V^2$$

Therefore, the drain current of n- and p-transistors is increased by 25%.

Problem 2.2: The effective width and length of the transistor

$$W = 20 + (0.5 + 0.5) = 21\ \mu m$$
$$L = 5 - (1 + 1) - (0.5 + 0.5) = 2 \mu m$$

Then, $\beta = K_p \cdot \left(\frac{W}{L}\right) = (15 \mu A/V^2) \times \left(\frac{21 \mu m}{2 \mu m}\right) = 0.16 mA/V^2$

β is increased by $\left(\frac{21}{2}\right) / \left(\frac{20}{5}\right) \simeq 2.6$ times

Problem 2.3: $I_{d,sat} = \frac{1}{2} \beta (V_{gs} - V_t)^2 (1 + \lambda V_{ds})$

$$g_{m(sat)} = \left.\frac{\partial I_d}{\partial V_{gs}}\right|_{V_{ds} = const.} = \beta (V_{gs} - V_t)(1 + \lambda \cdot V_{ds})$$

Assume $V_{gd} = 0$ or $V_{gs} = V_{ds}$,

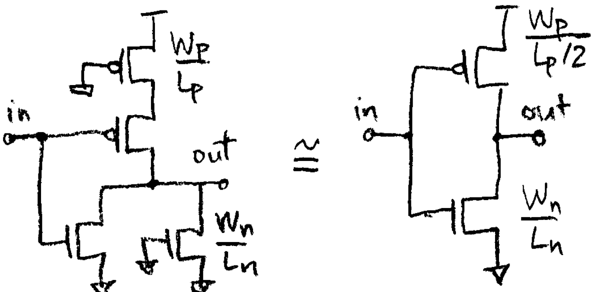
$$g_{m(sat)} = (40\ \mu A/V^2)(5V - 1V)(1 + 0.03 \times 5)$$
$$= 184 \mu A/V$$

Problem 2.4: Input switching voltages refer to V_{IL} and V_{IH}

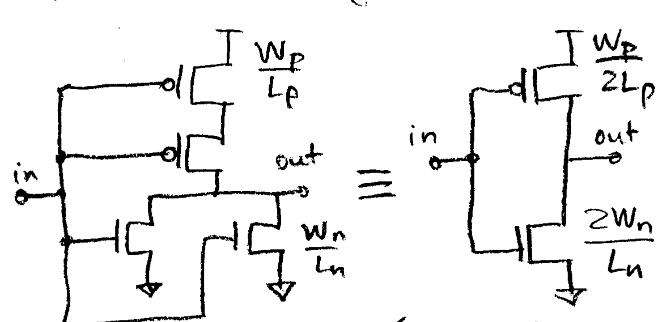
For inverters, these voltages can be found using equations (2.23) and (2.27) in textbook and $\frac{dV_{out}}{dV_{in}} = -1$. (Figure 2.17, textbook)

If no solution exists for a switching voltage, it can be found from equation (2.24).

For 2-input NOR gate, there are 2 possible switching scenarios.



Case A: $k = \dfrac{K_n (W_n/L_n)}{K_p (W_p/2L_p)} = 2$



Case B: $k = \dfrac{K_n (2W_n/L_n)}{K_p (W_p/2L_p)} = 4.$

Assume PMOS and NMOS are identically sized such that $\beta_p = \beta_n$.
That is, $K_p \left(\frac{W_p}{L_p}\right) = K_n \left(\frac{W_n}{L_n}\right)$.

(a) V_{IH}:

Using equation (2.27) and solving for $\left.\dfrac{dV_{out}}{dV_{in}}\right|_{V_{in}=V_{IH}} = -1$,
you'll get

$$4\left[(V_{IH} - V_{tn})^2 - \frac{1}{k}\cdot(V_{IH} - V_{DD} - V_{tp})^2\right] = \left[(V_{IH} - V_{tn}) - \frac{1}{k}(V_{IH} - V_{DD} - V_{tp})\right]^2$$

(b) V_{IL}:

Using equation (2.23) and solving for $\left.\dfrac{dV_{out}}{dV_{in}}\right|_{V_{in}=V_{IL}} = -1$,
you'll get

$$4\left[(V_{IL} - V_{tp})^2 - 2\left(V_{IL} - \frac{V_{DD}}{2} - V_{tp}\right)V_{DD} - k(V_{IL} - V_{tn})^2\right] =$$
$$= \left[(V_{IL} - V_{tp}) - V_{DD} - k(V_{IL} - V_{tn})\right]^2$$

To illustrate the effect of switching scenarios on V_{IH} and V_{IL}, I'll assume $V_{DD} = 5V$, $V_{tn} = -V_{tp} = 1V$.

- case A: $V_{IL} = 1.8V$; $V_{IH} = 3.0V \Rightarrow NM_L = 1.8V$; $NM_H = 2V$
- case B: $V_{IL} = 1.5V$; $V_{IH} = 2.7V \Rightarrow NM_L = 1.5V$; $NM_H = 2.3V$
- Worst case noise margins: $NM_L = \min(1.8V, 1.5V) = 1.5V$
  $NM_H = \min(2V, 2.3V) = 2V$

Noise margins are reduced in multi-input gates.