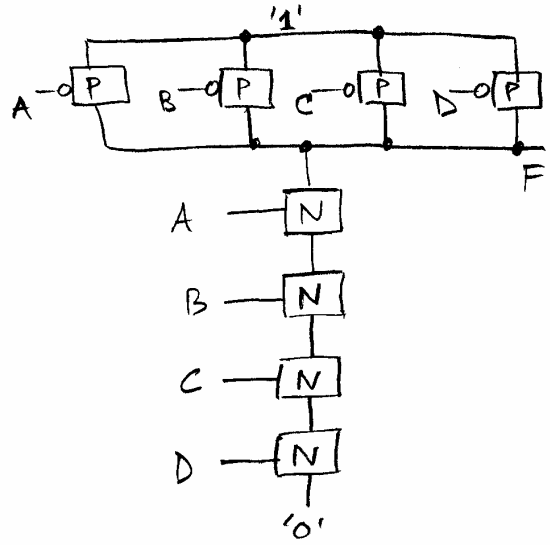
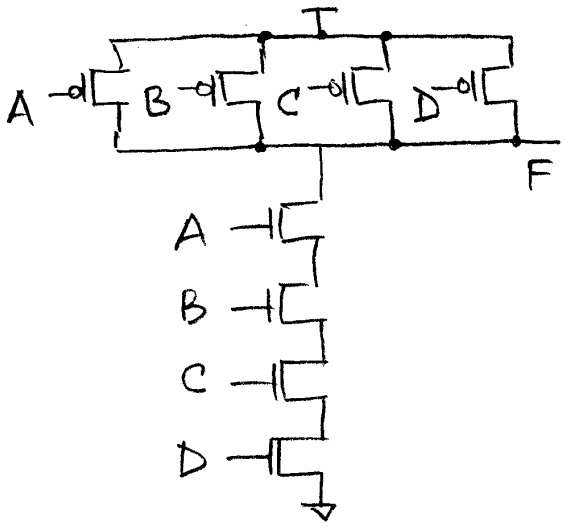
EEC118
SPRING '03

Homework # 1 Solution

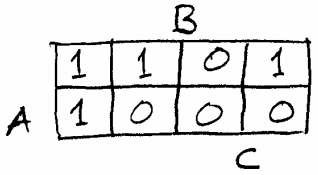
Problem 1.1 4-input NAND gate, $F = \overline{A \cdot B \cdot C \cdot D}$



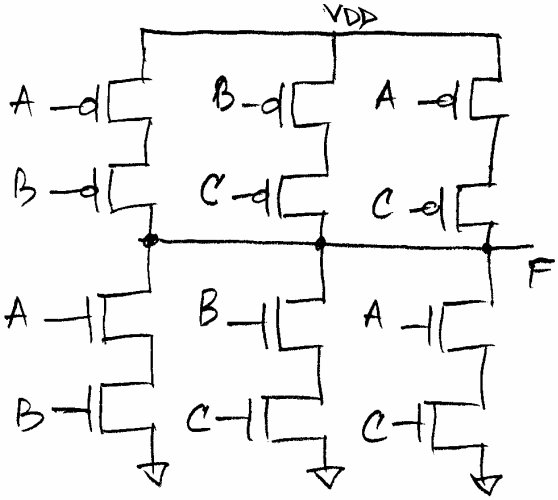


Problem 1.2: $F = \overline{AB + BC + AC}$

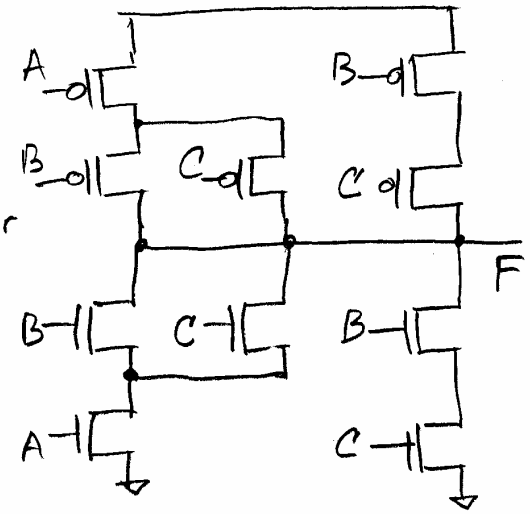
It's best to use Karnaugh map.



- Logic for NMOS = $AB + BC + AC$
- Logic for PMOS = $\bar{A}\bar{B} + \bar{B}\bar{C} + \bar{A}\bar{C}$



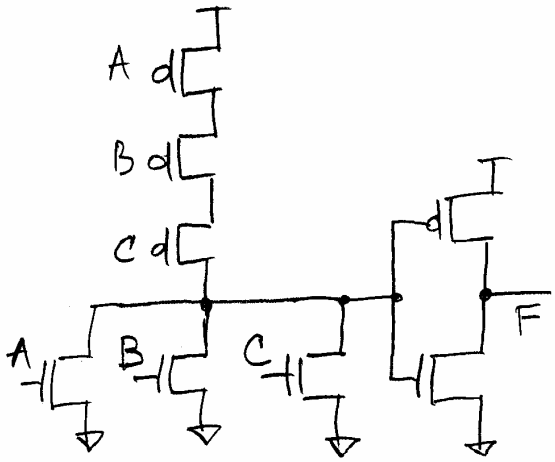
or



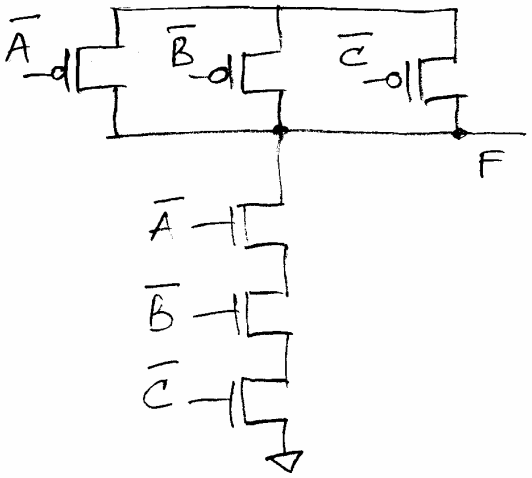
Problem 1.3: 3-input OR gate.

$$F = A + B + C = \overline{\overline{A + B + C}} = \overline{\bar{A} \cdot \bar{B} \cdot \bar{C}}$$

Two possible implementations.



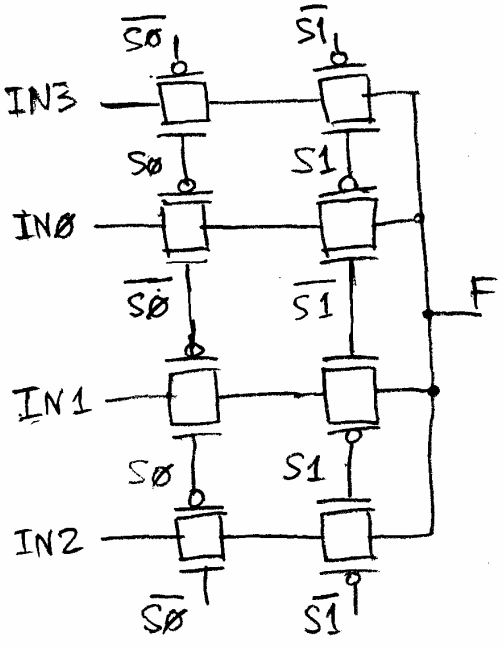
Straight-forward; bad high-PMOS stack

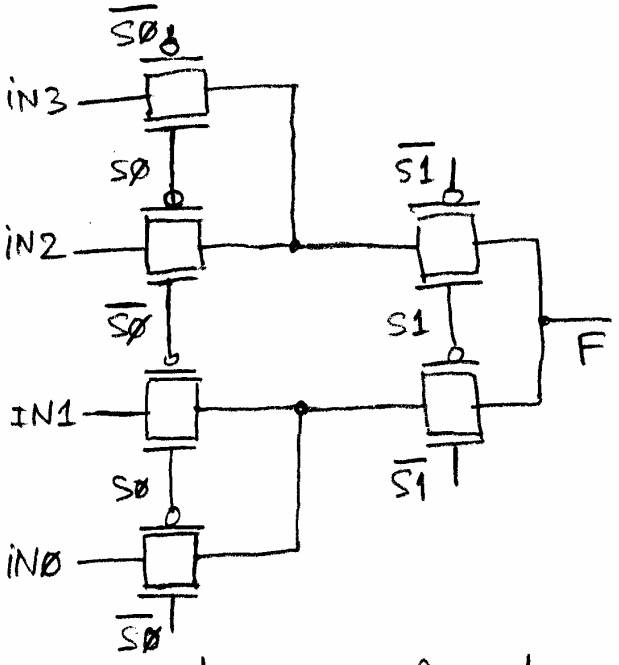


Simple circuit; need inverting input

Problem 1.4: 4-input multiplexer

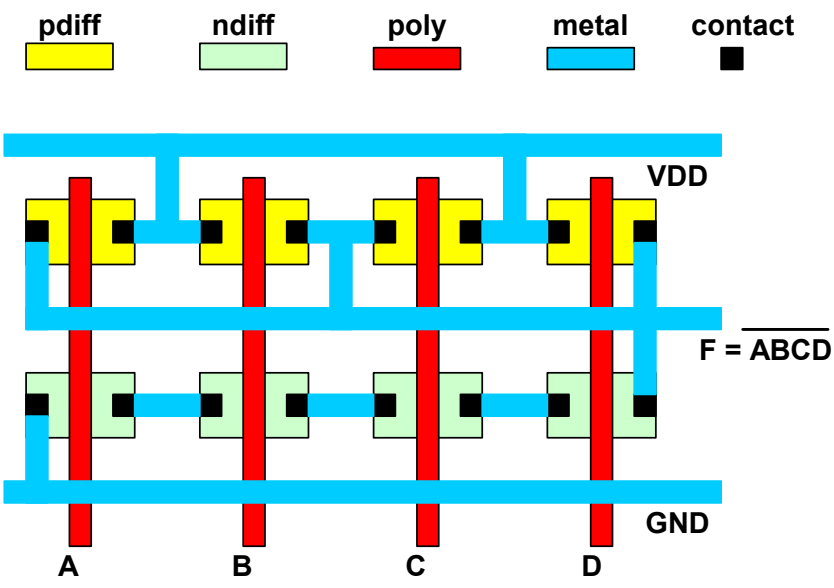
You can use one 4:1 MUX or three 2:1 MUX's.



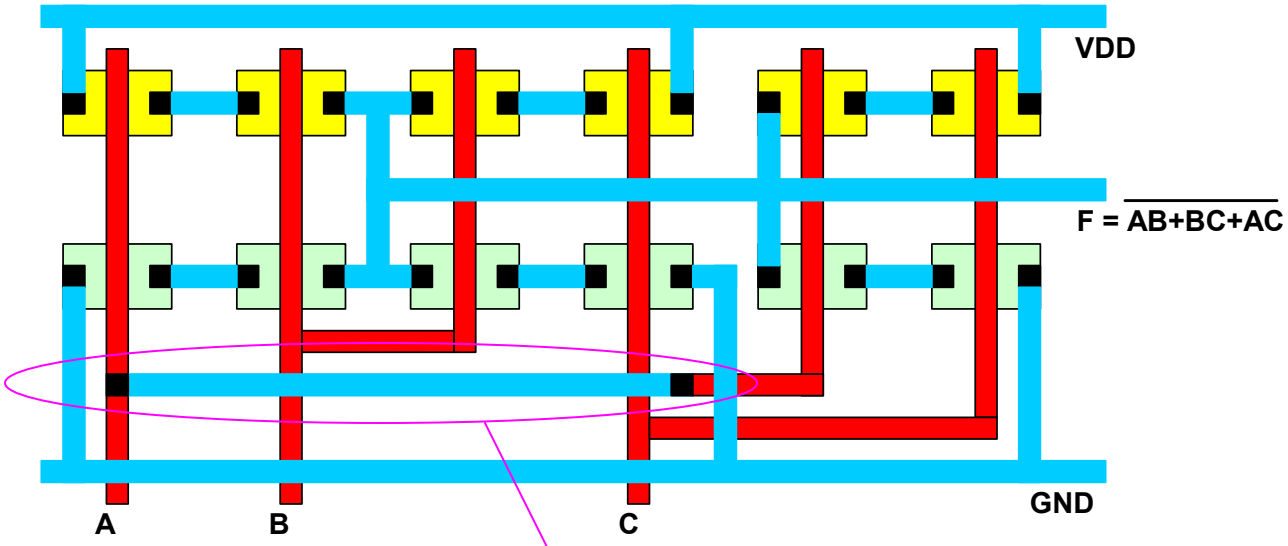


Preferred, using less transistors

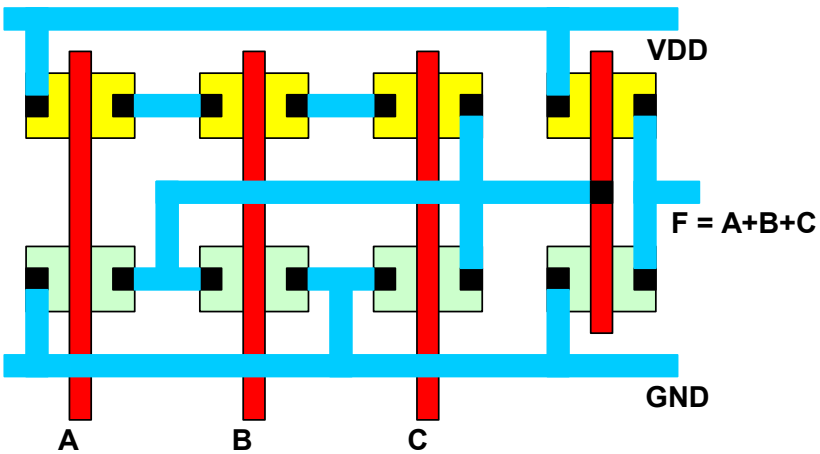
Problem 1.5



In layout, lines of same material cannot cross. You will face that often in your layout. The common solution is to switch to a different material over the crossing to eliminate it.



Solution to crossing wires



Problem 1.6. S-R latch