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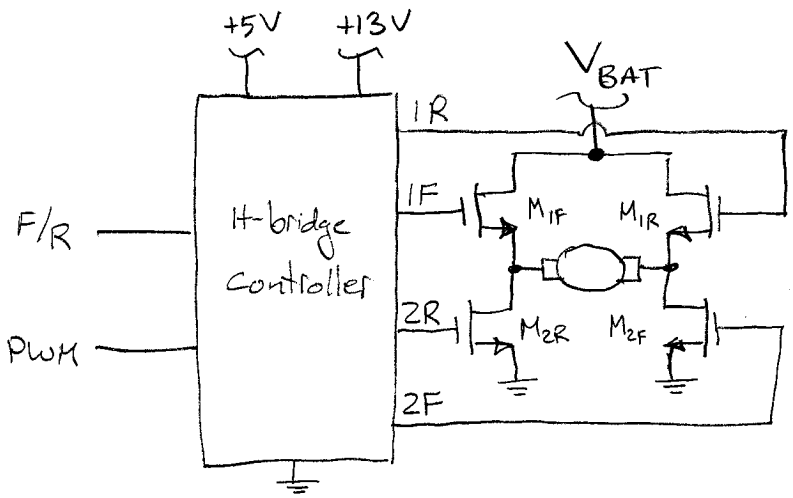
The circuit uses two inputs;

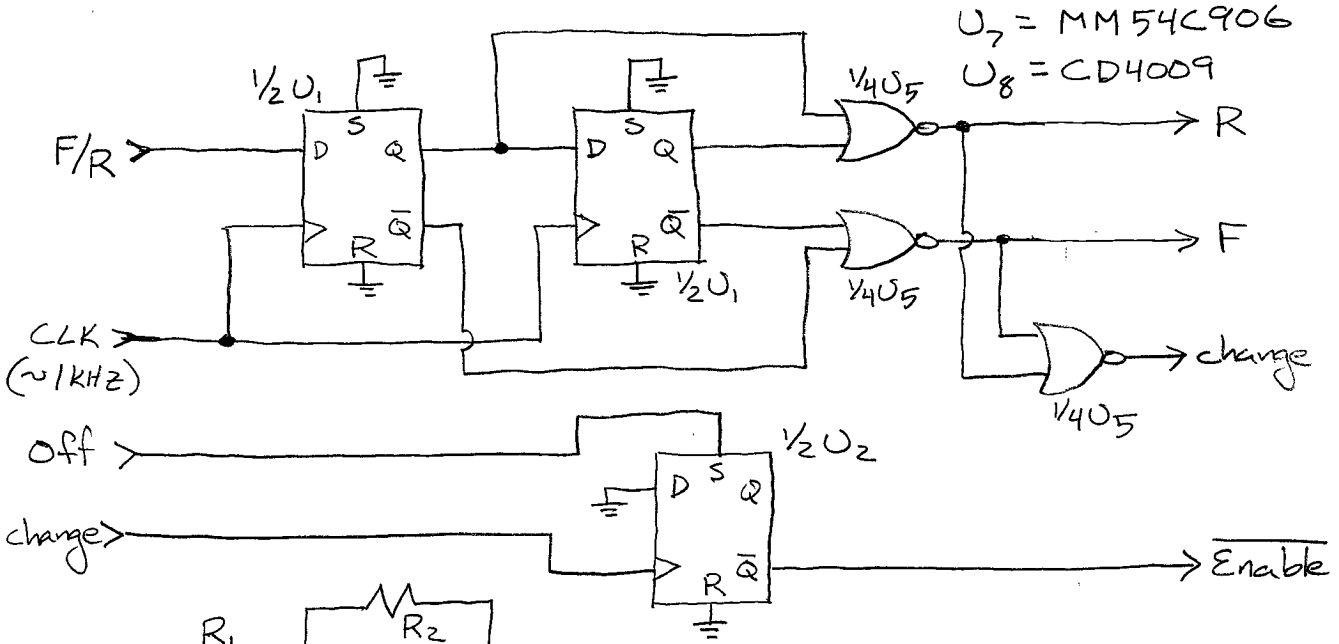
1) PWM – the same PWM signal that you use for a single NMOS drive
2) F/R – (forward/reverse) a CMOS compatible logic signal, 1 ⇒ forward, 0 ⇒ reverse

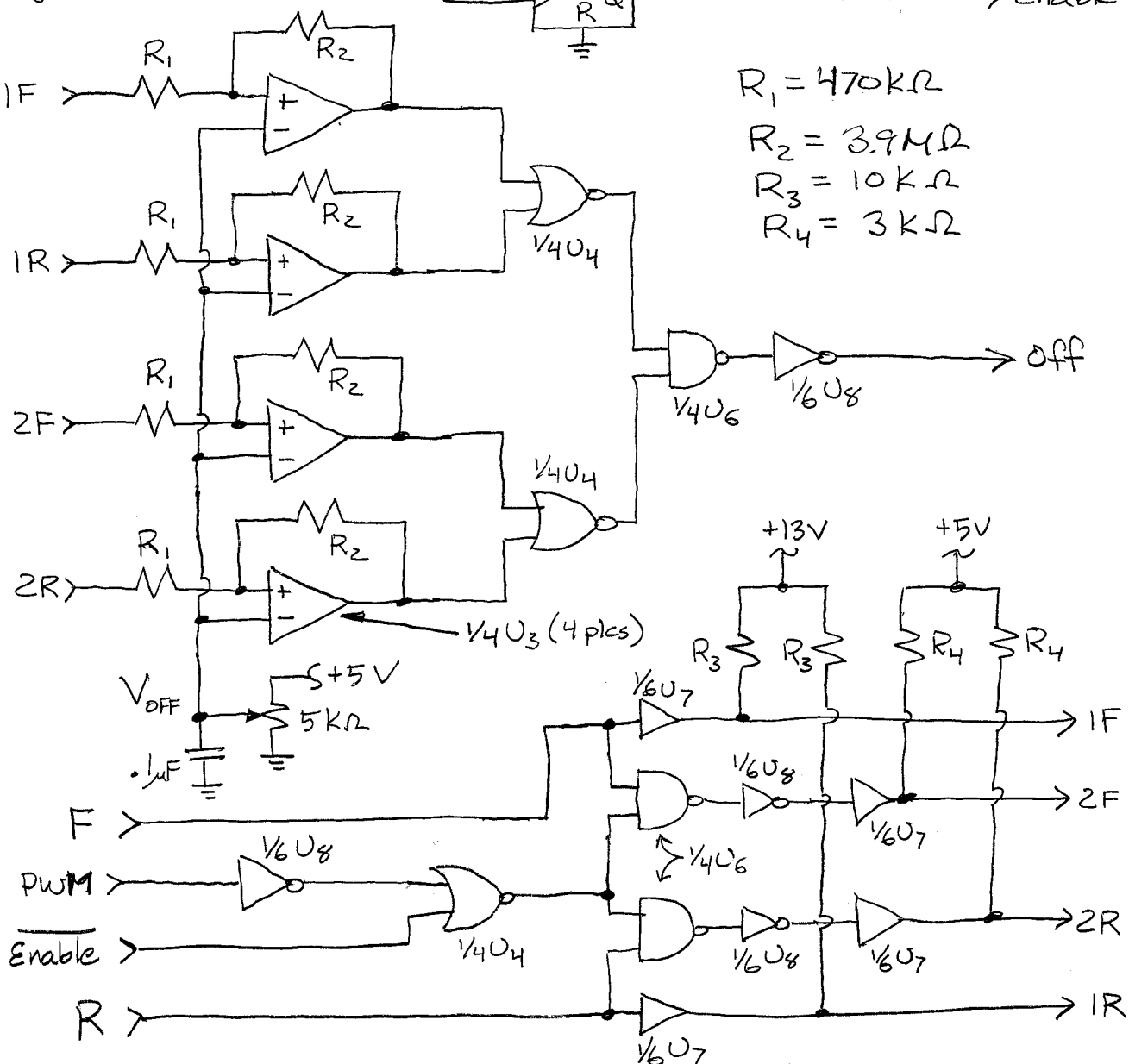
The circuit has four outputs to connect to the bridge:



The schematic is on page 2. V_{OFF} should be set to about 1V, which causes the hysteretical comparators' thresholds to be about 0.52V & 1.12V. When the gates of all MOSFETs are < 0.52V, 'OFF' will be high, signifying that the bridge is off and it is safe to change directions if desired. The flip-flops are clocked at 1KHz and keep track of the present and previous states of F/R.

U_1 & U_2 = CD4013, U_3 = LM6484, U_4 & U_5 = CD4001, U_6 = CD4011,
U_7 = MM54C906
U_8 = CD4009





R_1 = 470kΩ
R_2 = 3.9MΩ
R_3 = 10kΩ
R_4 = 3kΩ

This circuit has not been tested

The two flip flops driven by F/R are used to

1) deglitch the F/R signal
2) ensure that F & R are turned off and the PWM output is disabled until the H-bridge is off.

The four comparators with hysteresis are used to check whether the H bridge is off or not. If you switch from F to R (or vice versa) without ensuring the bridge is off, you may turn on M_{1F} and M_{2R} or M_{1R} and M_{2F} simultaneously, which destroys the bridge.

The open-drain buffers (U7) drive the bridge transistors. The top transistors are either off or on and the bottom ones are pulse-width modulated. You can't set the PWM frequency too high or the gates won't be able to switch fast enough. About 5-6 kHz is good.

The +13 V supply was chosen as a compromise between being sure M_{1F} & M_{1R} can be fully on when V_{BAT} is high (~ 8V) and not breaking down the gate oxides when the car is going slow and the back emf in the motor is low ($V_{GS\,max} = 10V$).