UC DAVIS

Electronic Circuits – Course Outline

EEC110A CRN: 61535 Professor Spencer
Spring 2010 2041 Kemper Hall
Lecture: MW 10:00-11:15, 1062 Bainer 752-6885
Discussion Section: MW 11:25-11:50, 1062 Bainer
Office hours: Wednesdays, 1-3 in 2041 Kemper Hall

TA: Travis Kleeburg – office hours: Fridays 1-3 in 2101 Kemper (tklee@ucdavis.edu)

Please do NOT use email to contact me unless it is necessary (i.e., don't use it in place of questions in class, the discussion session and office hours). My email address is: spencer@ece.ucdavis.edu

Required Text: R. Spencer and M. Ghausi, *Introduction to Electronic Circuit Design*, Prentice Hall, 2003 **Be sure to look at the book errata on the website: www.prenhall.com/spencer**

Optional References:

(If you are planning to continue taking courses in circuits and want to get familiar with SPICE, the following books are recommended. You will *NOT* need them for this course, although you are encouraged to use PSPICE on your own!)

A. Vladimirescu, *The SPICE Book*, New York: John Wiley & Sons, 1994 (this is a good overall reference. It describes the history of SPICE, how it works and how to use it. It does have some annoying minor errors in the modeling section though!)

B. Al-Hashimi, *The Art of Simulation Using PSPICE, Analog and Digital*, 1995, CRC Press (A good reference on how to use PSPICE. Includes many advanced features like behavioral modeling and Monte-Carlo analysis, but does not discuss device modeling at all.)

Prerequisite: EEC100 & 140A (may be taken concurrently)

Homework: Assignments will be posted on the course website each week and will indicate when they are due (it will usually, if not always, be Friday afternoon). Homework should be put in the box in Room 2131 in Kemper Hall unless specified otherwise. Late homework will be accepted the day after it was due if there is a *good* reason (be prepared to supply documentation), it will not be accepted after that except in *extraordinary* cases. Late homework *must* be handed in to Prof. Spencer. Homework solutions will be available on the course website (when you click on the links to view solutions you will be required to login, the user name is eec110a and the password is analogrules, both are case sensitive). You may collaborate on HW assignments, but each student must hand in his or her own assignment.

Homework problems will be graded on a four-level scale; 0 = little, if anything, done, 1 = sloppy and/or a number of mistakes, 2 = basically correct, but somewhat sloppy and/or minor mistakes, 3 = easy to follow and completely correct. **Format:** All homework should be done on standard 8 1/2"x11" paper, stapled together, *not* folded, and should have your name (last name first, *please*) and the assignment number. Be sure to put your name *as it appears on UC transcripts and class lists*!

Grading: There will be one 75-minute midterm, and a two-hour final exam. Both exams will be closed book and closed notes and calculators will *not* be allowed. You will be provided with a formula sheet for each exam. A copy of the formula sheet will be available for you to use when studying. I will report any instances of attempted cheating to Student Judicial Affairs.

The final course grade will be based on the following weighting: Homework 15%, Midterm 35%, Final 50%. **Any disagreements about homework or exam scores must be brought to the attention of Prof. Spencer within one week of the assignment in question being handing back, otherwise, the score stands.**

Electronic Circuits Class Schedule – Spring 2010

Date		Day	Topic	Reading[1]
Mar.	29	M	Introduction. The design process. Analysis for design.	Chap. 1
	31	W	Small-signal approximation and analysis. Review two-port models. Amplifier models. DC bias models (large-signal DC models) and analyses for BJTs.	Chap. 6, Chap. 7 up through §7.1.4, and §7.2.1
Apr.	5	M	Finish BJT biasing. Low-frequency small-signal (LFSS) BJT model.	Chap. 8 up through §8.1.5
	7	W	Finish LFSS BJT model. Start LFSS circuit analysis.	§8.2.1-8.2.2
	12	M	LFSS circuit analysis – gain (CE) stage.	
	14	W	Finish CE stage. Buffer stages (CC & CB – focus mostly on CC).	§8.3.1-8.3.2, §8.4.1-8.4.2
	19	M	Finish buffer stages. Start high-frequency small-signal (HFSS) diode and transistor models.	Chap. 9 up through §9.1.5
	21	W	Finish HFSS diode and transistor models including $\beta(j\omega)$ and f_T.	

[1] All reading assignments refer to the required text and should be completed *before* the lecture they are listed next to (except for the first lecture of course).

	26	M	Miller effect and approximate bandwidth of the CE stage (CC stage as time permits).	§9.2.1-9.2.2 & §9.3.1-9.3.2 ("Introductory Treatment" only!)
	28	W	Begin Negative Feedback (NFB): basic concept, advantages and characteristics.	§10.1-10.1.2 (The material on noise and feedback is optional. You may also want to review Asides A1.1 and §6.5.1)
May	3	M	**Midterm** (covers material up through lecture on 4/26)	
	5	W	NFB: Ideal analysis, classification.	
	10	M	NFB: Practical analysis, series-shunt.	§10.1.3 (up to the Series-Series Connection on page 698)
	12	W	NFB: Practical analysis, transistor-level series-shunt.	
	17	M	NFB: Practical analysis, other connections.	§10.1.3 (from page 698 on)
	19	W	NFB: Loop gain and stability, gain and phase margins.	§10.1.5
	24	M	NFB: Compensation.	§10.1.6
	26	W	**Start Digital** material: Introduction to digital circuits, Boolean algebra, binary logic gates. MOS device models for digital circuits.	Chap. 14 Introduction & §14.1; Chap. 15 Introduction & §15.1.3
	31	M	Inverter specifications & power dissipation. MOS inverter design.	§15.2-15.3.2
Jun.	2	W	Finish MOS inverters. CMOS logic gates; NOR, NAND, complex gates.	§15.3.3-15.3.5
	7	**M**	**8:00-10:00 AM Final Exam** (Comprehensive – but will emphasize material since midterm)	