University of California, Davis
Department of Electrical and Computer Engineering

EEC180B DIGITAL SYSTEMS II Spring 2006

LAB 2: HIERARCHICAL DESIGN IN VHDL

Objective

The objective of this lab is to illustrate the differences between structural and behavioral modeling in VHDL. You will design a basic cell using behavioral modeling and then "instantiate" and interconnect components at the top-level using structural modeling. In this lab, you will use ModelSim to simulate your design and then use Synplicity and Xilinx tools to synthesize, implement and test your hierarchical design.

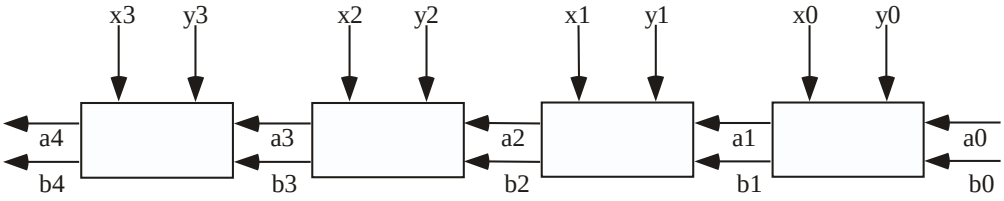
Pre-lab (10 points)

Complete step #1 of the Design Procedure section before your first lab session. You will turn in the pre-lab to be graded at your first lab session.

Problem Statement

This design problem is based on material from Fundamentals of Logic Design by Charles Roth, Jr. In the Fourth Edition of this book, see Section 17.2, p. 455-458. In the Fifth Edition, see Section 16.3, p 473-476. Get a copy of one of these books and read the appropriate section before attempting the lab. (These books will be on Reserve at Shields Library.)

Design an iterative network to compare two unsigned 4-bit binary numbers, $X = x_3x_2x_1x_0$ and $Y = y_3y_2y_1y_0$. The comparator must compare the least significant bits first so that inter-cell signals will propagate from right to left as shown in the block diagram below:



The circuit inside each of the four cells is identical. The output signals, a_i and b_i, give the status of the comparison after the previous cell, as defined in the table below.

a_i b_i	**Comparison of X and Y after previous cell**
0 0	X = Y
0 1	X > Y
1 0	X < Y

The a0 and b0 inputs to the right-most cell should be 00 since, by definition, the numbers X and Y are equal to the right of their least significant bits. Also, note that a_i and b_i cannot both be equal to 1 at the same time.

Input/Output Specifications

You will be implementing and testing your design on the Xilinx Spartan-3 board. The X and Y inputs will be generated using the eight slide switches, with the upper 4 switches representing X and the lower 4 switches representing Y.

$X = x_3x_2x_1x_0$: SW7 SW6 SW5 SW4
$Y = y_3y_2y_1y_0$: SW3 SW2 SW1 SW0

The output results will be displayed on the four seven-segment displays and also three LEDs. The four 7-segment displays will be designated from left to right as DISP3 downto DISP0. Similarly, the LEDs are labeled LED7 to LED0, going from left to right.

Display X and Y in hex on DISP3 and DISP0, respectively. You can use the hex_7seg function and modify the DISPLAY process from the Lab 1 tutorial code. Also, display the result of the comparison on the 7-segment displays and LEDs as follows:

If X > Y
- Turn on LED2
- Display ‘]’ signs on both DISP2 and DISP1 by turning on segments C, D and G.

If X = Y
- Turn on LED1
- Display equal signs on both DISP2 and DISP1 by turning on segments D and G.

If X < Y
- Turn on LED0
- Display ‘[’ signs on both DISP2 and DISP1 by turning on segments D, E and G.

Check the Spartan-3 Starter Kit Board User Guide, available on the course web page, for the appropriate pin assignments for the various I/O devices.

Design Procedure

1. Derive the Boolean equations for the logic inside a typical one-bit comparator cell. Use Karnaugh maps to minimize your output equations using the fact that $a_ib_i=11$ will never occur. Express your Boolean equations in VHDL to model a single cell. (This is one type of behavioral model.) The model must include an entity and architecture so that it can be instantiated as a component in a higher-level design.

2. Write the top-level structural model of the comparator using the basic cell component. Your top-level model must have 4 instantiations of the single-bit comparator cell as shown in the previous block diagram.

3. Simulate your design using ModelSim. Use the testbench from the Lab 1 tutorial as a template for your testbench. You can interactively assign values to X and Y and then simulate and verify that the outputs are correct.

   Demonstrate your simulation to your TA for verification. (30 points)

4. Synthesize and implement your design for the Xilinx Spartan-3 Board using the I/O assignments specified earlier.

5. Download your design to a Xilinx Spartan-3 Board and demonstrate your circuit to your TA. **Have your TA sign a verification sheet when your circuit works. (35 points)**

Lab report (25 points)

Submit the following items in your lab report:

- Verification sheets signed by your TA for simulation and synthesis verification.

- Simulation waveforms showing the correct functioning of your 4-bit comparator.

- Schematic diagram of your one-bit comparator cell generated by the Synplicity's Amplify tool. Print the RTL View of your one-bit comparator by opening the .srs output file in Amplify. Push down into one of your one-bit comparator instances and print the schematic to a Postscript file and then print the file.

- Answers to the following questions:

  1. Is it possible to design an 8-bit comparator using 4-bit comparators as components? If so, write the entity of the 4-bit comparator and show how the components would be instantiated in a top-level design. (The seven-segment display and LED output signals would not be included in the entity.)

  2. Does your 4-bit iterative comparator circuit work if the 4-bit numbers are interpreted as two's complement signed numbers (x_3 and y_3 bits are sign bits) rather than unsigned numbers? For a review of the two's complement number system, see Section 1.4 of Fundamentals of Logic Design, Fifth Edition, by Roth. Justify your answer. If your answer is no, redesign the most significant cell so that the comparator works for 4-bit signed inputs, if possible. Show your logic equation and circuit. (Note: this is a paper design only – you do not need to modify your VHDL code and simulate, synthesize and test.)