Spartan-3 FPGA Family: DC and Switching Characteristics

DS099-3 (v1.6) August 19, 2005

Preliminary Product Specification

DC Electrical Characteristics

In this section, specifications may be designated as Advance, Preliminary, or Production. These terms are defined as follows:

Advance: Initial estimates are based on simulation, early characterization, and/or extrapolation from the characteristics of other families. Values are subject to change. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur. Use as estimates, not for production.

Preliminary: Based on complete early silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reported delays is greatly reduced compared to Advance data. Use as estimates, not for production.

Production: These specifications are approved only after silicon has been characterized over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Parameter values are considered stable with no future changes expected.

Production-quality systems must only use FPGA designs compiled with a Production status speed file. FPGA designs using a less mature speed file designation should only be used during system prototyping or preproduction qualification. FPGA designs with speed files designated as Preview, Advance, or Preliminary should not be used in a production-quality system.

Whenever a speed file designation changes, as a device matures toward Production status, rerun the latest Xilinx ISE software on the FPGA design to ensure that the FPGA design incorporates the latest timing information and software updates.

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. **The following applies unless otherwise noted: The parameter values published in this module apply to all Spartan™-3 devices. AC and DC characteristics are specified using the same numbers for both commercial and industrial grades.** All parameters representing voltages are measured with respect to GND.

Some specifications list different values for one or more die or mask revisions, indicated by the device top marking.

If a particular Spartan-3 FPGA differs in functional behavior or electrical characteristic from this data sheet, those differences are described in a separate errata document. The errata notices for Spartan-3 FPGAs are living documents and are available online. Also, create a Xilinx MySupport user account and sign up for automatic E-mail notification whenever this data sheet or an errata notice is updated.

- **Spartan-3/Spartan-3L Errata Notices**
  www.xilinx.com/xlnx/xweb/xil_publications_display.jsp?category=-1210888
- **To Sign Up for Alerts on Xilinx MySupport**
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All specifications in this module also apply to the Spartan-3L family (the low-power version of the Spartan-3 family). Refer to the Spartan-3L datasheet (DS313) for any differences.

Table 1: **Absolute Maximum Ratings**

Symbol	Description	Conditions	Min	Max	Units
V_{CCINT}	Internal supply voltage relative to GND		–0.5	1.32	V
V_{CCAUX}	Auxiliary supply voltage relative to GND		–0.5	3.00	V
V_{CCO}	Output driver supply voltage relative to GND		–0.5	3.75	V
V_{REF}	Input reference voltage relative to GND		–0.5	V_{CCO} + 0.5(3)	V
V_{IN}(2)	Voltage applied to all User I/O pins and Dual-Purpose pins relative to GND	Driver in a high-impedance state	–0.5	V_{CCO} + 0.5(3)	V
	Voltage applied to all Dedicated pins relative to GND		–0.5	V_{CCAUX} + 0.5(4)	V

Table 1: **Absolute Maximum Ratings *(Continued)***

Symbol	Description	Conditions		Min	Max	Units
V_{ESD}	Electrostatic Discharge Voltage pins relative to GND	Human body model	XC3S50	-	±1500	V
			Other	-	±2000	V
		Charged device model		-	±500	V
		Machine model		-	±200	V
T_J	Junction temperature			-	125	°C
T_{SOL}	Soldering temperature			-	220	°C
T_{STG}	Storage temperature			–65	150	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time adversely affects device reliability.
2. The V_{IN} limits apply to both the DC and AC components of signals. Simple application solutions are available that show how to handle overshoot/undershoot as well as achieve PCI compliance. Refer to the following application notes: "Virtex™-II Pro and Spartan-3 3.3V PCI Reference Design" (**XAPP653**) and "Using 3.3V I/O Guidelines in a Virtex-II Pro Design" (**XAPP659**).
3. All User I/O and Dual-Purpose pins (DIN/D0, D1–D7, CS_B, RDWR_B, BUSY/DOUT, and INIT_B) draw power from the V_{CCO} power rail of the associated bank. Meeting the V_{IN} max limit ensures that the internal diode junctions that exist between each of these pins and the V_{CCO} rail do not turn on. Table 5 specifies the V_{CCO} range used to determine the max limit. When V_{CCO} is at its maximum recommended operating level (3.45V), V_{IN} max is 3.95V. The maximum voltage that avoids oxide stress is V_{INX} = 4.05V. As long as the V_{IN} max specification is met, oxide stress is not possible.
4. All Dedicated pins (M0–M2, CCLK, PROG_B, DONE, HSWAP_EN, TCK, TDI, TDO, and TMS) draw power from the V_{CCAUX} rail (2.5V). Meeting the V_{IN} max limit ensures that the internal diode junctions that exist between each of these pins and the V_{CCAUX} rail do not turn on. Table 5 specifies the V_{CCAUX} range used to determine the max limit. When V_{CCAUX} is at its maximum recommended operating level (2.625V), V_{IN} max $\leq$ 3.125V. As long as the V_{IN} max specification is met, oxide stress is not possible. For information concerning the use of 3.3V signals, see the "3.3V-Tolerant Configuration Interface" section in **Module 2**.
5. For soldering guidelines, see "Device Packaging and Thermal Characteristics" (**UG112**) and "Implementation and Solder Reflow Guidelines for Pb-Free Packages" (**XAPP427**).

Table 2: **Supply Voltage Thresholds for Power-On Reset**

Symbol	Description	Min	Max	Units
V_{CCINTT}	Threshold for the V_{CCINT} supply	0.4	1.0	V
V_{CCAUXT}	Threshold for the V_{CCAUX} supply	0.8	2.0	V
V_{CCO4T}	Threshold for the V_{CCO} Bank 4 supply	0.4	1.0	V

Notes:

1. V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies may be applied in any order. When applying V_{CCINT} power before V_{CCAUX} power, the FPGA may draw a *surplus* current in addition to the quiescent current levels specified in Table 7. Applying V_{CCAUX} eliminates the surplus current. The FPGA does not use any of the surplus current for the power-on process. For this power sequence, make sure that regulators with foldback features will not shut down inadvertently.
2. To ensure successful power-on, V_{CCINT}, V_{CCO} Bank 4, and V_{CCAUX} supplies must rise through their respective threshold-voltage ranges with no dips at any point.
3. If a brown-out condition occurs where V_{CCAUX} or V_{CCINT} drops below the retention voltage indicated in Table 4, then V_{CCAUX} or V_{CCINT} must drop below the minimum power-on reset voltage in order to clear out the device configuration content.

Table 3: **Power Voltage Ramp Time Requirements**

Symbol	Description	Top Marking(2)	Device	Package	Min	Max	Units
T_{CCO}	V_{CCO} ramp time for all eight banks	Mask revisions 'A' through 'D'	XC3S50	All	No limit	-	ms
			XC3S200	FT and FG	0.6	-	ms
				Other	2.0	-	ms
			XC3S400	FT and FG	0.6	-	ms
				Other	2.0	-	ms
			XC3S1000	All	No limit	-	
			XC3S1500	All	0.6	-	ms
			XC3S2000	All	No limit	-	
			XC3S4000	All	0.6	-	ms
			XC3S5000	All	No limit	-	
		Mask revisions 'E' or later	All	All	No limit	-	
T_{CCINT}	V_{CCINT} ramp time, only if V_{CCINT} is last in three-rail power-on sequence	Devices with 'FQ' fabrication/process code not specifically ordered with SCD0961	All	All	No limit	500	µs
		Devices with 'GQ' fabrication/process code or parts ordered with SCD0961 or SCD0974(6)	All	All	No limit	-	

Notes:
1. If a limit exists, this specification is based on characterization.
2. The mask revision code appears on the device top marking. See "Package Marking" in **Module 1**.
3. The ramp time is measured from 10% to 90% of the full nominal voltage swing for all I/O standards.
4. For information on power-on current needs, see "Power-On Behavior" in **Module 2**.
5. Mask revision, fabrication, and process codes appear in "Package Marking" in **Module 1**. Devices ordered with SCD0961 are specially screened. Devices ordered with SCD0974 or with 'GQ' fabrication/process code are also described in **XCN05009**.
6. All Spartan-3 FPGAs ordered directly from Xilinx using standard part ordering codes (i.e., no special SCD codes) for delivery after 15-AUG-2005 automatically specify mask revision 'E' and the 'GQ' fabrication/process code. These devices are also **errata** free.

Table 4: **Power Voltage Levels Necessary for Preserving RAM Contents**

Symbol	Description	Min	Units
V_{DRINT}	V_{CCINT} level required to retain RAM data	1.0	V
V_{DRAUX}	V_{CCAUX} level required to retain RAM data	2.0	V

Notes:
1. RAM contents include data stored in CMOS configuration latches.
2. The level of the V_{CCO} supply has no effect on data retention.
3. If a brown-out condition occurs where V_{CCAUX} or V_{CCINT} drops below the retention voltage, then V_{CCAUX} or V_{CCINT} must drop below the minimum power-on reset voltage indicated in Table 2 in order to clear out the device configuration content.

Table 5: **General Recommended Operating Conditions**

Symbol	Description		Min	Nom	Max	Units
T_J	Junction temperature	Commercial	0	25	85	°C
		Industrial	–40	25	100	°C
V_{CCINT}	Internal supply voltage		1.140	1.200	1.260	V
V_{CCO} (1)	Output driver supply voltage		1.140	-	3.450	V
V_{CCAUX}	Auxiliary supply voltage		2.375	2.500	2.625	V
ΔV_{CCAUX} (2)	Voltage variance on V_{CCAUX} when using a DCM		-	-	10	mV/ms
V_{IN} (2)	Voltage applied to all User I/O pins and Dual-Purpose pins relative to GND	V_{CCO} = 3.3V	–0.3	-	3.75	V
		$V_{CCO} \leq$2.5V	–0.3	-	V_{CCO} + 0.3 (3)	V
	Voltage applied to all Dedicated pins relative to GND		–0.3	-	V_{CCAUX} + 0.3 (4)	V

Notes:
1. The V_{CCO} range given here spans the lowest and highest operating voltages of all supported I/O standards. The recommended V_{CCO} range specific to each of the single-ended I/O standards is given in Table 8, and that specific to the differential standards is given in Table 10.
2. Only during DCM operation is it recommended that the rate of change of V_{CCAUX} not exceed 10 mV/ms.

Table 6: **General DC Characteristics of User I/O, Dual-Purpose, and Dedicated Pins**

Symbol	Description	Test Conditions		Min	Typ	Max	Units
I_L (2)	Leakage current at User I/O, Dual-Purpose, and Dedicated pins	Driver is Hi-Z, V_{IN} = 0V or V_{CCO} max, sample-tested	$V_{CCO} \geq$ 3.0V	-	-	±25	µA
			V_{CCO} < 3.0V	-	-	±10	µA
I_{RPU} (3)	Current through pull-up resistor at User I/O, Dual-Purpose, and Dedicated pins	V_{IN} = 0V, V_{CCO} = 3.3V		–0.84	-	–2.35	mA
		V_{IN} = 0V, V_{CCO} = 3.0V		–0.69	-	–1.99	mA
		V_{IN} = 0V, V_{CCO} = 2.5V		–0.47	-	–1.41	mA
		V_{IN} = 0V, V_{CCO} = 1.8V		–0.21	-	–0.69	mA
		V_{IN} = 0V, V_{CCO} = 1.5V		–0.13	-	–0.43	mA
		V_{IN} = 0V, V_{CCO} = 1.2V		–0.06	-	–0.22	mA
R_{RPU} (3)	Equivalent resistance of pull-up resistor at User I/O, Dual-Purpose, and Dedicated pins, derived from I_{RPU}	V_{CCO} = 3.0V to 3.45V		1.27	-	4.11	kΩ
		V_{CCO} = 2.3V to 2.7V		1.15	-	3.25	kΩ
		V_{CCO} = 1.7V to 1.9V		2.45	-	9.10	kΩ
		V_{CCO} = 1.4V to 1.6V		3.25	-	12.10	kΩ
		V_{CCO} = 1.14 to 1.26V		5.15	-	21.00	kΩ
I_{RPD} (3)	Current through pull-down resistor at User I/O, Dual-Purpose, and Dedicated pins	$V_{IN} = V_{CCO}$		0.37	-	1.67	mA
R_{RPD} (3)	Equivalent resistance of pull-down resistor at User I/O, Dual-Purpose, and Dedicated pins, driven from I_{RPD}	V_{CCO} = 3.0V to 3.45V		1.75	-	9.35	kΩ
		V_{CCO} = 2.3V to 2.7V		1.35	-	7.30	kΩ
		V_{CCO} = 1.7V to 1.9V		1.00	-	5.15	kΩ
		V_{CCO} = 1.4V to 1.6V		0.85	-	4.35	kΩ
		V_{CCO} = 1.14 to 1.26V		0.68	-	3.45	kΩ
R_{DCI}	Value of external reference resistor to support DCI I/O standards			20	-	100	Ω

Table 6: **General DC Characteristics of User I/O, Dual-Purpose, and Dedicated Pins *(Continued)***

Symbol	Description	Test Conditions	Min	Typ	Max	Units
I_{REF}	V_{REF} current per pin	$V_{CCO} \geq 3.0V$	-	-	±25	µA
		$V_{CCO} < 3.0V$	-	-	±10	µA
C_{IN}	Input capacitance		3	-	10	pF

Notes:
1. The numbers in this table are based on the conditions set forth in Table 5.
2. The I_L specification applies to every I/O pin throughout power-on as long as the voltage on that pin stays between the absolute V_{IN} minimum and maximum values (Table 1). For hot-swap applications, at the time of card connection, be sure to keep all I/O voltages within this range before applying V_{CCO} power. Also consider applying V_{CCO} power before the connection of data lines occurs. When the FPGA is completely unpowered, the impedance at the I/O pins is high.
3. This parameter is based on characterization. The pull-up resistance $R_{PU} = V_{CCO} / I_{RPU}$. The pull-down resistance $R_{PD} = V_{IN} / I_{RPD}$. Spartan-3 family values for both resistances are stronger than they have been for previous FPGA families.

Table 7: **Quiescent Supply Current Characteristics**

Symbol	Description	Device	Typical(1)	Commercial Maximum(1)	Industrial Maximum(1)	Units
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XC3S50	5	30	50	mA
		XC3S200	10	80	125	mA
		XC3S400	15	115	180	mA
		XC3S1000	35	200	315	mA
		XC3S1500	45	260	410	mA
		XC3S2000	60	450	650	mA
		XC3S4000	100	810	1200	mA
		XC3S5000	120	990	1450	mA
I_{CCOQ}	Quiescent V_{CCO} supply current	XC3S50	1.5	10	12	mA
		XC3S200	1.5	10	12	mA
		XC3S400	1.5	12	14	mA
		XC3S1000	2.0	12	14	mA
		XC3S1500	2.5	14	16	mA
		XC3S2000	3.0	16	19	mA
		XC3S4000	3.5	18	22	mA
		XC3S5000	3.5	18	22	mA
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	XC3S50	7	20	22	mA
		XC3S200	10	30	33	mA
		XC3S400	15	40	44	mA
		XC3S1000	20	50	55	mA
		XC3S1500	35	75	85	mA
		XC3S2000	45	90	100	mA
		XC3S4000	55	110	125	mA
		XC3S5000	70	130	145	mA

Notes:

1. The numbers in this table are based on the conditions set forth in Table 5. Quiescent supply current is measured with all I/O drivers in a high-impedance state and with all pull-up/pull-down resistors at the I/O pads disabled. Typical values are characterized using devices with typical processing at ambient room temperature (T_A of 25°C at V_{CCINT} = 1.2V, V_{CCO} = 3.3V, and V_{CCAUX} = 2.5V). Maximum values are the production test limits measured for each device at the maximum specified junction temperature and at maximum voltage limits with V_{CCINT} = 1.26V, V_{CCO} = 3.45V, and V_{CCAUX} = 2.625V. The FPGA is programmed with a "blank" configuration data file (i.e., a design with no functional elements instantiated). For conditions other than those described above, (e.g., a design including functional elements, the use of DCI standards, etc.), measured quiescent current levels may be different than the values in the table. Use the Web Power Tool or XPower for more accurate estimates. See Note 2.
2. There are two recommended ways to estimate the total power consumption (quiescent plus dynamic) for a specific design: a) The Spartan-3 Web Power Tool at **http://www.xilinx.com/ise/power_tools** provides quick, approximate, typical estimates, and does not require a netlist of the design. b) XPower, part of the Xilinx ISE development software, uses the FPGA netlist as input to provide more accurate maximum and typical estimates.
3. The maximum numbers in this table also indicate the minimum current each power rail requires in order for the FPGA to power-on successfully, once all three rails are supplied. If V_{CCINT} is applied before V_{CCAUX}, there may be temporary additional I_{CCINT} current until V_{CCAUX} is applied. See "Surplus I_{CCINT} if V_{CCINT} Applied before V_{CCAUX}" in **Module 2**.
4. For reduced maximum quiescent current in power-sensitive applications, see the Spartan-3L Low Power FPGA Family (**DS313**).

Table 8: **Recommended Operating Conditions for User I/Os Using Single-Ended Standards**

Signal Standard (IOSTANDARD)	V_{CCO}			V_{REF}			V_{IL}	V_{IH}
	Min (V)	Nom (V)	Max (V)	Min (V)	Nom (V)	Max (V)	Max (V)	Min (V)
GTL(3)	-	-	-	0.74	0.8	0.86	V_{REF} - 0.05	V_{REF} + 0.05
GTL_DCI	-	1.2	-	0.74	0.8	0.86	V_{REF} - 0.05	V_{REF} + 0.05
GTLP(3)	-	-	-	0.88	1	1.12	V_{REF} - 0.1	V_{REF} + 0.1
GTLP_DCI	-	1.5	-	0.88	1	1.12	V_{REF} - 0.1	V_{REF} + 0.1
HSLVDCI_15	1.4	1.5	1.6	-	0.75	-	V_{REF} - 0.1	V_{REF} + 0.1
HSLVDCI_18	1.7	1.8	1.9	-	0.9	-	V_{REF} - 0.1	V_{REF} + 0.1
HSLVDCI_25	2.3	2.5	2.7	-	1.25	-	V_{REF} - 0.1	V_{REF} + 0.1
HSLVDCI_33	3.0	3.3	3.45	-	1.65	-	V_{REF} - 0.1	V_{REF} + 0.1
HSTL_I, HSTL_I_DCI	1.4	1.5	1.6	0.68	0.75	0.9	V_{REF} - 0.1	V_{REF} + 0.1
HSTL_III, HSTL_III_DCI	1.4	1.5	1.6	-	0.9	-	V_{REF} - 0.1	V_{REF} + 0.1
HSTL_I_18, HSTL_I_DCI_18	1.7	1.8	1.9	0.8	0.9	1.1	V_{REF} - 0.1	V_{REF} + 0.1
HSTL_II_18, HSTL_II_DCI_18	1.7	1.8	1.9	-	0.9	-	V_{REF} - 0.1	V_{REF} + 0.1
HSTL_III_18, HSTL_III_DCI_18	1.7	1.8	1.9	-	1.1	-	V_{REF} - 0.1	V_{REF} + 0.1
LVCMOS12(4)	1.14	1.2	1.3	-	-	-	$0.37V_{CCO}$	$0.58V_{CCO}$
LVCMOS15, LVDCI_15, LVDCI_DV2_15(4)	1.4	1.5	1.6	-	-	-	$0.30V_{CCO}$	$0.70V_{CCO}$
LVCMOS18, LVDCI_18, LVDCI_DV2_18(4)	1.7	1.8	1.9	-	-	-	$0.30V_{CCO}$	$0.70V_{CCO}$
LVCMOS25(4,5), LVDCI_25, LVDCI_DV2_25(4)	2.3	2.5	2.7	-	-	-	0.7	1.7
LVCMOS33, LVDCI_33, LVDCI_DV2_33(4)	3.0	3.3	3.45	-	-	-	0.8	2.0
LVTTL	3.0	3.3	3.45	-	-	-	0.8	2.0
PCI33_3(7)	-	3.0	-	-	-	-	$0.30V_{CCO}$	$0.50V_{CCO}$
SSTL18_I, SSTL18_I_DCI	1.7	1.8	1.9	0.833	0.900	0.969	V_{REF} - 0.125	V_{REF} + 0.125
SSTL18_II	1.7	1.8	1.9	0.833	0.900	0.969	V_{REF} - 0.125	V_{REF} + 0.125
SSTL2_I, SSTL2_I_DCI	2.3	2.5	2.7	1.15	1.25	1.35	V_{REF} - 0.15	V_{REF} + 0.15
SSTL2_II, SSTL2_II_DCI	2.3	2.5	2.7	1.15	1.25	1.35	V_{REF} - 0.15	V_{REF} + 0.15

Notes:
1. Descriptions of the symbols used in this table are as follows:
   V_{CCO} — the supply voltage for output drivers as well as LVCMOS, LVTTL, and PCI inputs
   V_{REF} — the reference voltage for setting the input switching threshold
   V_{IL} — the input voltage that indicates a Low logic level
   V_{IH} — the input voltage that indicates a High logic level
2. For device operation, the maximum signal voltage (V_{IH} max) may be as high as V_{IN} max. See Table 1.
3. Because the GTL and GTLP standards employ open-drain output buffers, V_{CCO} lines do not supply current to the I/O circuit, rather this current is provided using an external pull-up resistor connected from the I/O pin to a termination voltage (V_{TT}). Nevertheless, the voltage applied to the associated V_{CCO} lines must always be at or above V_{TT} and I/O pad voltages.
4. There is approximately 0 to 100 mV of hysteresis on inputs using any LVCMOS standard.
5. All Dedicated pins (M0-M2, CCLK, PROG_B, DONE, HSWAP_EN, TCK, TDI, TDO, and TMS) use the LVCMOS25 standard and draw power from the V_{CCAUX} rail (2.5V). The Dual-Purpose configuration pins (DIN/D0, D1-D7, CS_B, RDWR_B, BUSY/DOUT, and INIT_B) use the LVCMOS25 standard before the User mode. For these pins, apply 2.5V to the V_{CCO} Bank 4 and V_{CCO} Bank 5 rails at power-on as well as throughout configuration. For information concerning the use of 3.3V signals, see the "3.3V-Tolerant Configuration Interface" section in **Module 2**.
6. The Global Clock Inputs (GCLK0-GCLK7) are Dual-Purpose pins to which any signal standard may be assigned.
7. For more information, see "Virtex-II Pro and Spartan-3 3.3V PCI Reference Design" (**XAPP653**).

Table 9: **DC Characteristics of User I/Os Using Single-Ended Standards**

Signal Standard (IOSTANDARD) and Current Drive Attribute (mA)		Test Conditions		Logic Level Characteristics	
		I_{OL} (mA)	I_{OH} (mA)	V_{OL} Max (V)	V_{OH} Min (V)
GTL		32	-	0.4	-
GTL_DCI		Note 3	Note 3		
GTLP		36	-	0.6	-
GTLP_DCI		Note 3	Note 3		
HSLVDCI_15		Note 3	Note 3	0.4	V_{CCO} - 0.4
HSLVDCI_18					
HSLVDCI_25					
HSLVDCI_33					
HSTL_I		8	–8	0.4	V_{CCO} - 0.4
HSTL_I_DCI		Note 3	Note 3		
HSTL_III		24	–8	0.4	V_{CCO} - 0.4
HSTL_III_DCI		Note 3	Note 3		
HSTL_I_18		8	–8	0.4	V_{CCO} - 0.4
HSTL_I_DCI_18		Note 3	Note 3		
HSTL_II_18		16	–16	0.4	V_{CCO} - 0.4
HSTL_II_DCI_18		Note 3	Note 3		
HSTL_III_18		24	–8	0.4	V_{CCO} - 0.4
HSTL_III_DCI_18		Note 3	Note 3		
LVCMOS12(4)	2	2	–2	0.4	V_{CCO} - 0.4
	4	4	–4		
	6	6	–6		
LVCMOS15(4)	2	2	–2	0.4	V_{CCO} - 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
LVDCI_15, LVDCI_DV2_15		Note 3	Note 3		
LVCMOS18(4)	2	2	–2	0.4	V_{CCO} - 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16	16	–16		
LVDCI_18, LVDCI_DV2_18		Note 3	Note 3		
LVCMOS25(4,5)	2	2	–2	0.4	V_{CCO} - 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16	16	–16		
	24	24	–24		
LVDCI_25, LVDCI_DV2_25		Note 3	Note 3		

Table 9: **DC Characteristics of User I/Os Using Single-Ended Standards *(Continued)***

Signal Standard (IOSTANDARD) and Current Drive Attribute (mA)		Test Conditions		Logic Level Characteristics	
		I_{OL} (mA)	I_{OH} (mA)	V_{OL} Max (V)	V_{OH} Min (V)
LVCMOS33(4)	2	2	–2	0.4	V_{CCO} - 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16	16	–16		
	24	24	–24		
LVDCI_33, LVDCI_DV2_33		Note 3	Note 3		
LVTTL(4)	2	2	–2	0.4	2.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16	16	–16		
	24	24	–24		
PCI33_3		Note 6	Note 6	$0.10V_{CCO}$	$0.90V_{CCO}$
SSTL18_I		6.7	–6.7	V_{TT} - 0.475	V_{TT} + 0.475
SSTL18_I_DCI		Note 3	Note 3		
SSTL18_II		13.4	–13.4	V_{TT} - 0.475	V_{TT} + 0.475
SSTL2_I		8.1	–8.1	V_{TT} - 0.61	V_{TT} + 0.61
SSTL2_I_DCI		Note 3	Note 3		
SSTL2_II(7)		16.2	–16.2	V_{TT} - 0.80	V_{TT} + 0.80
SSTL2_II_DCI(7)		Note 3	Note 3		

Notes:

1. The numbers in this table are based on the conditions set forth in Table 5 and Table 8.
2. Descriptions of the symbols used in this table are as follows:
   I_{OL} – the output current condition under which V_{OL} is tested
   I_{OH} – the output current condition under which V_{OH} is tested
   V_{OL} – the output voltage that indicates a Low logic level
   V_{OH} – the output voltage that indicates a High logic level
   V_{IL} – the input voltage that indicates a Low logic level
   V_{IH} – the input voltage that indicates a High logic level
   V_{CCO} – the supply voltage for output drivers as well as LVCMOS, LVTTL, and PCI inputs
   V_{REF} – the reference voltage for setting the input switching threshold
   V_{TT} – the voltage applied to a resistor termination
3. Tested according to the standard's relevant specifications. When using the DCI version of a standard on a given I/O bank, that bank will consume more power than if the non-DCI version had been used instead. The additional power is drawn for the purpose of impedance-matching at the I/O pins. A portion of this power is dissipated in the two R_{REF} resistors.
4. For the LVCMOS and LVTTL standards: the same V_{OL} and V_{OH} limits apply for both the Fast and Slow slew attributes.
5. All Dedicated output pins (CCLK, DONE, and TDO) as well as Dual-Purpose totem-pole output pins (D0-D7 and BUSY/DOUT) exhibit the characteristics of LVCMOS25 with 12 mA drive and Fast slew rate. For information concerning the use of 3.3V signals, see the "3.3V-Tolerant Configuration Interface" section in **Module 2**.
6. Tested according to the relevant PCI specifications. For more information, see "Virtex-II Pro and Spartan-3 3.3V PCI Reference Design" (**XAPP653**).

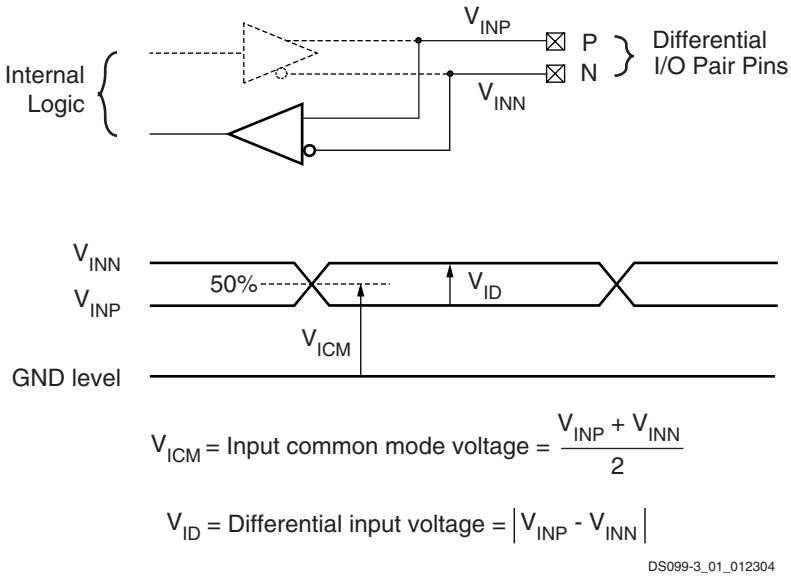


Figure 1: **Differential Input Voltages**

Table 10: **Recommended Operating Conditions for User I/Os Using Differential Signal Standards**

Signal Standard (IOSTANDARD)	V_{CCO}[1]			V_{ID}			V_{ICM}			V_{IH}		V_{IL}	
	Min (V)	Nom (V)	Max (V)	Min (mV)	Nom (mV)	Max (mV)	Min (V)	Nom (V)	Max (V)	Min (V)	Max (V)	Min (V)	Max (V)
LDT_25 (ULVDS_25)	2.375	2.50	2.625	200	600	1000	0.44	0.60	0.78	-	-	-	-
LVDS_25, LVDS_25_DCI	2.375	2.50	2.625	100	350	600	0.30	1.25	2.20	-	-	-	-
BLVDS_25	2.375	2.50	2.625	-	350	-	-	1.25	-	-	-	-	-
LVDSEXT_25, LVDSEXT_25_DCI	2.375	2.50	2.625	100	540	1000	0.30	1.20	2.20	-	-	-	-
LVPECL_25	2.375	2.50	2.625	100	-	-	-	-	-	0.8	2.0	0.5	1.7
RSDS_25	2.375	2.50	2.625	100	200	-	-	1.20	-	-	-	-	-
DIFF_HSTL_II_18, DIFF_HSTL_II_18_DCI	1.70	1.80	1.90	200	-	-	0.80	-	1.00	-	-	-	-
DIFF_SSTL2_II, DIFF_SSTL2_II_DCI	2.375	2.50	2.625	300	-	-	1.05	-	1.45	-	-	-	-

Notes:
1. V_{CCO} only supplies differential output drivers, not input circuits.
2. V_{REF} inputs are not used for any of the differential I/O standards.
3. V_{ID} is a differential measurement.

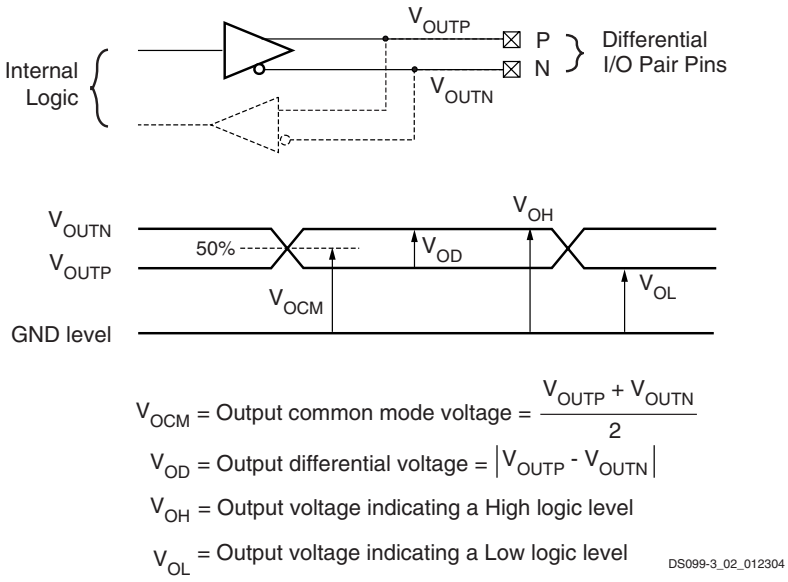


Figure 2: **Differential Output Voltages**

Table 11: **DC Characteristics of User I/Os Using Differential Signal Standards**

Signal Standard	Mask(1) Revision	V_{OD}			ΔV_{OD}		V_{OCM}			ΔV_{OCM}		V_{OH}		V_{OL}	
		Min (mV)	Typ (mV)	Max (mV)	Min (mV)	Max (mV)	Min (V)	Typ (V)	Max (V)	Min (mV)	Max (mV)	Min (V)	Max (V)	Min (V)	Max (V)
LDT_25 (ULVDS_25)	All	430(3)	600	670	–15	15	0.495	0.600	0.715	–15	15	0.71	1.05	0.16	0.50
LVDS_25	'A' – 'E'	100	-	600	-	-	0.80	-	1.6	-	-	0.85	1.90	0.50	1.55
	Future	250	-	450	-	-	1.125	-	1.375	-	-	1.25	1.60	0.90	1.25
BLVDS_25	All	250	350	450	-	-	-	1.20	-	-	-	-	-	-	-
LVDSEXT_25	'A' – 'E'	100	-	600	-	-	0.80	-	1.6	-	-	0.85	1.90	0.50	1.55
	Future	330	-	700	-	-	1.125	-	1.375	-	-	1.29	1.73	0.77	1.21
LVPECL_25(6)	All	-	-	-	-	-	-	-	-	-	-	1.35	1.745	0.565	1.005
RSDS_25	'A' – 'E'	100	-	600	-	-	0.80	-	1.6	-	-	0.85	1.90	0.50	1.55
	Future	100	-	400	-	-	1.1	-	1.4	-	-	1.15	1.60	0.90	1.35
DIFF_HSTL_II_18	All	-	-	-	-	-	-	-	-	-	-	V_{CCO}– 0.40	-	-	0.40
DIFF_SSTL2_II	All	-	-	-	-	-	-	-	-	-	-	V_{TT}– 0.80	-		V_{TT}– 0.80

Notes:
1. The mask revision code appears on the device top marking. See "Package Marking" in **Module 1**.
2. The numbers in this table are based on the conditions set forth in Table 5 and Table 10.
3. V_{OD}, ΔV_{OD}, and ΔV_{OCM} are differential measurements.
4. This value must be compatible with the receiver to which the FPGA's output pair is connected.
5. Output voltage measurements for all differential standards are made with a termination resistor (R_T) of 100Ω across the N and P pins of the differential signal pair.
6. At any given time, only one 2.5V differential output standard (LDT, LVDS, LVDS_EXT, or RSDS) may be assigned to each bank.
7. Each LVPECL output-pair requires three external resistors: a 70Ω resistor in series with each output followed by a 240Ω shunt resistor. These are in addition to the external 100Ω termination resistor at the receiver side. See Figure 3.

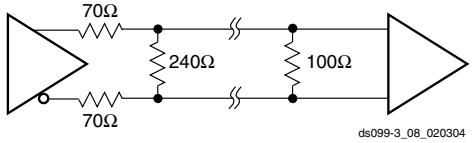


Figure 3: **External Terminations for LVPECL**

Switching Characteristics

All Spartan-3 devices are available in two speed grades: –4 and the higher performance –5. Switching characteristics in this document may be designated as Advance, Preliminary, or Production. Each category is defined as follows:

Advance: These specifications are based on simulations only and are typically available soon after establishing FPGA specifications. Although speed grades with this designation are considered relatively stable and conservative, some under-reported delays may still occur. *The XC3S5000 speed file is undergoing final characterization.*

Preliminary: These specifications are based on complete early silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting preliminary delays is greatly reduced compared to Advance data.

Production: These specifications are approved once enough production silicon of a particular device family member has been characterized to provide full correlation between speed files and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

Production-quality systems must use FPGA designs compiled using a Production status speed file. FPGAs designs using a less mature speed file designation may only be used during system prototyping or preproduction qualification. FPGA designs using Advance or Preliminary status speed files should never be used in a production-quality system.

Whenever a speed file designation changes, as a device matures toward Production status, rerun the Xilinx ISE software on the FPGA design to ensure that the FPGA design incorporates the latest timing information and software updates.

- **Xilinx ISE Software Updates**
  http://www.xilinx.com/xlnx/xil_sw_updates_home.jsp

All specified limits are representative of worst-case supply voltage and junction temperature conditions. Unless otherwise noted, the following applies: Parameter values apply to all Spartan-3 devices. All parameters representing voltages are measured with respect to GND.

Selected timing parameters and their representative values are included below either because they are important as general design requirements or they indicate fundamental device performance characteristics. The Spartan-3 v1.37 speed files are the original source for many but not all of the values. The v1.37 speed files are available in Xilinx Integrated Software Environment (ISE) version 7.1i, Service Pack 3.

The speed grade designations for these files are shown in Table 12. For more complete, more precise, and worst-case data, use the values reported by the Xilinx static timing analyzer (TRACE in the Xilinx development software) and back-annotated to the simulation netlist.

Table 12: **Spartan-3 v1.37 Speed Grade Designations (ISE v7.1, Service Pack 3 or later)**

Device	Advance	Preliminary	Production
XC3S50			–4, -5
XC3S200			–4, -5
XC3S400			–4, -5
XC3S1000			–4, -5
XC3S1500			–4, -5
XC3S2000			–4, -5
XC3S4000			–4, -5
XC3S5000	–4, –5		

I/O Timing

Table 13: **Pin-to-Pin Clock-to-Output Times for the IOB Output Path**

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Max	Max	
Clock-to-Output Times						
$T_{ICKOFDCM}$	When reading from the Output Flip-Flop (OFF), the time from the active transition on the Global Clock pin to data appearing at the Output pin. The DCM is in use.	LVCMOS25(2), 12mA output drive, Fast slew rate, with DCM(3)	**XC3S50**	2.04	2.35	ns
			XC3S200	1.45	1.75	ns
			XC3S400	1.45	1.75	ns
			XC3S1000	2.07	2.39	ns
			XC3S1500	2.05	2.36	ns
			XC3S2000	2.03	2.34	ns
			XC3S4000	1.94	2.24	ns
			XC3S5000	2.00	2.30	ns
T_{ICKOF}	When reading from OFF, the time from the active transition on the Global Clock pin to data appearing at the Output pin. The DCM is not in use.	LVCMOS25(2), 12mA output drive, Fast slew rate, without DCM	**XC3S50**	3.70	4.24	ns
			XC3S200	3.89	4.46	ns
			XC3S400	3.91	4.48	ns
			XC3S1000	4.00	4.59	ns
			XC3S1500	4.07	4.66	ns
			XC3S2000	4.19	4.80	ns
			XC3S4000	4.44	5.09	ns
			XC3S5000	4.38	5.02	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 21 and are based on the operating conditions set forth in Table 5 and Table 8.
2. This clock-to-output time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or a standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. If the former is true, *add* the appropriate Input adjustment from Table 17. If the latter is true, *add* the appropriate Output adjustment from Table 20.
3. DCM output jitter is included in all measurements.

Table 14: **Pin-to-Pin Setup and Hold Times for the IOB Input Path**

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Min	Min	
Setup Times						
T_{PSDCM}	When writing to the Input Flip-Flop (IFF), the time from the setup of data at the Input pin to the active transition at a Global Clock pin. The DCM is in use. No Input Delay is programmed.	LVCMOS25(2), IOBDELAY = NONE, with DCM(4)	**XC3S50**	2.37	2.71	ns
			XC3S200	2.13	2.35	ns
			XC3S400	2.15	2.36	ns
			XC3S1000	2.58	2.95	ns
			XC3S1500	2.55	2.91	ns
			XC3S2000	2.59	2.96	ns
			XC3S4000	2.67	3.05	ns
			XC3S5000	2.52	2.88	ns
T_{PSFD}	When writing to IFF, the time from the setup of data at the Input pin to an active transition at the Global Clock pin. The DCM is not in use. The Input Delay is programmed.	LVCMOS25(2), IOBDELAY = IFD, without DCM	**XC3S50**	3.00	3.46	ns
			XC3S200	2.63	3.02	ns
			XC3S400	2.50	2.87	ns
			XC3S1000	3.50	4.03	ns
			XC3S1500	3.78	4.35	ns
			XC3S2000	3.78	4.35	ns
			XC3S4000	4.44	5.12	ns
			XC3S5000	5.26	6.06	ns
Hold Times						
T_{PHDCM}	When writing to IFF, the time from the active transition at the Global Clock pin to the point when data must be held at the Input pin. The DCM is in use. No Input Delay is programmed.	LVCMOS25(3), IOBDELAY = NONE, with DCM(4)	**XC3S50**	–0.45	–0.40	ns
			XC3S200	–0.12	–0.05	ns
			XC3S400	–0.12	–0.05	ns
			XC3S1000	–0.43	–0.38	ns
			XC3S1500	–0.45	–0.40	ns
			XC3S2000	–0.47	–0.42	ns
			XC3S4000	–0.54	–0.49	ns
			XC3S5000	–0.49	–0.44	ns
T_{PHFD}	When writing to IFF, the time from the active transition at the Global Clock pin to the point when data must be held at the Input pin. The DCM is not in use. The Input Delay is programmed.	LVCMOS25(3), IOBDELAY = IFD, without DCM	**XC3S50**	–0.98	–0.93	ns
			XC3S200	–0.40	–0.35	ns
			XC3S400	–0.27	–0.22	ns
			XC3S1000	–1.19	–1.14	ns
			XC3S1500	–1.43	–1.38	ns
			XC3S2000	–1.38	–1.33	ns
			XC3S4000	–1.82	–1.77	ns
			XC3S5000	–2.57	–2.52	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 21 and are based on the operating conditions set forth in Table 5 and Table 8.
2. This setup time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or the data Input. If this is true of the Global Clock Input, *subtract* the appropriate adjustment from Table 17. If this is true of the data Input, *add* the appropriate Input adjustment from the same table.
3. This hold time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or the data Input. If this is true of the Global Clock Input, *add* the appropriate Input adjustment from Table 17. If this is true of the data Input, *subtract* the appropriate Input adjustment from the same table. When the hold time is negative, it is possible to change the data before the clock's active edge.
4. DCM output jitter is included in all measurements.

Table 15: **Setup and Hold Times for the IOB Input Path**

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Min	Min	
Setup Times						
T_{IOPICK}	Time from the setup of data at the Input pin to the active transition at the ICLK input of the Input Flip-Flop (IFF). No Input Delay is programmed.	LVCMOS25(2), IOBDELAY = NONE	**XC3S50**	1.65	1.89	ns
			XC3S200	1.37	1.57	ns
			XC3S400	1.37	1.57	ns
			XC3S1000	1.65	1.89	ns
			XC3S1500	1.65	1.89	ns
			XC3S2000	1.65	1.89	ns
			XC3S4000	1.73	1.99	ns
			XC3S5000	1.82	2.09	ns
$T_{IOPICKD}$	Time from the setup of data at the Input pin to the active transition at the IFF's ICLK input. The Input Delay is programmed.	LVCMOS25(2), IOBDELAY = IFD	**XC3S50**	4.39	5.04	ns
			XC3S200	4.76	5.47	ns
			XC3S400	4.63	5.32	ns
			XC3S1000	5.02	5.76	ns
			XC3S1500	5.40	6.20	ns
			XC3S2000	6.68	7.68	ns
			XC3S4000	7.16	8.24	ns
			XC3S5000	7.33	8.42	ns
Hold Times						
T_{IOICKP}	Time from the active transition at the IFF's ICLK input to the point where data must be held at the Input pin. No Input Delay is programmed.	LVCMOS25(2), IOBDELAY = NONE	**XC3S50**	-0.55	-0.63	ns
			XC3S200	-0.29	-0.33	ns
			XC3S400	-0.29	-0.33	ns
			XC3S1000	-0.55	-0.63	ns
			XC3S1500	-0.55	-0.63	ns
			XC3S2000	-0.55	-0.63	ns
			XC3S4000	-0.61	-0.71	ns
			XC3S5000	-0.68	-0.79	ns
$T_{IOICKPD}$	Time from the active transition at the IFF's ICLK input to the point where data must be held at the Input pin. The Input Delay is programmed.	LVCMOS25(2), IOBDELAY = IFD	**XC3S50**	-2.74	-3.15	ns
			XC3S200	-3.00	-3.45	ns
			XC3S400	-2.90	-3.33	ns
			XC3S1000	-3.24	-3.73	ns
			XC3S1500	-3.55	-4.08	ns
			XC3S2000	-4.57	-5.26	ns
			XC3S4000	-4.96	-5.70	ns
			XC3S5000	-5.09	-5.85	ns
Set/Reset Pulse Width						
T_{RPW_IOB}	Minimum pulse width to SR control input on IOB		**All**	0.66	0.76	ns

Notes:
1. The numbers in this table are tested using the methodology presented in Table 21 and are based on the operating conditions set forth in Table 5 and Table 8.
2. This setup time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. If this is true, *add* the appropriate Input adjustment from Table 17.
3. These hold times require adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. If this is true, *subtract* the appropriate Input adjustment from Table 17. When the hold time is negative, it is possible to change the data before the clock's active edge.

Table 16: **Propagation Times for the IOB Input Path**

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Max	Max	
Propagation Times						
T_{IOPLI}	The time it takes for data to travel from the Input pin through the IFF latch to the I output with no input delay programmed	LVCMOS25(2), IOBDELAY = NONE	**XC3S50**	2.01	2.31	ns
			XC3S200	1.50	1.72	ns
			XC3S400	1.50	1.72	ns
			XC3S1000	2.01	2.31	ns
			XC3S1500	2.01	2.31	ns
			XC3S2000	2.01	2.31	ns
			XC3S4000	2.09	2.41	ns
			XC3S5000	2.18	2.51	ns
T_{IOPLID}	The time it takes for data to travel from the Input pin through the IFF latch to the I output with the input delay programmed	LVCMOS25(2), IOBDELAY = IFD	**XC3S50**	4.75	5.46	ns
			XC3S200	4.89	5.62	ns
			XC3S400	4.76	5.48	ns
			XC3S1000	5.38	6.18	ns
			XC3S1500	5.76	6.62	ns
			XC3S2000	7.04	8.09	ns
			XC3S4000	7.52	8.65	ns
			XC3S5000	7.69	8.84	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 21 and are based on the operating conditions set forth in Table 5 and Table 8.
2. This propagation time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. When this is true, *add* the appropriate Input adjustment from Table 17.

Table 17: **Input Timing Adjustments for IOB**

Convert Input Time from LVCMOS25 to the Following Signal Standard (IOSTANDARD)	Add the Adjustment Below		Units
	Speed Grade		
	-5	-4	
Single-Ended Standards			
GTL, GTL_DCI	0.44	0.50	ns
GTLP, GTLP_DCI	0.36	0.42	ns
HSLVDCI_15	0.51	0.59	ns
HSLVDCI_18	0.29	0.33	ns
HSLVDCI_25	0.51	0.59	ns
HSLVDCI_33	0.51	0.59	ns
HSTL_I, HSTL_I_DCI	0.51	0.59	ns
HSTL_III, HSTL_III_DCI	0.37	0.42	ns
HSTL_I_18, HSTL_I_DCI_18	0.36	0.41	ns
HSTL_II_18, HSTL_II_DCI_18	0.39	0.45	ns
HSTL_III_18, HSTL_III_DCI_18	0.45	0.52	ns
LVCMOS12	0.63	0.72	ns
LVCMOS15	0.42	0.49	ns
LVDCI_15	0.38	0.43	ns
LVDCI_DV2_15	0.38	0.44	ns
LVCMOS18	0.24	0.28	ns
LVDCI_18	0.29	0.33	ns
LVDCI_DV2_18	0.28	0.33	ns
LVCMOS25	0	0	ns
LVDCI_25	0.05	0.05	ns
LVDCI_DV2_25	0.04	0.04	ns
LVCMOS33, LVDCI_33, LVDCI_DV2_33	–0.05	–0.02	ns
LVTTL	0.18	0.21	ns
PCI33_3	0.20	0.22	ns
PCI66_3	0.18	0.20	ns
SSTL18_I, SSTL18_I_DCI	0.39	0.45	ns
SSTL18_II	0.39	0.45	ns
SSTL2_I, SSTL2_I_DCI	0.40	0.46	ns
SSTL2_II, SSTL2_II_DCI	0.36	0.41	ns
Differential Standards			
LDT_25 (ULVDS_25)	0.76	0.88	ns
LVDS_25, LVDS_25_DCI	0.65	0.75	ns
BLVDS_25	0.34	0.39	ns
LVDSEXT_25, LVDSEXT_25_DCI	0.80	0.92	ns
LVPECL_25	0.18	0.21	ns
RSDS_25	0.43	0.50	ns
DIFF_HSTL_II_18, DIFF_HSTL_II_18_DCI	0.34	0.39	ns
DIFF_SSTL2_II DIFF_SSTL2_II_DCI	0.65	0.75	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 21 and are based on the operating conditions set forth in Table 5, Table 8, and Table 10.
2. These adjustments are used to convert input path times originally specified for the LVCMOS25 standard to times that correspond to other signal standards.

Table 18: **Timing for the IOB Output Path**

Symbol	Description	Conditions	Device	Speed Grade -5 Max	Speed Grade -4 Max	Units
Clock-to-Output Times						
T_{IOCKP}	When reading from the Output Flip-Flop (OFF), the time from the active transition at the OTCLK input to data appearing at the Output pin	LVCMOS25(2), 12mA output drive, Fast slew rate	**XC3S200 XC3S400**	1.63	1.84	ns
			XC3S50 XC3S1000 XC3S1500 XC3S2000 XC3S4000 XC3S5000	2.30	2.64	ns
Propagation Times						
T_{IOOP}	The time it takes for data to travel from the IOB's O input to the Output pin	LVCMOS25(2), 12mA output drive, Fast slew rate	**XC3S200 XC3S400**	1.28	1.46	ns
			XC3S50 XC3S1000 XC3S1500 XC3S2000 XC3S4000 XC3S5000	1.94	2.23	ns
T_{IOOLP}	The time it takes for data to travel from the O input through the OFF latch to the Output pin		**XC3S200 XC3S400**	1.63	1.87	ns
			XC3S50 XC3S1000 XC3S1500 XC3S2000 XC3S4000 XC3S5000	2.30	2.64	ns
Set/Reset Times						
T_{IOSRP}	Time from asserting the OFF's SR input to setting/resetting data at the Output pin	LVCMOS25(2), 12mA output drive, Fast slew rate	**XC3S200 XC3S400**	2.44	2.81	ns
			XC3S50 XC3S1000 XC3S1500 XC3S2000 XC3S4000 XC3S5000	3.11	3.57	ns
T_{IOGSRQ}	Time from asserting the Global Set Reset (GSR) net to setting/resetting data at the Output pin		**All**	8.07	9.28	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 21 and are based on the operating conditions set forth in Table 5 and Table 8.
2. This time requires adjustment whenever a signal standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. When this is true, *add* the appropriate Output adjustment from Table 20.

Table 19: **Timing for the IOB Three-State Path**

Symbol	Description	Conditions	Device	Speed Grade -5 Max	Speed Grade -4 Max	Units
Synchronous Output Enable/Disable Times						
T_{IOCKHZ}	Time from the active transition at the OTCLK input of the Three-state Flip-Flop (TFF) to when the Output pin enters the high-impedance state	LVCMOS25, 12mA output drive, Fast slew rate	**All**	0.74	0.85	ns
T_{IOCKON}(2)	Time from the active transition at TFF's OTCLK input to when the Output pin drives valid data		**All**	2.09	2.40	ns
Asynchronous Output Enable/Disable Times						
T_{GTS}	Time from asserting the Global Three State (GTS) net to when the Output pin enters the high-impedance state	LVCMOS25, 12mA output drive, Fast slew rate	**XC3S200 XC3S400**	7.71	8.87	ns
			XC3S50 XC3S1000 XC3S1500 XC3S2000 XC3S4000 XC3S5000	8.38	9.63	ns
Set/Reset Times						
T_{IOSRHZ}	Time from asserting TFF's SR input to when the Output pin enters a high-impedance state	LVCMOS25, 12mA output drive, Fast slew rate	**All**	1.55	1.78	ns
T_{IOSRON}(2)	Time from asserting TFF's SR input at TFF to when the Output pin drives valid data		**XC3S200 XC3S400**	2.29	2.63	ns
			XC3S50 XC3S1000 XC3S1500 XC3S2000 XC3S4000 XC3S5000	2.91	3.34	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 21 and are based on the operating conditions set forth in Table 5 and Table 8.
2. This time requires adjustment whenever a signal standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. When this is true, *add* the appropriate Output adjustment from Table 20.

Table 20: **Output Timing Adjustments for IOB**

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
Single-Ended Standards					
GTL			0	0.02	ns
GTL_DCI			0.13	0.15	ns
GTLP			0.03	0.04	ns
GTLP_DCI			0.23	0.27	ns
HSLVDCI_15			1.51	1.74	ns
HSLVDCI_18			0.81	0.94	ns
HSLVDCI_25			0.27	0.31	ns
HSLVDCI_33			0.28	0.32	ns
HSTL_I			0.60	0.69	ns
HSTL_I_DCI			0.59	0.68	ns
HSTL_III			0.19	0.22	ns
HSTL_III_DCI			0.20	0.23	ns
HSTL_I_18			0.18	0.21	ns
HSTL_I_DCI_18			0.17	0.19	ns
HSTL_II_18			–0.02	–0.01	ns
HSTL_II_DCI_18			0.75	0.86	ns
HSTL_III_18			0.28	0.32	ns
HSTL_III_DCI_18			0.28	0.32	ns
LVCMOS12	Slow	2 mA	7.60	8.73	ns
		4 mA	7.42	8.53	ns
		6 mA	6.67	7.67	ns
	Fast	2 mA	3.16	3.63	ns
		4 mA	2.70	3.10	ns
		6 mA	2.41	2.77	ns
LVCMOS15	Slow	2 mA	4.55	5.23	ns
		4 mA	3.76	4.32	ns
		6 mA	3.57	4.11	ns
		8 mA	3.55	4.09	ns
		12 mA	3.00	3.45	ns
	Fast	2 mA	3.11	3.57	ns
		4 mA	1.71	1.96	ns
		6 mA	1.44	1.66	ns
		8 mA	1.26	1.44	ns
		12 mA	1.11	1.27	ns

Table 20: **Output Timing Adjustments for IOB *(Continued)***

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
LVDCI_15			1.51	1.74	ns
LVDCI_DV2_15			1.32	1.52	ns
LVCMOS18	Slow	2 mA	5.49	6.31	ns
		4 mA	3.45	3.97	ns
		6 mA	2.84	3.26	ns
		8 mA	2.62	3.01	ns
		12 mA	2.11	2.43	ns
		16 mA	2.07	2.38	ns
	Fast	2 mA	2.50	2.88	ns
		4 mA	1.15	1.32	ns
		6 mA	0.96	1.10	ns
		8 mA	0.87	1.01	ns
		12 mA	0.79	0.91	ns
		16 mA	0.76	0.87	ns
LVDCI_18			0.81	0.94	ns
LVDCI_DV2_18			0.67	0.77	ns
LVCMOS25	Slow	2 mA	6.43	7.39	ns
		4 mA	4.15	4.77	ns
		6 mA	3.38	3.89	ns
		8 mA	2.99	3.44	ns
		12 mA	2.53	2.91	ns
		16 mA	2.50	2.87	ns
		24 mA	2.22	2.55	ns
	Fast	2 mA	3.27	3.76	ns
		4 mA	1.87	2.15	ns
		6 mA	0.32	0.37	ns
		8 mA	0.19	0.22	ns
		12 mA	0	0	ns
		16 mA	–0.02	–0.01	ns
		24 mA	–0.04	–0.02	ns
LVDCI_25			0.27	0.31	ns
LVDCI_DV2_25			0.16	0.19	ns

Table 20: **Output Timing Adjustments for IOB *(Continued)***

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
LVCMOS33	Slow	2 mA	6.38	7.34	ns
		4 mA	4.83	5.55	ns
		6 mA	4.01	4.61	ns
		8 mA	3.92	4.51	ns
		12 mA	2.91	3.35	ns
		16 mA	2.81	3.23	ns
		24 mA	2.49	2.86	ns
	Fast	2 mA	3.86	4.44	ns
		4 mA	1.87	2.15	ns
		6 mA	0.62	0.71	ns
		8 mA	0.61	0.70	ns
		12 mA	0.16	0.19	ns
		16 mA	0.14	0.16	ns
		24 mA	0.06	0.07	ns
LVDCI_33			0.28	0.32	ns
LVDCI_DV2_33			0.26	0.30	ns
LVTTL	Slow	2 mA	7.27	8.36	ns
		4 mA	4.94	5.69	ns
		6 mA	3.98	4.58	ns
		8 mA	3.98	4.58	ns
		12 mA	2.97	3.42	ns
		16 mA	2.84	3.26	ns
		24 mA	2.65	3.04	ns
	Fast	2 mA	4.32	4.97	ns
		4 mA	1.87	2.15	ns
		6 mA	1.27	1.47	ns
		8 mA	1.19	1.37	ns
		12 mA	0.42	0.48	ns
		16 mA	0.27	0.32	ns
		24 mA	0.16	0.18	ns

Table 20: **Output Timing Adjustments for IOB *(Continued)***

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)	Add the Adjustment Below		Units
	Speed Grade		
	-5	-4	
PCI33_3	0.74	0.85	ns
PCI66_3	0.71	0.82	ns
SSTL18_I	0.07	0.07	ns
SSTL18_I_DCI	0.22	0.25	ns
SSTL18_II	0.30	0.34	ns
SSTL2_I	0.23	0.26	ns
SSTL2_I_DCI	0.19	0.22	ns
SSTL2_II	0.13	0.15	ns
SSTL2_II_DCI	0.10	0.11	ns
Differential Standards			
LDT_25 (ULVDS_25)	–0.06	–0.05	ns
LVDS_25	–0.09	–0.07	ns
BLVDS_25	0.02	0.04	ns
LVDSEXT_25	–0.15	–0.13	ns
LVPECL_25	0.16	0.18	ns
RSDS_25	0.05	0.06	ns
DIFF_HSTL_II_18	–0.02	–0.01	ns
DIFF_HSTL_II_18_DCI	0.75	0.86	ns
DIFF_SSTL2_II	0.13	0.15	ns
DIFF_SSTL2_II_DCI	0.10	0.11	ns

Notes:

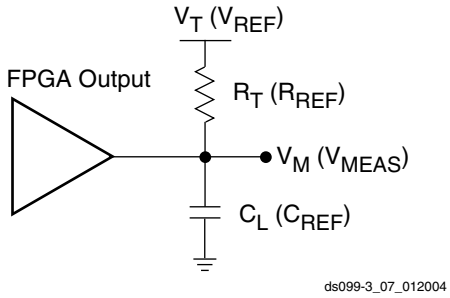
1. The numbers in this table are tested using the methodology presented in Table 21 and are based on the operating conditions set forth in Table 5, Table 8, and Table 10.
2. These adjustments are used to convert output- and three-state-path times originally specified for the LVCMOS25 standard with 12 mA drive and Fast slew rate to times that correspond to other signal standards. Do not adjust times that measure when outputs go into a high-impedance state.

Timing Measurement Methodology

When measuring timing parameters at the programmable I/Os, different signal standards call for different test conditions. Table 21 presents the conditions to use for each standard.

The method for measuring Input timing is as follows: A signal that swings between a Low logic level of V_L and a High logic level of V_H is applied to the Input under test. Some standards also require the application of a bias voltage to the V_{REF} pins of a given bank to properly set the input-switching threshold. The measurement point of the Input signal (V_M) is commonly located halfway between V_L and V_H.

The Output test setup is shown in Figure 4. A termination voltage V_T is applied to the termination resistor R_T, the other end of which is connected to the Output. For each standard, R_T and V_T generally take on the standard values recommended for minimizing signal reflections. If the standard does not ordinarily use terminations (e.g., LVCMOS, LVTTL), then R_T is set to 1MΩ to indicate an open connection, and V_T is set to zero. The same measurement point (V_M) that was used at the Input is also used at the Output.



Notes:
1. The names shown in parentheses are used in the IBIS file.

Figure 4: **Output Test Setup**

Table 21: **Test Methods for Timing Measurement at I/Os**

Signal Standard (IOSTANDARD)	Inputs			Outputs		Inputs and Outputs
	V_{REF} (V)	V_L (V)	V_H (V)	R_T (Ω)	V_T (V)	V_M (V)
Single-Ended						
GTL	0.8	V_{REF} - 0.2	V_{REF} + 0.2	25	1.2	V_{REF}
GTL_DCI				50	1.2	
GTLP	1.0	V_{REF} - 0.2	V_{REF} + 0.2	25	1.5	V_{REF}
GTLP_DCI				50	1.5	
HSLVDCI_15	0.9	V_{REF} - 0.5	V_{REF} + 0.5	1M	0	0.75
HSLVDCI_18						0.90
HSLVDCI_25						1.25
HSLVDCI_33						1.65
HSTL_I	0.75	V_{REF} - 0.5	V_{REF} + 0.5	50	0.75	V_{REF}
HSTL_I_DCI						
HSTL_III	0.90	V_{REF} - 0.5	V_{REF} + 0.5	50	1.5	V_{REF}
HSTL_III_DCI						
HSTL_I_18	0.90	V_{REF} - 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
HSTL_I_DCI_18						
HSTL_II_18	0.90	V_{REF} - 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
HSTL_II_DCI_18						
HSTL_III_18	1.1	V_{REF} - 0.5	V_{REF} + 0.5	50	1.8	V_{REF}
HSTL_III_DCI_18						
LVCMOS12	-	0	1.2	1M	0	0.6
LVCMOS15	-	0	1.5	1M	0	0.75
LVDCI_15						
LVDCI_DV2_15						

Table 21: **Test Methods for Timing Measurement at I/Os *(Continued)***

Signal Standard (IOSTANDARD)		Inputs			Outputs		Inputs and Outputs
		V_{REF} (V)	V_L (V)	V_H (V)	R_T (Ω)	V_T (V)	V_M (V)
LVCMOS18		-	0	1.8	1M	0	0.9
LVDCI_18							
LVDCI_DV2_18							
LVCMOS25		-	0	2.5	1M	0	1.25
LVDCI_25							
LVDCI_DV2_25							
LVCMOS33		-	0	3.3	1M	0	1.65
LVDCI_33							
LVDCI_DV2_33							
LVTTL		-	0	3.3	1M	0	1.4
PCI33_3	Rising	-	Note 3	Note 3	25	0	0.94
	Falling				25	3.3	2.03
SSTL18_I		0.9	V_{REF} - 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
SSTL18_I_DCI							
SSTL18_II		0.9	V_{REF} - 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
SSTL2_I		1.25	V_{REF} - 0.75	V_{REF} + 0.75	50	1.25	V_{REF}
SSTL2_I_DCI							
SSTL2_II		1.25	V_{REF} - 0.75	V_{REF} + 0.75	25	1.25	V_{REF}
SSTL2_II_DCI					50	1.25	
Differential							
LDT_25 (ULVDS_25)		-	V_{ICM} - 0.125	V_{ICM} + 0.125	60	0.6	V_{ICM}
LVDS_25		-	V_{ICM} - 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
LVDS_25_DCI					1M	0	
BLVDS_25		-	V_{ICM} - 0.125	V_{ICM} + 0.125	1M	0	V_{ICM}
LVDSEXT_25		-	V_{ICM} - 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
LVDSEXT_25_DCI					N/A	N/A	
LVPECL_25		-	V_{ICM} - 0.3	V_{ICM} + 0.3	1M	0	V_{ICM}
RSDS_25		-	V_{ICM} - 0.1	V_{ICM} + 0.1	50	1.2	V_{ICM}
DIFF_HSTL_II_18		-	V_{ICM} - 0.5	V_{ICM} + 0.5	50	1.8	V_{ICM}
DIFF_HSTL_II_18_DCI							
DIFF_SSTL2_II		-	V_{ICM} - 0.75	V_{ICM} + 0.75	50	1.25	V_{ICM}
DIFF_SSTL2_II_DCI							

Notes:

1. Descriptions of the relevant symbols are as follows:

   V_{REF} – The reference voltage for setting the input switching threshold
   V_{ICM} – The common mode input voltage
   V_M – Voltage of measurement point on signal transition
   V_L – Low-level test voltage at Input pin
   V_H – High-level test voltage at Input pin
   R_T – Effective termination resistance, which takes on a value of 1MΩ when no parallel termination is required
   V_T – Termination voltage

2. The load capacitance (C_L) at the Output pin is 0 pF for all signal standards.
3. According to the PCI specification.

The capacitive load (C_L) is connected between the output and GND. *The Output timing for all standards, as published in the speed files and the data sheet, is always based on a C_L value of zero.* High-impedance probes (less than 1 pF) are used for all measurements. Any delay that the test fixture might contribute to test measurements is subtracted from those measurements to produce the final timing numbers as published in the speed files and data sheet.

Using IBIS Models to Simulate Load Conditions in Application

IBIS Models permit the most accurate prediction of timing delays for a given application. The parameters found in the IBIS model (V_{REF}, R_{REF}, and V_{MEAS}) correspond directly with the parameters used in Table 21, V_T, R_T, and V_M. Do not confuse V_{REF} (the termination voltage) from the IBIS model with V_{REF} (the input-switching threshold) from the table. A fourth parameter, C_{REF}, is always zero. The four parameters describe all relevant output test conditions. IBIS models are found in the Xilinx development software as well as at the following link.

http://www.xilinx.com/xlnx/xil_sw_updates_home.jsp

Simulate delays for a given application according to its specific load conditions as follows:

1. Simulate the desired signal standard with the output driver connected to the test setup shown in Figure 4. Use parameter values V_T, R_T, and V_M from Table 21. C_{REF} is zero.
2. Record the time to V_M.
3. Simulate the same signal standard with the output driver connected to the PCB trace with load. Use the appropriate IBIS model (including V_{REF}, R_{REF}, C_{REF}, and V_{MEAS} values) or capacitive value to represent the load.
4. Record the time to V_{MEAS}.
5. Compare the results of steps 2 and 4. The increase (or decrease) in delay should be added to (or subtracted from) the appropriate Output standard adjustment

Simultaneously Switching Output Guidelines

This section provides guidelines for the maximum allowable number of Simultaneous Switching Outputs (SSOs). These guidelines describe the maximum number of user I/O pins, of a given output signal standard, that should simultaneously switch in the same direction, while maintaining a safe level of switching noise. Meeting these guidelines for the stated test conditions ensures that the FPGA operates free from the adverse effects of ground and power bounce.

Ground or power bounce occurs when a large number of outputs simultaneously switch in the same direction. The output drive transistors all conduct current to a common voltage rail. Low-to-High transitions conduct to the V_{CCO} rail; High-to-Low transitions conduct to the GND rail. The resulting cumulative current transient induces a voltage difference across the inductance that exists between the die pad and the power supply or ground return. The inductance is associated with bonding wires, the package lead frame, and any other signal routing inside the package. Other variables contribute to SSO noise levels, including stray inductance on the PCB as well as capacitive loading at receivers. Any SSO-induced voltage consequently affects internal switching noise margins and ultimately signal quality.

Table 22 and Table 23 provide the essential SSO guidelines. For each device/package combination, Table 22 provides the number of equivalent V_{CCO}/GND pairs. For each output signal standard and drive strength, Table 23 recommends the maximum number of SSOs, switching in the same direction, allowed per V_{CCO}/GND pair within an I/O bank. The Table 23 guidelines are categorized by package style. Multiply the appropriate numbers from Table 22 and Table 23 to calculate the maximum number of SSOs allowed within an I/O bank. Exceeding these SSO guidelines may result in increased power or ground bounce, degraded signal integrity, or increased system jitter.

$$SSO_{MAX}/IO\ Bank = Table\ 22 \times Table\ 23$$

The number of SSOs allowed for quad-flat packages (VQ, TQ, PQ) is lower than for ball grid array packages (FG) due to the larger lead inductance of the quad-flat packages. The results for chip-scale packaging (CP132) are better than quad-flat packaging but not as high as for ball grid array packaging. Ball grid array packages are recommended for applications with a large number of simultaneously switching outputs.

Table 22: **Equivalent V_{CCO}/GND Pairs per Bank**

Device	VQ100	CP132(1)	TQ144(1)	PQ208	FT256	FG320	FG456	FG676	FG900	FG1156
XC3S50	1	1.5	1.5	2	-	-	-	-	-	-
XC3S200	1	-	1.5	2	3	-	-	-	-	-
XC3S400	-	-	1.5	2	3	3	5	-	-	-
XC3S1000	-	-	-	-	3	3	5	5	-	-
XC3S1500	-	-	-	-	-	3	5	6	-	-
XC3S2000	-	-	-	-	-	-	5	6	9	-
XC3S4000	-	-	-	-	-	-	-	6	10	12
XC3S5000	-	-	-	-	-	-	-	-	10	12

Notes:

1. The V_{CCO} lines for the pair of banks on each side of the CP132 and TQ144 packages are internally tied together. Each pair of interconnected banks shares three V_{CCO}/GND pairs. Consequently, the per bank number is 1.5.
2. The information in this table also applies to Pb-free packages.

Table 23: **Recommended Number of Simultaneously Switching Outputs per V_{CCO}-GND Pair**

Signal Standard (IOSTANDARD)			Package				
			VQ 100	TQ 144	PQ 208	CP 132	FT256, FG320, FG456, FG676, FG900, FG1156
Single-Ended Standards							
GTL			0	0	0	1	4
GTL_DCI			0	0	0	1	4
GTLP			0	0	0	1	4
GTLP_DCI			0	0	0	1	4
HSLVDCI_15			2	1	1	3	14
HSLVDCI_18			4	2	2	6	10
HSLVDCI_25			4	2	2	6	11
HSLVDCI_33			4	2	2	6	9
HSTL_I			3	1	1	5	17
HSTL_I_DCI			3	1	1	5	17
HSTL_III			2	1	1	3	7
HSTL_III_DCI			2	1	1	3	7
HSTL_I_18			4	2	2	6	17
HSTL_I_DCI_18			4	2	2	6	17
HSTL_II_18			2	1	1	3	9
HSTL_II_DCI_18			2	1	1	3	9
HSTL_III_18			2	1	1	3	8
HSTL_III_DCI_18			2	1	1	3	8
LVCMOS12	Slow	2	17	8	5	16	55
		4	10	5	2	6	32
		6	5	3	2	6	18
	Fast	2	6	4	2	6	31
		4	4	1	1	3	13
		6	2	1	1	3	9
LVCMOS15	Slow	2	16	8	6	19	55
		4	8	5	3	9	31
		6	6	3	3	9	18
		8	3	2	1	3	15
		12	2	1	1	3	10
	Fast	2	8	5	4	13	25
		4	4	2	2	6	16
		6	4	2	2	6	13
		8	2	1	1	3	11
		12	2	1	1	3	7
LVDCI_15			2	1	1	3	14
LVDCI_DV2_15			2	1	1	3	14

Table 23: **Recommended Number of Simultaneously Switching Outputs per V_{CCO}-GND Pair *(Continued)***

Signal Standard (IOSTANDARD)			Package				
			VQ 100	TQ 144	PQ 208	CP 132	FT256, FG320, FG456, FG676, FG900, FG1156
LVCMOS18	Slow	2	19	11	9	29	64
		4	13	7	6	19	34
		6	6	3	3	9	22
		8	6	3	3	9	18
		12	3	1	1	3	13
		16	2	1	1	3	10
	Fast	2	13	7	6	19	36
		4	8	5	4	13	21
		6	4	2	2	6	13
		8	4	2	2	6	10
		12	2	1	1	3	9
		16	2	1	1	3	6
LVDCI_18			4	2	2	6	10
LVDCI_DV2_18			4	2	2	6	10
LVCMOS25	Slow	2	28	16	13	42	76
		4	13	7	6	19	46
		6	13	7	6	19	33
		8	6	3	3	9	24
		12	6	3	3	9	18
		16	2	1	1	3	11
		24	2	1	1	3	7
	Fast	2	17	10	8	26	42
		4	8	5	4	13	20
		6	8	5	4	13	15
		8	4	2	2	6	13
		12	4	2	2	6	11
		16	2	1	1	3	8
		24	2	1	1	3	5
LVDCI_25			4	2	2	6	11
LVDCI_DV2_25			4	2	2	6	11

Table 23: **Recommended Number of Simultaneously Switching Outputs per V_{CCO}-GND Pair *(Continued)***

Signal Standard (IOSTANDARD)			Package				
			VQ 100	TQ 144	PQ 208	CP 132	FT256, FG320, FG456, FG676, FG900, FG1156
LVCMOS33	Slow	2	34	20	12	52	76
		4	17	10	8	26	46
		6	17	10	8	26	27
		8	8	5	4	13	20
		12	8	5	4	13	13
		16	4	2	2	6	10
		24	4	2	2	6	9
	Fast	2	17	10	8	26	44
		4	8	5	4	13	26
		6	8	5	4	13	16
		8	4	2	2	6	12
		12	4	2	2	6	10
		16	2	1	1	3	7
		24	2	1	1	3	3
LVDCI_33			4	2	2	6	9
LVDCI_DV2_33			4	2	2	6	9
LVTTL	Slow	2	34	20	16	52	60
		4	17	10	8	26	41
		6	17	10	8	26	29
		8	8	5	4	13	22
		12	8	5	4	13	13
		16	4	2	2	6	11
		24	4	2	2	6	9
	Fast	2	17	10	8	26	34
		4	8	5	4	13	20
		6	8	5	4	13	15
		8	4	2	2	6	12
		12	4	2	2	6	10
		16	2	1	1	3	9
		24	2	1	1	3	5

Table 23: **Recommended Number of Simultaneously Switching Outputs per V_{CCO}-GND Pair *(Continued)***

Signal Standard (IOSTANDARD)	Package				
	VQ 100	TQ 144	PQ 208	CP 132	FT256, FG320, FG456, FG676, FG900, FG1156
PCI33_3	2	1	1	3	7
PCI66_3	2	1	1	3	7
SSTL18_I	4	2	2	6	17
SSTL18_I_DCI	4	2	2	6	17
SSTL18_II	2	1	1	3	9
SSTL2_I	5	2	2	8	13
SSTL2_I_DCI	5	2	2	8	13
SSTL2_II	2	1	1	3	9
SSTL2_II_DCI	2	1	1	3	9
Differential Standards (Number of I/O Pairs or Channels)					
LDT_25 (ULVDS_25)	4	4	4	4	4
LVDS_25	7	3	3	12	20
BLVDS_25	2	1	1		4
LVDSEXT_25	4	4	4	4	4
LVPECL_25	2	1	1		4
RSDS_25	7	3	3	12	20
DIFF_HSTL_II_18	1	1	1	1	4
DIFF_HSTL_II_18_DCI	1	1	1	1	4
DIFF_SSTL2_II	1	1	1	1	4
DIFF_SSTL2_II_DCI	1	1	1	1	4

Notes:
1. The numbers in this table are recommendations that assume sound board layout practice. This table assumes the following parasitic factors: combined PCB trace and land inductance per V_{CCO} and GND pin of 1.0 nH, receiver capacitive load of 15 pF. Test limits appear in Table 24.
2. Regarding the SSO numbers for all DCI standards, the R_{REF} resistors connected to the V_{RN} and V_{RP} pins of the FPGA are 50Ω.
3. If more than one signal standard is assigned to the I/Os of a given bank, refer to **XAPP689**: "Managing Ground Bounce in Large FPGAs" for information on how to perform weighted average SSO calculations.
4. Results are based on worst-case simulation and actual silicon testing using an FPGA seated in a high-quality, low-impedance socket. Data collection is in progress using an FPGA soldered on the test board.

Table 24: **SSO Test Limits**

V_{CCO} (V)	Maximum GND Bounce (V)	Minimum V_{CCO} Rail Collapse (V)
3.3	0.8	2.0
2.5	0.7	1.7
1.8	0.36	1.26
1.5	0.30	1.05

Notes:
1. All voltages referenced to external system ground.

Internal Logic Timing

Table 25: **CLB Timing**

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Clock-to-Output Times						
T_{CKO}	When reading from the FFX (FFY) Flip-Flop, the time from the active transition at the CLK input to data appearing at the XQ (YQ) output	-	0.63	-	0.72	ns
Setup Times						
T_{AS}	Time from the setup of data at the F or G input to the active transition at the CLK input of the CLB	0.46	-	0.53	-	ns
T_{DICK}	Time from the setup of data at the BX or BY input to the active transition at the CLK input of the CLB	0.18	-	0.21	-	ns
Hold Times						
T_{AH}	Time from the active transition at the CLK input to the point where data is last held at the F or G input	0	-	0	-	ns
T_{CKDI}	Time from the active transition at the CLK input to the point where data is last held at the BX or BY input	0.25	-	0.29	-	ns
Clock Timing						
T_{CH}	The High pulse width of the CLB's CLK signal	0.69	-	0.79	-	ns
T_{CL}	The Low pulse width of the CLK signal	0.69	-	0.79	-	ns
F_{TOG}	Maximum toggle frequency (for export control)	-	750	-	650	MHz
Propagation Times						
T_{ILO}	The time it takes for data to travel from the CLB's F (G) input to the X (Y) output	-	0.53	-	0.61	ns
Set/Reset Pulse Width						
T_{RPW_CLB}	The minimum allowable pulse width, High or Low, to the CLB's SR input	0.76	-	0.87	-	ns

Notes:
1. The numbers in this table are based on the operating conditions set forth in Table 5.
2. The timing shown is for SLICEM.

Table 26: **CLB Distributed RAM Switching Characteristics**

Symbol	Description	-5		-4		Units
		Min	Max	Min	Max	
Clock-to-Output Times						
T_{SHCKO}	Time from the active edge at the CLK input to data appearing on the distributed RAM output	-	1.87	-	2.15	ns
Setup Times						
T_{DS}	Setup time of data at the BX or BY input before the active transition at the CLK input of the distributed RAM	0.46	-	0.52	-	ns
T_{AS}	Setup time of the F/G address inputs before the active transition at the CLK input of the distributed RAM	0.46	-	0.53	-	ns
T_{WS}	Setup time of the write enable input before the active transition at the CLK input of the distributed RAM	0.33	-	0.37	-	ns
Hold Times						
T_{DH}, T_{AH}, T_{WH}	Hold time of the BX, BY data inputs, the F/G address inputs, or the write enable input after the active transition at the CLK input of the distributed RAM	0	-	0	-	ns
Clock Pulse Width						
T_{WPH}, T_{WPL}	Minimum High or Low pulse width at CLK input	0.85	-	0.97	-	ns

Table 27: **CLB Shift Register Switching Characteristics**

Symbol	Description	-5		-4		Units
		Min	Max	Min	Max	
Clock-to-Output Times						
T_{REG}	Time from the active edge at the CLK input to data appearing on the shift register output	-	3.30		3.79	ns
Setup Times						
T_{SRLDS}	Setup time of data at the BX or BY input before the active transition at the CLK input of the distributed RAM		-		-	ns
Hold Times						
T_{SRLDH}	Hold time of the BX or BY data input after the active transition at the CLK input of the distributed RAM	0	-	0	-	ns
Clock Pulse Width						
T_{WPH}, T_{WPL}	Minimum High or Low pulse width at CLK input	0.85	-	0.97	-	ns

Table 28: **Synchronous 18 x 18 Multiplier Timing**

Symbol	Description	P Outputs	Speed Grade				Units
			-5		-4		
			Min	Max	Min	Max	
Clock-to-Output Times							
T_{MULTCK}	When reading from the Multiplier, the time from the active transition at the C clock input to data appearing at the P outputs	P[0]	-	1.00	-	1.15	ns
		P[15]	-	1.15	-	1.32	ns
		P[17]	-	1.30	-	1.50	ns
		P[19]	-	1.45	-	1.67	ns
		P[23]	-	1.76	-	2.02	ns
		P[31]	-	2.37	-	2.72	ns
		P[35]	-	2.67	-	3.07	ns
Setup Times							
$T_{MULIDCK}$	Time from the setup of data at the A and B inputs to the active transition at the C input of the Multiplier	-	1.84	-	2.11	-	ns
Hold Times							
$T_{MULCKID}$	Time from the active transition at the Multiplier's C input to the point where data is last held at the A and B inputs	-	0	-	0	-	ns

Notes:
1. The numbers in this table are based on the operating conditions set forth in Table 5.

Table 29: **Asynchronous 18 x 18 Multiplier Timing**

Symbol	Description	P Outputs	Speed Grade		Units
			-5	-4	
			Max	Max	
Propagation Times					
T_{MULT}	The time it takes for data to travel from the A and B inputs to the P outputs	P[0]	1.55	1.78	ns
		P[15]	3.15	3.62	ns
		P[17]	3.36	3.86	ns
		P[19]	3.49	4.01	ns
		P[23]	3.73	4.29	ns
		P[31]	4.23	4.86	ns
		P[35]	4.47	5.14	ns

Notes:
1. The numbers in this table are based on the operating conditions set forth in Table 5.

Table 30: **Block RAM Timing**

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Clock-to-Output Times						
T_{BCKO}	When reading from the Block RAM, the time from the active transition at the CLK input to data appearing at the DOUT output	-	2.09	-	2.40	ns
Setup Times						
T_{BDCK}	Time from the setup of data at the DIN inputs to the active transition at the CLK input of the Block RAM	0.43	-	0.49	-	ns
Hold Times						
T_{BCKD}	Time from the active transition at the Block RAM's CLK input to the point where data is last held at the DIN inputs	0	-	0	-	ns
Clock Timing						
T_{BPWH}	The High pulse width of the Block RAM's CLK signal	1.19	-	1.37	-	ns
T_{BPWL}	The Low pulse width of the CLK signal	1.19	-	1.37	-	ns

Notes:
1. The numbers in this table are based on the operating conditions set forth in Table 5.

Clock Distribution Switching Characteristics

Table 31: **Clock Distribution Switching Characteristics**

Description	Symbol	Minimum	Maximum Speed Grade		Units
			-5	-4	
Global clock buffer (BUFG, BUFGMUX, BUFGCE) I-input to O-output delay	T_{GIO}	0.13	0.36	0.41	ns
Global clock multiplexer (BUFGMUX) select S-input setup to I0- and I1-inputs. Same as BUFGCE enable CE-input	T_{GSI}	0.19	0.53	0.60	ns

Digital Clock Manager (DCM) Timing

For specification purposes, the DCM consists of three key components: the Delay-Locked Loop (DLL), the Digital Frequency Synthesizer (DFS), and the Phase Shifter (PS).

Aspects of DLL operation play a role in all DCM applications. All such applications inevitably use the CLKIN and the CLKFB inputs connected to either the CLK0 or the CLK2X feedback, respectively. Thus, specifications in the DLL tables (Table 32 and Table 33) apply to any application that only employs the DLL component. When the DFS and/or the PS components are used together with the DLL, then the specifications listed in the DFS and PS tables (Table 34 through Table 37) supersede any corresponding ones in the DLL tables. DLL specifications that do not change with the addition of DFS or PS functions are presented in Table 32 and Table 33.

Period jitter and cycle-cycle jitter are two (of many) different ways of characterizing clock jitter. Both specifications describe statistical variation from a mean value.

Period jitter is the worst-case deviation from the average clock period of all clock cycles in the collection of clock periods sampled (usually from 100,000 to more than a million samples for specification purposes). In a histogram of period jitter, the mean value is the clock period.

Cycle-cycle jitter is the worst-case difference in clock period between adjacent clock cycles in the collection of clock periods sampled. In a histogram of cycle-cycle jitter, the mean value is zero.

Delay-Locked Loop (DLL)

Table 32: **Recommended Operating Conditions for the DLL**

Symbol		Description	Frequency Mode/ F_{CLKIN} Range	Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Input Frequency Ranges								
F_{CLKIN}	CLKIN_FREQ_DLL_LF	Frequency for the CLKIN input	Low	18(2)	167(3)	18(2)	167(3)	MHz
	CLKIN_FREQ_DLL_HF		High	48	280(3)	48	280(3,4)	MHz
Input Pulse Requirements								
CLKIN_PULSE		CLKIN pulse width as a percentage of the CLKIN period	$F_{CLKIN} \leq 100$ MHz	40%	60%	40%	60%	-
			$F_{CLKIN} > 100$ MHz	45%	55%	45%	55%	-
Input Clock Jitter Tolerance and Delay Path Variation(4)								
CLKIN_CYC_JITT_DLL_LF		Cycle-to-cycle jitter at the CLKIN input	Low	-	±261	-	±300	ps
CLKIN_CYC_JITT_DLL_HF			High	-	±131	-	+150	ps
CLKIN_PER_JITT_DLL_LF		Period jitter at the CLKIN input	All	-	±0.87	-	±1	ns
CLKIN_PER_JITT_DLL_HF								
CLKFB_DELAY_VAR_EXT		Allowable variation of off-chip feedback delay from the DCM output to the CLKFB input	All	-	±0.87	-	±1	ns

Notes:
1. DLL specifications apply when any of the DLL outputs (CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, or CLKDV) are in use.
2. The DFS, when operating independently of the DLL, supports lower F_{CLKIN} frequencies. See Table 34.
3. To double the maximum effective F_{CLKIN} limit, set the CLKIN_DIVIDE_BY_2 attribute to TRUE.
4. Industrial temperature range devices have additional requirements for continuous clocking, as specified in Table 38.
5. CLKIN input jitter beyond these limits may cause the DCM to lose lock.

Table 33: **Switching Characteristics for the DLL**

Symbol	Description	Frequency Mode / F_{CLKIN} Range	Device	Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Output Frequency Ranges								
CLKOUT_FREQ_1X_LF	Frequency for the CLK0, CLK90, CLK180, and CLK270 outputs	Low	All	18	167	18	167	MHz
CLKOUT_FREQ_1X_HF	Frequency for the CLK0 and CLK180 outputs	High		48	280	48	280	MHz
CLKOUT_FREQ_2X_LF(3)	Frequency for the CLK2X and CLK2X180 outputs	Low		36	334	36	334	MHz
CLKOUT_FREQ_DV_LF	Frequency for the CLKDV output	Low		1.125	110	1.125	110	MHz
CLKOUT_FREQ_DV_HF		High		3	185	3	185	MHz
Output Clock Jitter(4)								
CLKOUT_PER_JITT_0	Period jitter at the CLK0 output	All	All	-	±100	-	±100	ps
CLKOUT_PER_JITT_90	Period jitter at the CLK90 output			-	±150	-	±150	ps
CLKOUT_PER_JITT_180	Period jitter at the CLK180 output			-	±150	-	±150	ps
CLKOUT_PER_JITT_270	Period jitter at the CLK270 output			-	±150	-	±150	ps
CLKOUT_PER_JITT_2X	Period jitter at the CLK2X and CLK2X180 outputs			-	±200	-	±200	ps
CLKOUT_PER_JITT_DV1	Period jitter at the CLKDV output when performing integer division			-	±150	-	±150	ps
CLKOUT_PER_JITT_DV2	Period jitter at the CLKDV output when performing non-integer division			-	±300	-	±300	ps
Duty Cycle								
CLKOUT_DUTY_CYCLE_DLL(5)	Duty cycle variation for the CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV outputs	All	XC3S50	-	±150	-	±150	ps
			XC3S200	-	±150	-	±150	ps
			XC3S400	-	±250	-	±250	ps
			XC3S1000	-	±400	-	±400	ps
			XC3S1500	-	±400	-	±400	ps
			XC3S2000	-	±400	-	±400	ps
			XC3S4000	-	±400	-	±400	ps
			XC3S5000	-	±400	-	±400	ps
Phase Alignment								
CLKIN_CLKFB_PHASE	Phase offset between the CLKIN and CLKFB inputs	All	All	-	±150	-	±150	ps
CLKOUT_PHASE	Phase offset between any two DLL outputs (except CLK2X and CLK0)			-	±140	-	±140	ps
	Phase offset between the CLK2X and CLK0 outputs			-	±250	-	±250	ps

Table 33: **Switching Characteristics for the DLL *(Continued)***

Symbol	Description	Frequency Mode / F_{CLKIN} Range	Device	Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Lock Time								
LOCK_DLL	When using the DLL alone: The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. When the DCM is locked, the CLKIN and CLKFB signals are in phase	18 MHz ≤ F_{CLKIN} ≤ 30 MHz	All	-	2.88	-	2.88	ms
		30 MHz < F_{CLKIN} ≤ 40 MHz		-	2.16	-	2.16	ms
		40 MHz < F_{CLKIN} ≤ 50 MHz		-	1.20	-	1.20	ms
		50 MHz < F_{CLKIN} ≤ 60 MHz		-	0.60	-	0.60	ms
		F_{CLKIN} > 60 MHz		-	0.48	-	0.48	ms
Delay Lines								
DCM_TAP	Delay tap resolution	All	All	30.0	60.0	30.0	60.0	ps

Notes:
1. The numbers in this table are based on the operating conditions set forth in Table 5 and Table 32.
2. DLL specifications apply when any of the DLL outputs (CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, or CLKDV) are in use.
3. Only mask revision 'E' and later devices (see "Package Marking" in **Module 1**) and the XC3S50 and the XC3S1000 support DLL feedback using the CLK2X output. For all other Spartan-3 devices, use feedback from the CLK0 output (instead of the CLK2X output) and set the *CLK_FEEDBACK* attribute to *1X*.
4. Indicates the maximum amount of output jitter that the DCM adds to the jitter on the CLKIN input.
5. This specification only applies if the attribute *DUTY_CYCLE_CORRECTION* = TRUE.

Digital Frequency Synthesizer (DFS)

Table 34: **Recommended Operating Conditions for the DFS**

Symbol		Description	Frequency Mode	Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Input Frequency Ranges(2)								
F_{CLKIN}	CLKIN_FREQ_FX	Frequency for the CLKIN input	All	1	280	1	280	MHz
Input Clock Jitter Tolerance(3)								
CLKIN_CYC_JITT_FX_LF		Cycle-to-cycle jitter at the CLKIN input	Low	-	±261	-	±300	ps
CLKIN_CYC_JITT_FX_HF			High	-	±131	-	±150	ps
CLKIN_PER_JITT_FX		Period jitter at the CLKIN input	All	-	±0.87	-	±1	ns

Notes:
1. DFS specifications apply when either of the DFS outputs (CLKFX or CLKFX180) are used.
2. If both DFS and DLL outputs are used on the same DCM, follow the more restrictive CLKIN_FREQ_DLL specifications in Table 32.
3. CLKIN input jitter beyond these limits may cause the DCM to lose lock.

Table 35: **Switching Characteristics for the DFS**

Symbol	Description	Frequency Mode	Device	Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Output Frequency Ranges								
CLKOUT_FREQ_FX_LF	Frequency for the CLKFX and CLKFX180 outputs	Low	All	18	210	18	210	MHz
CLKOUT_FREQ_FX_HF		High	Mask revisions 'A' – 'D'(5)	210	280	210	280	MHz
			Mask revisions 'E' and later(5)	210	326	210	307	MHz
Output Clock Jitter								
CLKOUT_PER_JITT_FX	Period jitter at the CLKFX and CLKFX180 outputs	All	All	Note 3	Note 3	Note 3	Note 3	ps
Duty Cycle(4)								
CLKOUT_DUTY_CYCLE_FX	Duty cycle precision for the CLKFX and CLKFX180 outputs	All	XC3S50	-	±100	-	±100	ps
			XC3S200	-	±100	-	±100	ps
			XC3S400	-	±250	-	±250	ps
			XC3S1000	-	±400	-	±400	ps
			XC3S1500	-	±400	-	±400	ps
			XC3S2000	-	±400	-	±400	ps
			XC3S4000	-	±400	-	±400	ps
			XC3S5000	-	±400	-	±400	ps
Phase Alignment								
CLKOUT_PHASE	Phase offset between the DFS output and the CLK0 output	All	All	-	±300	-	±300	ps
Lock Time								
LOCK_DLL_FX	When using the DFS in conjunction with the DLL: The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. When the DCM is locked, the CLKIN and CLKFB signals are in phase.	All	All	-	10.0	-	10.0	ms
LOCK_FX	When using the DFS without the DLL: The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. By asserting the LOCKED signal, the DFS indicates valid CLKFX and CLKFX180 signals.	All	All	-	10.0	-	10.0	ms

Notes:
1. The numbers in this table are based on the operating conditions set forth in Table 5 and Table 34.
2. DFS specifications apply when either of the DFS outputs (CLKFX or CLKFX180) is in use.
3. Use the Virtex-II Jitter Calculator at **http://www.xilinx.com/applications/web_ds_v2/jitter_calc.htm**.
4. The CLKFX and CLKFX180 outputs always approximate 50% duty cycles.
5. The mask revision code appears on the device top marking. See "Package Marking" in **Module 1**.

Phase Shifter (PS)

Phase Shifter operation is only supported if the DLL is in the Low frequency mode.

Table 36: **Recommended Operating Conditions for the PS in Variable Phase Mode**

Symbol	Description	Device Revision	Frequency Mode/ F_{CLKIN} Range		Speed Grade				Units
					-5		-4		
					Min	Max	Min	Max	
Operating Frequency Ranges									
PSCLK_FREQ (F_{PSCLK})	Frequency for the PSCLK input	All	Low		1	167	1	167	MHz
Input Pulse Requirements									
PSCLK_PULSE	PSCLK pulse width as a percentage of the PSCLK period	All	Low	$F_{CLKIN} \leq 100$ MHz	40%	60%	40%	60%	-
				$F_{CLKIN} > 100$ MHz	45%	55%	45%	55%	-

Table 37: **Switching Characteristics for the PS in Variable Phase Mode**

Symbol	Description	Frequency Mode/ F_{CLKIN} Range	Speed Grade				Units
			-5		-4		
			Min	Max	Min	Max	
Phase Shifting Range							
FINE_SHIFT_RANGE	Range for variable phase shifting	Low	-	10.0	-	10.0	ns
Lock Time							
LOCK_DLL_PS	When using the PS in conjunction with the DLL: The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. When the DCM is locked, the CLKIN and CLKFB signals are in phase.	18 MHz $\leq F_{CLKIN} \leq$ 30 MHz	-	3.28	-	3.28	ms
		30 MHz $< F_{CLKIN} \leq$ 40 MHz	-	2.56	-	2.56	ms
		40 MHz $< F_{CLKIN} \leq$ 50 MHz	-	1.60	-	1.60	ms
		50 MHz $< F_{CLKIN} \leq$ 60 MHz	-	1.00	-	1.00	ms
		60 MHz $< F_{CLKIN} \leq$ 165 MHz	-	0.88	-	0.88	ms
LOCK_DLL_PS_FX	When using the PS in conjunction with the DLL and DFS: The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. When the DCM is locked, the CLKIN and CLKFB signals are in phase.	Low	-	10.40	-	10.40	ms

Notes:
1. The numbers in this table are based on the operating conditions set forth in Table 5 and Table 36.
2. The PS specifications in this table apply when the PS attribute CLKOUT_PHASE_SHIFT= VARIABLE.

Miscellaneous DCM Timing

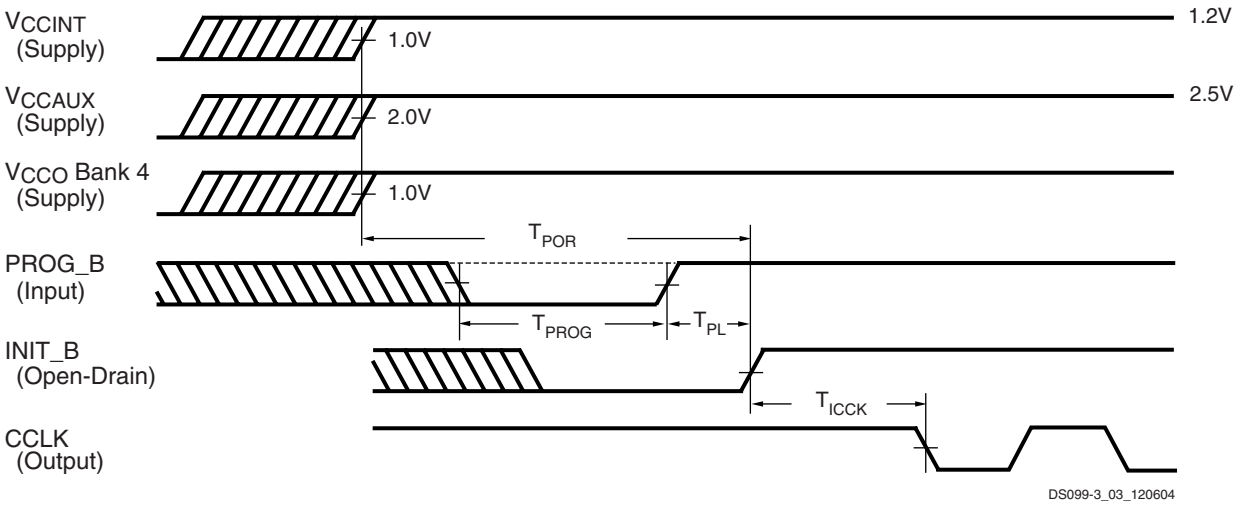
Table 38: **Miscellaneous DCM Timing**

Symbol	Description	DLL Frequency Mode	Temperature Range		Units
			Commercial	Industrial	
DCM_INPUT_CLOCK_STOP	Maximum duration that the CLKIN and CLKFB signals can be stopped(1, 2)	Any	100	100	ms
DCM_RST_PW_MIN	Minimum duration of a RST pulse width	Any	3	3	CLKIN cycles
DCM_RST_PW_MAX	Maximum duration of a RST pulse width(1, 2)	Low	N/A	N/A	seconds
		High	N/A	10	seconds
DCM_CONFIG_LAG_TIME	Maximum duration from V_{CCINT} applied to FPGA configuration successfully completed (DONE pin goes High) and clocks applied to DCM DLL(1, 2)	Low	N/A	N/A	minutes
		High	N/A	10	minutes

Notes:

1. These limits only apply to applications that use the DCM DLL outputs (CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV). The DCM DFS outputs (CLKFX, CLKFX180) are unaffected.
2. Industrial-temperature applications that use the DLL in High-Frequency mode must use a continuous or increasing operating frequency. The DLL under these conditions does not support reducing the operating frequency once establishing an initial operating frequency.

Configuration and JTAG Timing



Notes:
1. The V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies may be applied in any order.
2. The Low-going pulse on PROG_B is optional after power-on but necessary for reconfiguration without a power cycle.
3. The rising edge of INIT_B samples the voltage levels applied to the mode pins (M0 - M2).

Figure 5: **Waveforms for Power-On and the Beginning of Configuration**

Table 39: **Power-On Timing and the Beginning of Configuration**

Symbol	Description	Device	All Speed Grades		Units
			Min	Max	
T_{POR}(2)	The time from the application of V_{CCINT}, V_{CCAUX}, and V_{CCO} Bank 4 supply voltage ramps (whichever occurs last) to the rising transition of the INIT_B pin	XC3S50	-	5	ms
		XC3S200	-	5	ms
		XC3S400	-	5	ms
		XC3S1000	-	5	ms
		XC3S1500	-	7	ms
		XC3S2000	-	7	ms
		XC3S4000	-	7	ms
		XC3S5000	-	7	ms
T_{PROG}	The width of the low-going pulse on the PROG_B pin	All	0.3	-	µs
T_{PL}(2)	The time from the rising edge of the PROG_B pin to the rising transition on the INIT_B pin	XC3S50	-	2	ms
		XC3S200	-	2	ms
		XC3S400	-	2	ms
		XC3S1000	-	2	ms
		XC3S1500	-	3	ms
		XC3S2000	-	3	ms
		XC3S4000	-	3	ms
		XC3S5000	-	3	ms
T_{ICCK}(3)	The time from the rising edge of the INIT_B pin to the generation of the configuration clock signal at the CCLK output pin	All	0.5	4.0	µs

Notes:
1. The numbers in this table are based on the operating conditions set forth in Table 5. This means power must be applied to all V_{CCINT}, V_{CCO}, and V_{CCAUX} lines.
2. Power-on reset and the clearing of configuration memory occurs during this period.
3. This specification applies only for the Master Serial and Master Parallel modes.

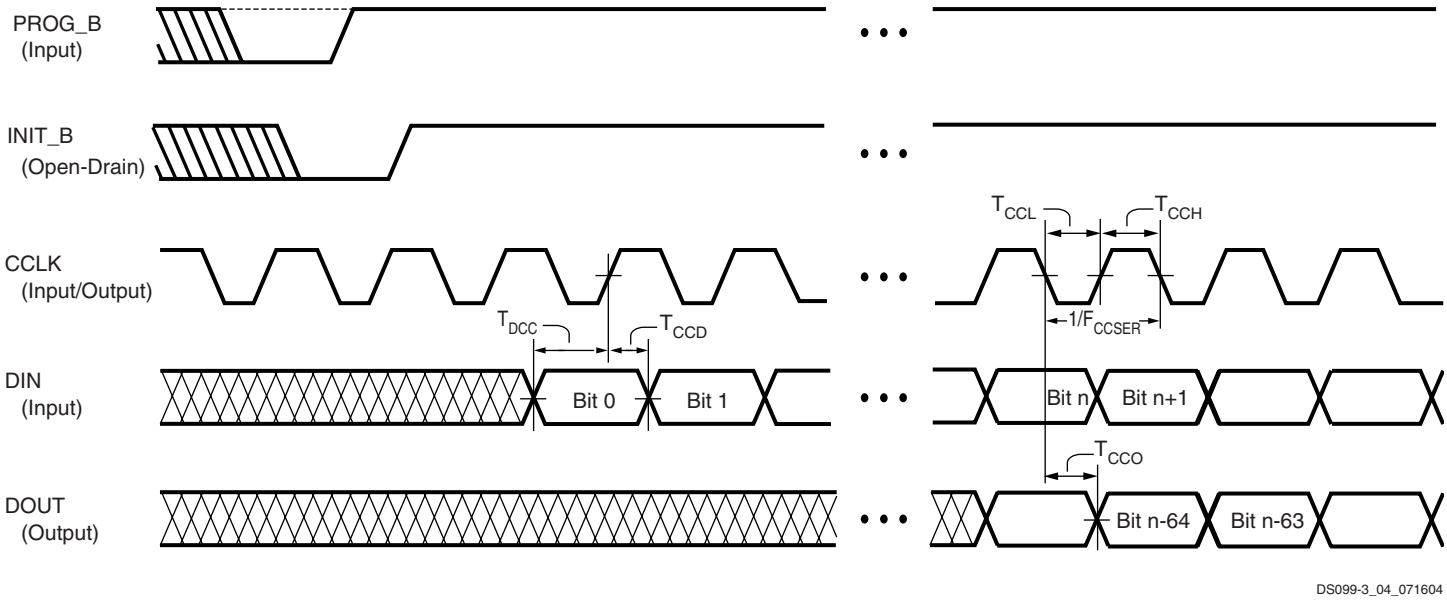
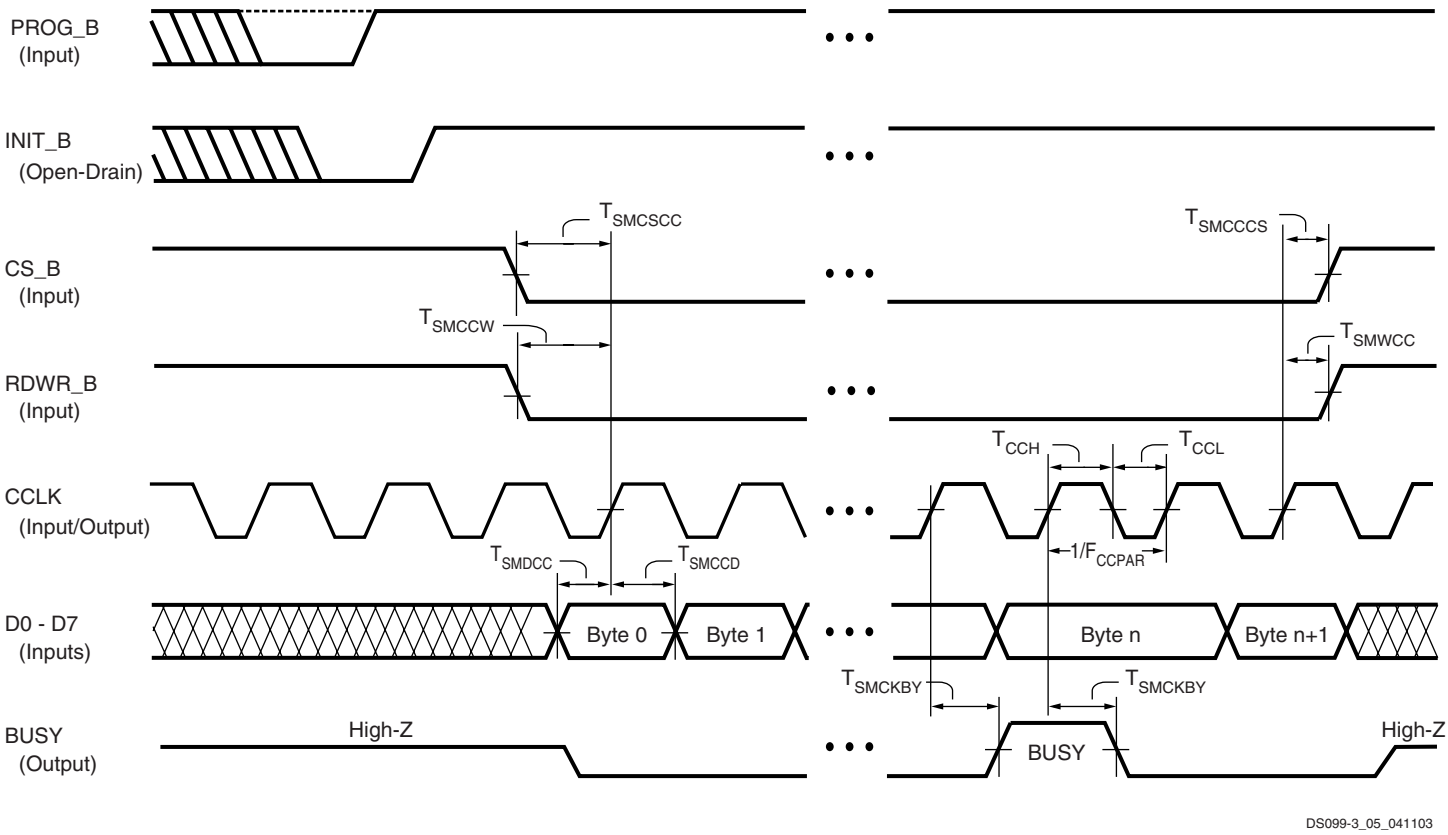


Figure 6: **Waveforms for Master and Slave Serial Configuration**

Table 40: **Timing for the Master and Slave Serial Configuration Modes**

Symbol	Description		Slave/ Master	All Speed Grades		Units
				Min	Max	
Clock-to-Output Times						
T_{CCO}	The time from the falling transition on the CCLK pin to data appearing at the DOUT pin		Both	1.5	12.0	ns
Setup Times						
T_{DCC}	The time from the setup of data at the DIN pin to the rising transition at the CCLK pin		Both	10.0	-	ns
Hold Times						
T_{CCD}	The time from the rising transition at the CCLK pin to the point when data is last held at the DIN pin		Both	0	-	ns
Clock Timing						
T_{CCH}	The High pulse width at the CCLK input pin		Slave	5.0	-	ns
T_{CCL}	The Low pulse width at the CCLK input pin			5.0	-	ns
F_{CCSER}	Frequency of the clock signal at the CCLK input pin	No bitstream compression		0	66(2)	MHz
		With bitstream compression		0	20	MHz
		During STARTUP phase		0	50	MHz
ΔF_{CCSER}	Variation from the CCLK output frequency set using the ConfigRate BitGen option		Master	–50%	+50%	-

Notes:
1. The numbers in this table are based on the operating conditions set forth in Table 5.
2. For serial configuration with a daisy-chain of multiple FPGAs, the maximum limit is 25 MHz.



Notes:
1. Switching RDWR_B High or Low while holding CS_B Low asynchronously aborts configuration.

Figure 7: **Waveforms for Master and Slave Parallel Configuration**

Table 41: **Timing for the Master and Slave Parallel Configuration Modes**

Symbol	Description	Slave/ Master	All Speed Grades		Units
			Min	Max	
Clock-to-Output Times					
T_{SMCKBY}	The time from the rising transition on the CCLK pin to a signal transition at the BUSY pin	Slave	-	12.0	ns
Setup Times					
T_{SMDCC}	The time from the setup of data at the D0-D7 pins to the rising transition at the CCLK pin	Both	10.0	-	ns
T_{SMCSCC}	The time from the setup of a logic level at the CS_B pin to the rising transition at the CCLK pin		10.0	-	ns
T_{SMCCW}(2)	The time from the setup of a logic level at the RDWR_B pin to the rising transition at the CCLK pin		10.0	-	ns

Table 41: **Timing for the Master and Slave Parallel Configuration Modes *(Continued)***

Symbol	Description			Slave/ Master	All Speed Grades		Units
					Min	Max	
Hold Times							
T_{SMCCD}	The time from the rising transition at the CCLK pin to the point when data is last held at the D0-D7 pins			Both	0	-	ns
T_{SMCCCS}	The time from the rising transition at the CCLK pin to the point when a logic level is last held at the CS_B pin				0	-	ns
T_{SMWCC}(2)	The time from the rising transition at the CCLK pin to the point when a logic level is last held at the RDWR_B pin				0	-	ns
Clock Timing							
T_{CCH}	The High pulse width at the CCLK input pin			Slave	5	-	ns
T_{CCL}	The Low pulse width at the CCLK input pin				5	-	ns
F_{CCPAR}	Frequency of the clock signal at the CCLK input pin	No bitstream compression	Not using the BUSY pin(3)		0	50	MHz
			Using the BUSY pin		0	66	MHz
		With bitstream compression			0	20	MHz
		During STARTUP phase			0	50	MHz
ΔF_{CCPAR}	Variation from the CCLK output frequency set using the BitGen option ConfigRate			Master	–50%	+50%	-

Notes:
1. The numbers in this table are based on the operating conditions set forth in Table 5.
2. RDWR_B is synchronized to CCLK for the purpose of performing the Abort operation. The same pin asynchronously controls the driver impedance of the D0 - D7 pins. To avoid contention when writing configuration data to the D0 - D7 bus, do not bring RDWR_B High when CS_B is Low.
3. In the Slave Parallel mode, it is necessary to use the BUSY pin when the CCLK frequency exceeds this maximum specification.
4. Some Xilinx documents may refer to Parallel modes as "SelectMAP" modes.

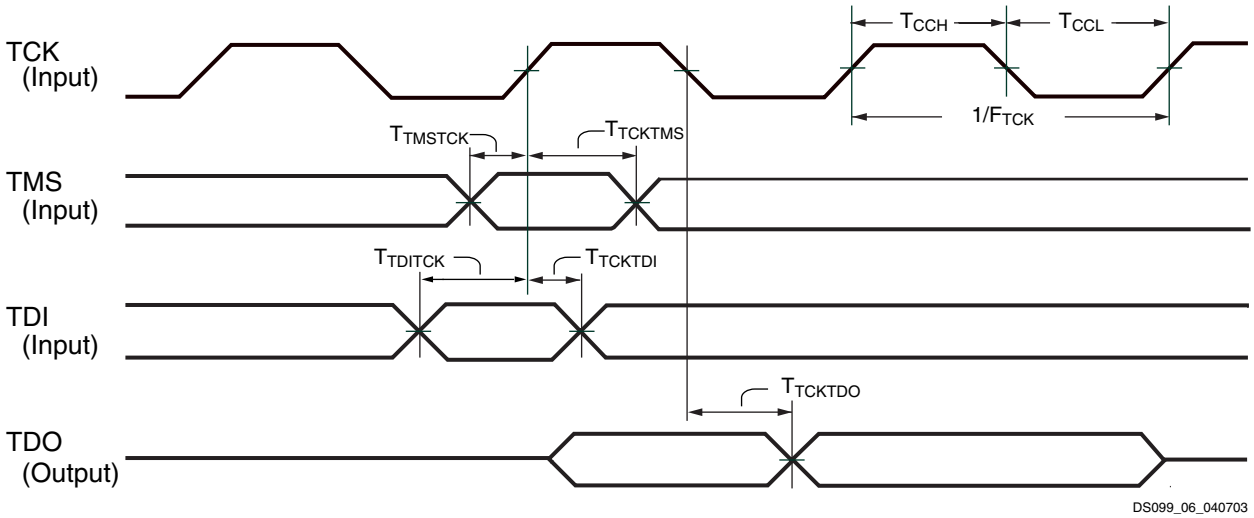


Figure 8: **JTAG Waveforms**

Table 42: **Timing for the JTAG Test Access Port**

Symbol	Description		All Speed Grades		Units
			Min	Max	
Clock-to-Output Times					
T_{TCKTDO}	The time from the falling transition on the TCK pin to data appearing at the TDO pin		1.0	11.0	ns
Setup Times					
T_{TDITCK}	The time from the setup of data at the TDI pin to the rising transition at the TCK pin		7.0	-	ns
T_{TMSTCK}	The time from the setup of a logic level at the TMS pin to the rising transition at the TCK pin		7.0	-	ns
Hold Times					
T_{TCKTDI}	The time from the rising transition at the TCK pin to the point when data is last held at the TDI pin		0	-	ns
T_{TCKTMS}	The time from the rising transition at the TCK pin to the point when a logic level is last held at the TMS pin		0	-	ns
Clock Timing					
T_{CCH}	The High pulse width at the TCK pin		5	-	ns
T_{CCL}	The Low pulse width at the TCK pin		5	-	ns
F_{TCK}	Frequency of the TCK signal	JTAG Configuration	0	33	MHz
		Boundary-Scan	0	25	MHz

Notes:
1. The numbers in this table are based on the operating conditions set forth in Table 5.

Revision History

Date	Version No.	Description
04/11/03	1.0	Initial Xilinx release.
07/11/03	1.1	Extended Absolute Maximum Rating for junction temperature in Table 1. Added numbers for typical quiescent supply current (Table 7) and DLL timing.
02/06/04	1.2	Revised V_{IN} maximum rating (Table 1). Added power-on requirements (Table 3), leakage current number (Table 6), and differential output voltage levels (Table 11) for Rev. 0. Published new quiescent current numbers (Table 7). Updated pull-up and pull-down resistor strengths (Table 6). Added LVDCI_DV2 and LVPECL standards (Table 10 and Table 11). Changed CCLK setup time (Table 40 and Table 41).
03/04/04	1.3	Added timing numbers from v1.29 speed files as well as DCM timing (Table 32 through Table 37).
08/24/04	1.4	Added reference to errata documents on page 1. Clarified Absolute Maximum Ratings and added ESD information (Table 1). Explained V_{CCO} ramp time measurement (Table 3). Clarified I_L specification (Table 6). Updated quiescent current numbers and added information on power-on and surplus current (Table 7). Adjusted V_{REF} range for HSTL_III and HSTL_I_18 and changed V_{IH} min for LVCMOS12 (Table 8). Added note limiting V_{TT} range for SSTL2_II signal standards (Table 9). Calculated V_{OH} and V_{OL} levels for differential standards (Table 11). Updated Switching Characteristics with speed file v1.32 (Table 13 through Table 21 and Table 25 through Table 30). Corrected IOB test conditions (Table 14). Updated DCM timing with latest characterization data (Table 32 through Table 36). Improved DCM CLKIN pulse width specification (Table 32). Recommended use of Virtex-II Jitter calculator (Table 35). Improved DCM PSCLK pulse width specification (Table 36). Changed Phase Shifter lock time parameter (Table 37). Because the BitGen option `Centered_x#_y#` is not necessary for Variable Phase Shift mode, removed BitGen command table and referring text. Adjusted maximum CCLK frequency for the slave serial and parallel configuration modes (Table 40). Inverted CCLK waveform (Figure 6). Adjusted JTAG setup times (Table 42).
12/17/04	1.5	Updated timing parameters to match v1.35 speed file. Improved V_{CCO} ramp time specification (Table 3). Added a note limiting the rate of change of V_{CCAUX} (Table 5). Added typical quiescent current values for the XC3S2000, XC3S4000, and XC3S5000 (Table 7). Increased I_{OH} and I_{OL} for SSTL2-I and SSTL2-II standards (Table 9). Added SSO guidelines for the VQ, TQ, and PQ packages as well as edited SSO guidelines for the FT and FG packages (Table 23). Added maximum CCLK frequencies for configuration using compressed bitstreams (Table 40 and Table 41). Added specifications for the HSLVDCI standards (Table 8, Table 9, Table 17, Table 20, Table 21, and Table 23).
08/19/05	1.6	Updated timing parameters to match v1.37 speed file. All Spartan-3 part types, except XC3S5000, promoted to Production status. Removed V_{CCO} ramp rate restriction from all mask revision 'E' and later devices (Table 3). Added equivalent resistance values for internal pull-up and pull-down resistors (Table 6). Added worst-case quiescent current values for XC3S2000, XC3S4000, XC3S5000 (Table 7). Added industrial temperature range specification and improved typical quiescent current values (Table 7). Improved the DLL minimum clock input frequency specification from 24 MHz down to 18 MHz (Table 32). Improved the DFS minimum and maximum clock output frequency specifications (Table 34, Table 35). Added new miscellaneous DCM specifications (Table 38), primarily affecting Industrial temperature range applications. Updated **Simultaneously Switching Output Guidelines** and Table 23 for QFP packages. Added information on SSTL18_II I/O standard and timing to support DDR2 SDRAM interfaces. Added differential (or complementary single-ended) DIFF_HSTL_II_18 and DIFF_SSTL2_II I/O standards, including DCI terminated versions. Added electro-static discharge (ESD) data for the XC3S2000 and larger FPGAs (Table 1). Added link to Spartan-3 errata notices and how to receive automatic notifications of data sheet or errata changes.

The Spartan-3 Family Data Sheet

DS099-1, ***Spartan-3 FPGA Family: Introduction and Ordering Information*** (Module 1)

DS099-2, *Spartan-3 FPGA Family: Functional Description* (Module 2)

DS099-3, *Spartan-3 FPGA Family: DC and Switching Characteristics* (Module 3)

DS099-4, ***Spartan-3 FPGA Family: Pinout Descriptions*** (Module 4)

DS312, ***Spartan-3E FPGA Family***

DS313, ***Spartan-3L Low Power FPGA Family***

DS314-1, ***Spartan-3 XA Automotive FPGA Family***