EEC170
Computer Architecture

Lecture 1: Introduction to Computer Architecture

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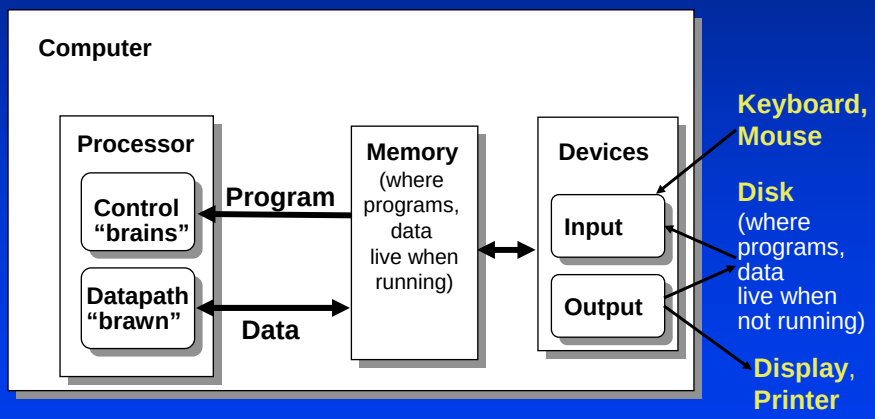
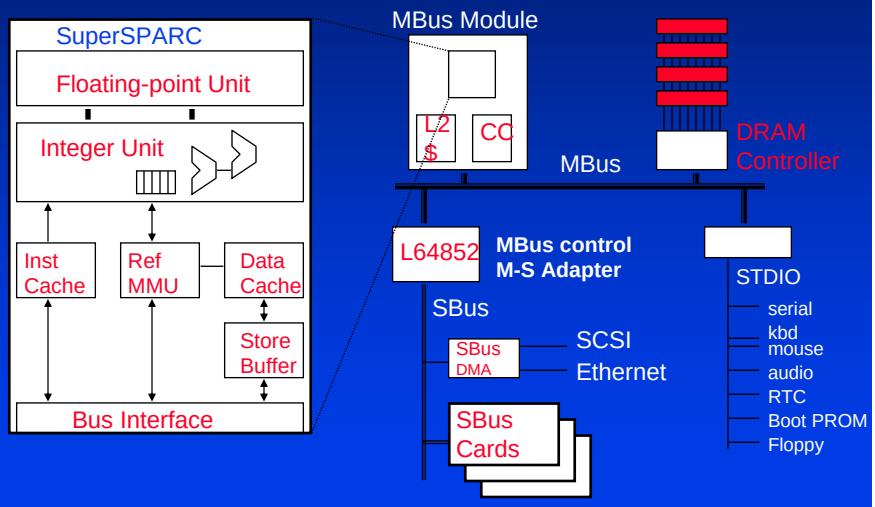
What is a Computer?

It has memory to store data and programs.
It has processing capability (control+datapath)
It has an input/output mechanism

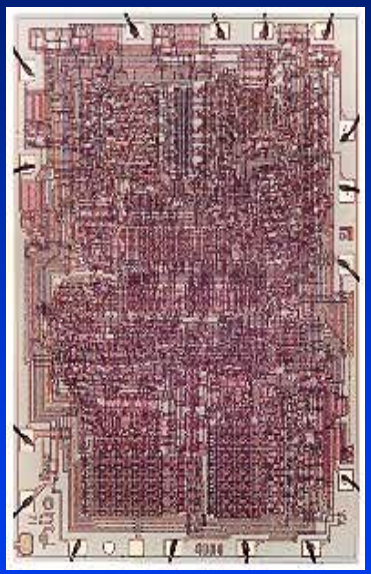


Example Organization

- TI SuperSPARC^{tm} TMS390Z50 in Sun SPARCstation20



Microprocessor Evolution

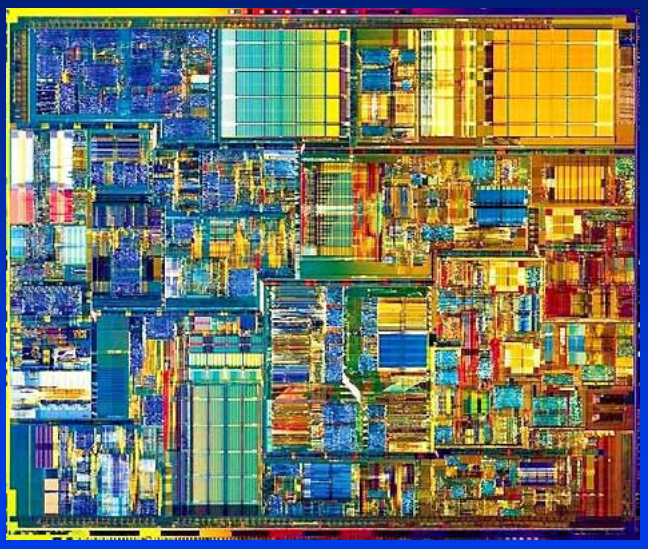


Intel 4004 – introduced 1971

Specs

- 4 bit datapath
- 256-byte ROM
- 32-bit RAM
- 10-bit shift register
- 2300 transistors
- Clock speed - 108 kilohertz, 60,000 operations/second
- 45 instructions

Pentium 4 Die Photo



- Specs:
- 42M transistors
  - PIII: 26M
- 217 mm^2
  - PIII: 106 mm^2
- L1 Execution Cache
  - Buffer 12,000 Micro-Ops
- 8KB data cache
- 256KB L2$

Speed of Computer Technologies

Epoch	Technology	Operations/sec
1930	Mechanical	1
1940	Relay	10
1950	Vacuum Tube	1,000
1960	Transistor	1,000,000
1970	Intergated Circuit	10,000,000
1980	Microprocessor	100,000,000
1990	Microprocessor	1,000,000,000
2000	Microprocessor	1,000,000,000,000
2010	Microprocessor, Quantum, Nano, Biological?	100,000,000,000,000?

Computer Technology - Dramatic Change!

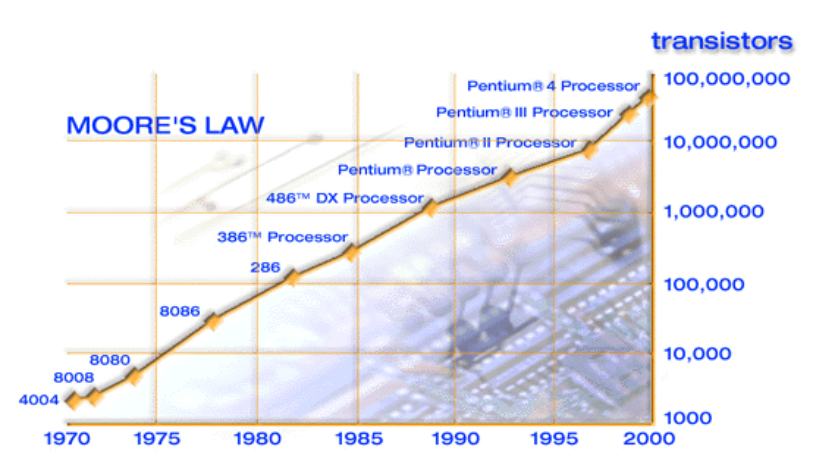
- Processor
  - 2X in speed every 1.5 years (since ‘85); 100X performance in last decade.
- Memory
  - DRAM capacity: 2x / 2 years (since ‘96); 64x size improvement in last decade.
- Disk
  - Capacity: 2X / 1 year (since ‘97)
  - 250X size in last decade.

Computer Technology => Dramatic Change

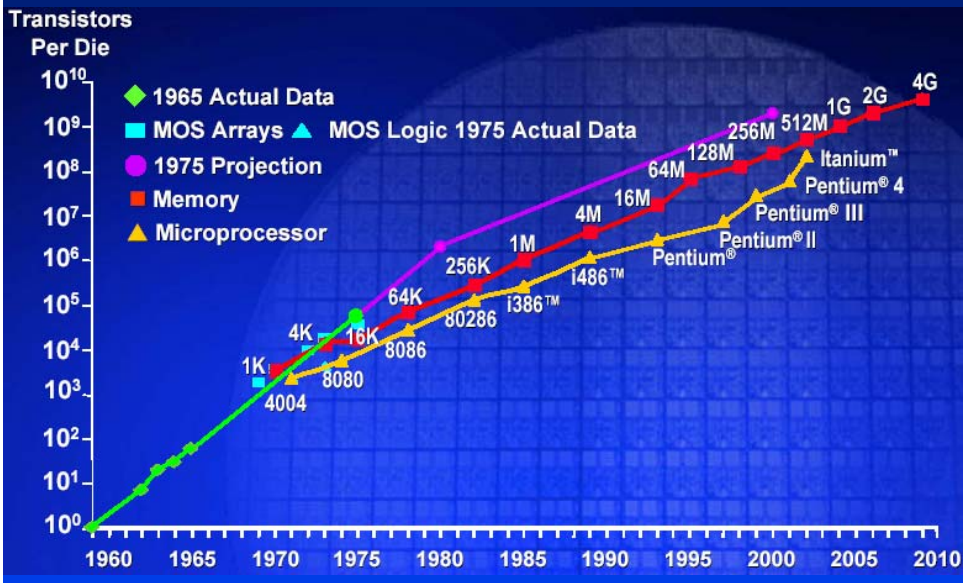
- State-of-the-art PC when you graduate:
  - Processor clock speed: 12.0 GigaHertz
  - Memory capacity: 10.0 GigaBytes
  - Disk capacity: 10000 GigaBytes (10.0 TeraBytes)
  - New unit! Giga => Tera
  - Might not be the case!
    - Challenges to Moore’s law

Technology Trends – Moore's Law

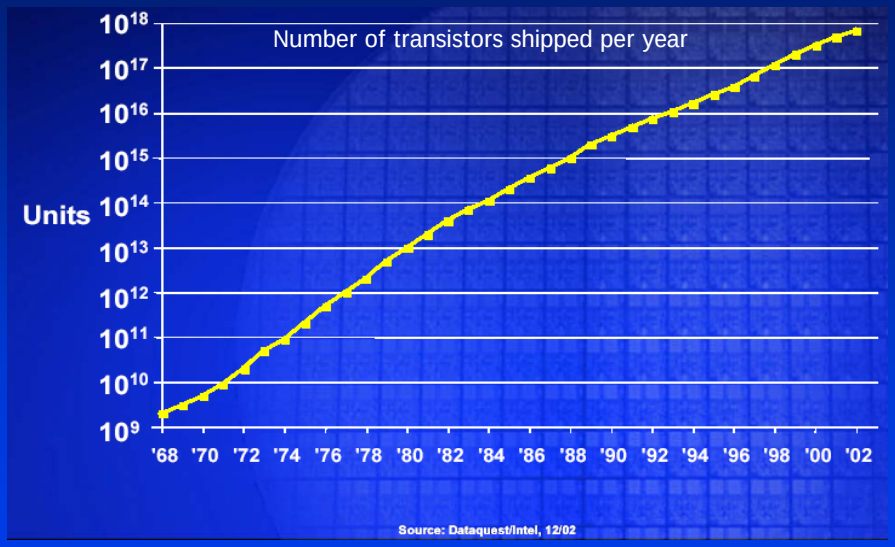
- In 1965, Gordon Moore predicted that the number of transistors per chip would double every 18 months (1.5 years)



Did Moore's prediction hold?



Side effects of Moore's Law



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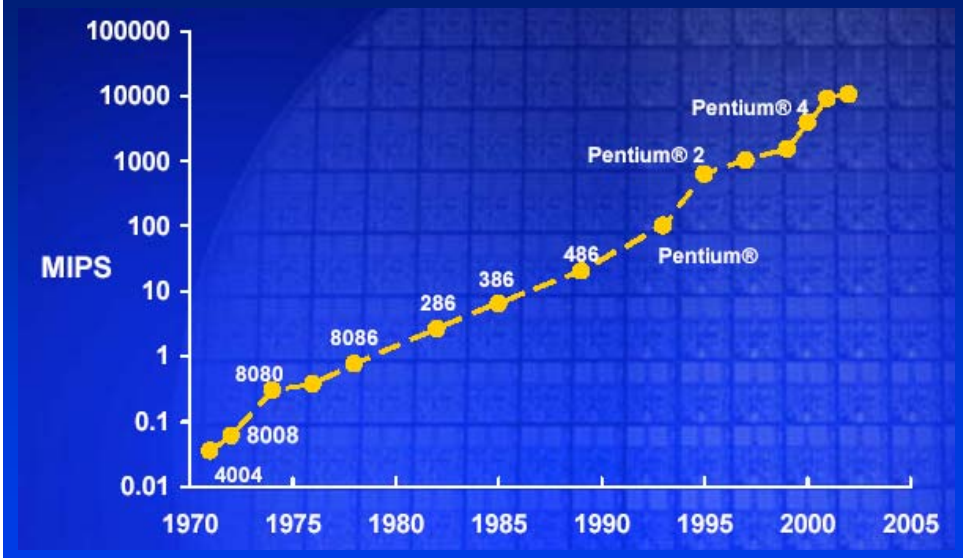

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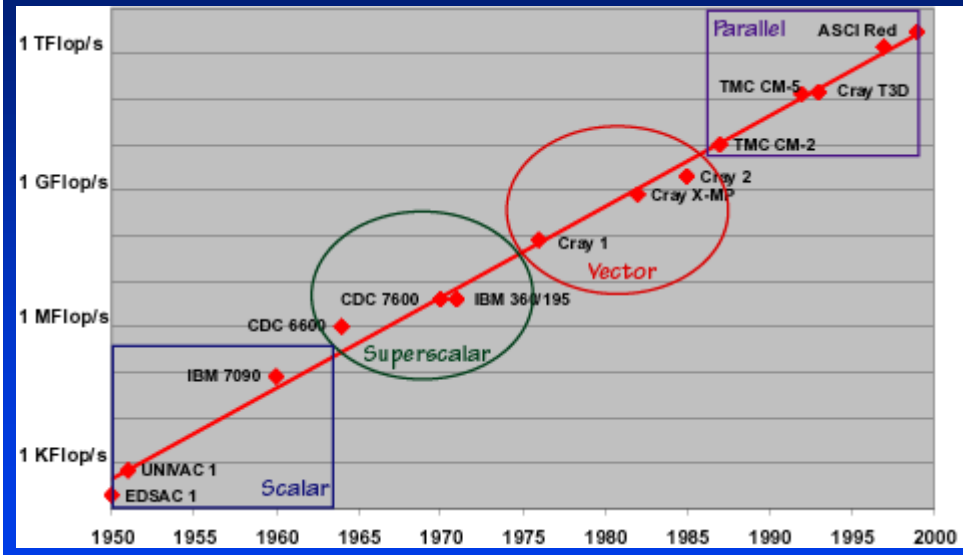
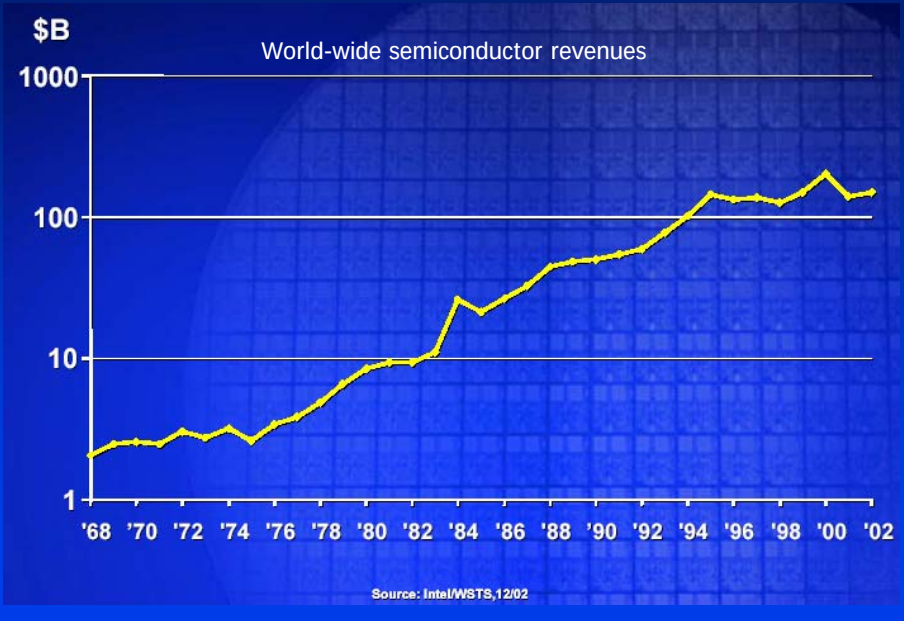


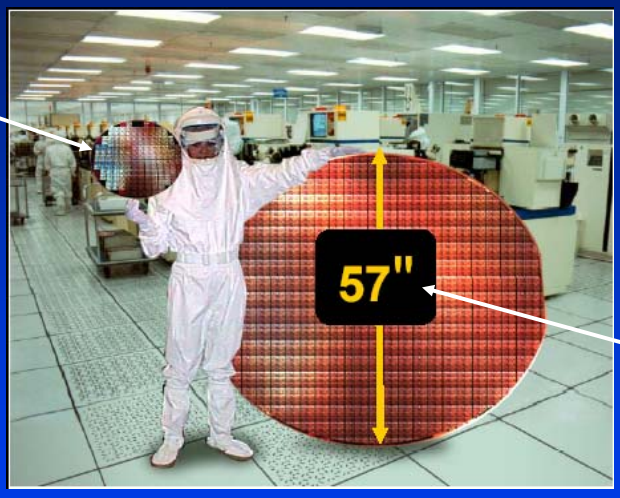
Side effects of Moore's Law



Side effects of Moore's Law

What is the actual size of a modern wafer?

Actual size of wafer today - 300 mm diameter, approx. 12''

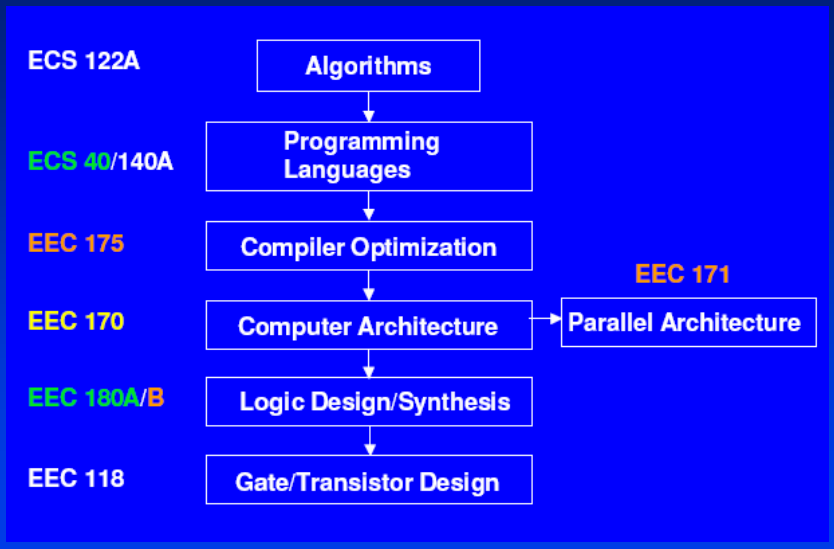


Moore's prediction

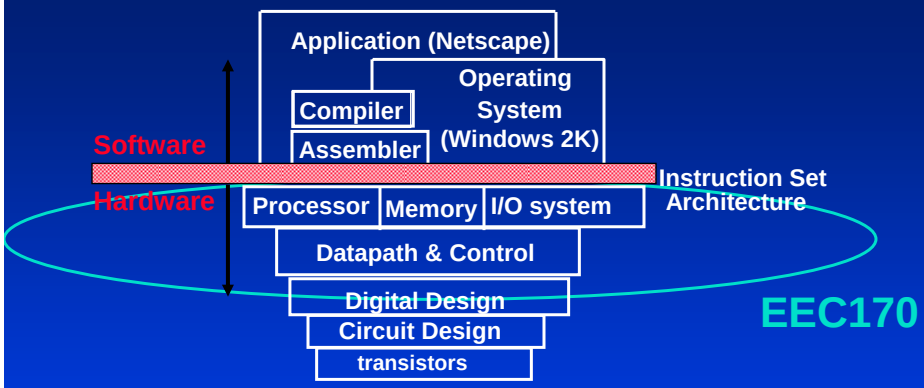
Moore didn't get everything right

The Classic Computer Engineering Problem:

How to physically implement computations?

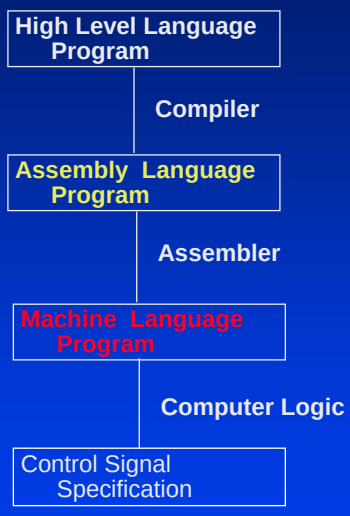


Where is Computer Architecture?



* Coordination of many *levels of abstraction*

Levels of Representation



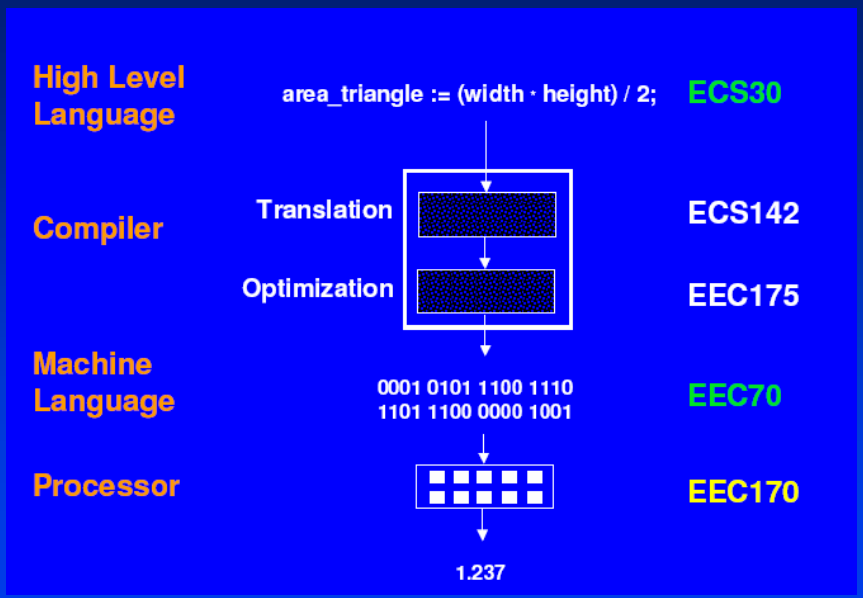

```
temp = v[k];
v[k] = v[k+1];
v[k+1] = temp;
```

```
lw  $15,   0($2)
lw  $16,   4($2)
sw $16,   0($2)
sw $15,   4($2)
```

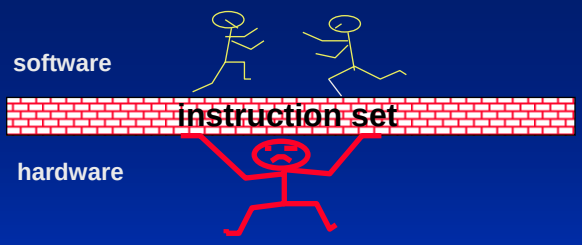
```
0000 1001 1100 0110 1010 1111 0101 1000
1010 1111 0101 1000 0000 1001 1100 0110
1100 0110 1010 1111 0101 1000 0000 1001
0101 1000 0000 1001 1100 0110 1010 1111
```

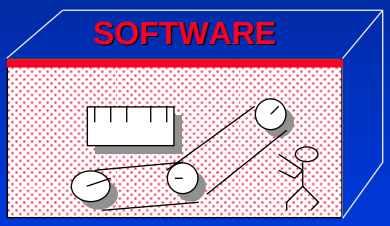
ALUOP[0:3] <= InstReg{9:12] & MASK

EEC170 View



Instruction Set Interface





-- Organization of Programmable Storage

-- Data Types & Data Structures: Encodings & Representations

-- Instruction Formats

-- Instruction (or Operation Code) Set

-- Modes of Addressing and Accessing Data Items and Instructions

-- Exceptional Conditions

Computer Implementation

Logic Designer's View

ISA Level

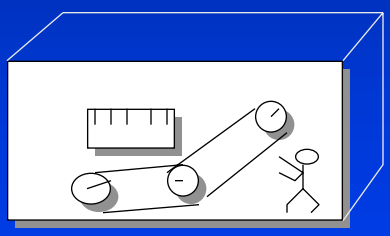
FUs & Interconnect

-- Capabilities & Performance Characteristics of Principal Functional Units
(e.g., Registers, ALU, Shifters, Logic Units, ...)

-- Ways in which these components are interconnected

-- nature of information flows between components

-- logic and means by which such information flow is controlled.



Choreography of FUs to realize the ISA

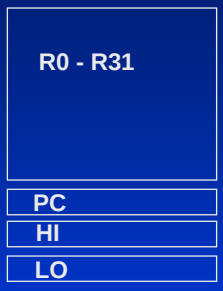
Register Transfer Level Description

Example ISAs (Instruction Set Architectures)

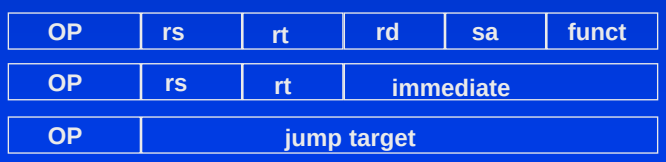
° Digital Alpha	(v1, v3)	1992-97
° HP PA-RISC	(v1.1, v2.0)	1986-96
° Sun Sparc	(v8, v9)	1987-95
° SGI MIPS	(MIPS I, II, III, IV, V)	1986-96
° Intel	(8086,80286,80386, 80486,Pentium, MMX, ...)	1978-96

MIPS Instruction Set Architecture

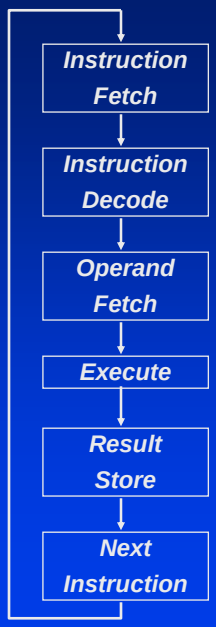
° Instruction Categories
- Load/Store
- Computational
- Jump and Branch
- Floating Point
  - coprocessor
- Memory Management
- Special



3 Instruction Formats: all 32 bits wide



Instruction Interpretation Cycle (Execution Cycle)



Obtain instruction from program storage

Determine required actions and instruction size

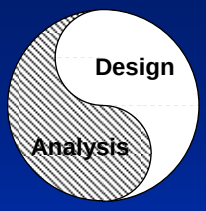
Locate and obtain operand data

Compute result value or status

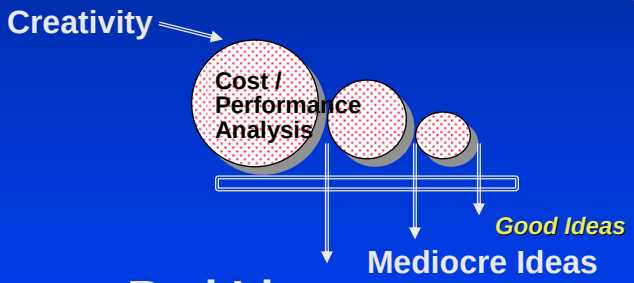
Deposit results in storage for later use

Determine successor instruction

Measurement and Evaluation



Architecture is an iterative process
-- searching the space of possible designs
-- at all levels of computer systems



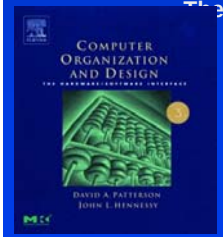
EEC170: So what's in it for me?

- Understanding of the inner-workings of modern computers, which is useful when programming them
- Understanding of trade-offs present at the hardware/software boundary
- Much of what used to be software can now be implemented in hardware.
- Insight into operations that are easy/hard to implement in hardware
- People who understand both hardware and software are in great demand
- Basis (and better understanding) for advanced courses
  - Operating systems
  - Compilers (EEC175)
  - Graduate Computer Architecture (EEC270)
  - High-performance parallel computing (EEC171)

Participate in lecture, ask questions

ECE154: Computer Architecture and Engineering

Instructor:	Soheil Ghiasi	
	Office: 3171 Kemper Hall, "*my-first-name*"@ece.ucdavis.edu	
	Office Hours: Thursday 3-5pm	
	prefer questions after class, or in office hours rather than email (if possible)	
TA:	Chris Giacomotto	giacomoc AT-SIGN ucdavis.edu
	Office Hours	Monday 4-6pm
	location:	TBD
Text:	Computer Organization & Design:	
	The Hardware / Software Interface (third edition)	



← This one

Not this one →

About Me

- PhD: UCLA 2004
- Joined UC-Davis in October 2004
- Undergraduate Teaching: EEC180A-B, EEC170
- Research: Computer in Embedded Applications (embedded systems)

Course Logistics: On the Web

- Course web site URL
  http://www.ece.ucdavis.edu/~soheil/teaching/EEC170-F05
- On-line material
  - lecture viewgraphs in PDF
  - softcopies of handouts, homework, project description, etc.
  - important announcements
  - I'll assume that you check website daily
    - Make sure to reload ☺
- Class mailing list

Class Format

- Published Schedule:
  - Lecture: 2:10-3:30
  - Discussion: 3:30-4
- Actual Schedule:
  - Lecture and discussion are merged
  - Two approx. 50 min lectures with 10 min break
    - 2:10-3:00
    - 3:10-4:00
  - Occasional classes are entirely dedicated to problem solving, exam review and might be taught by the TA.

Exams

- Midterm: Nov 9th in Class
  - Material Chapters 1-5
- Final: 1:30pm Friday, December 16, 2005
- Review meetings: the class before the exams
- Goal: test knowledge and reasoning rather than memory

Homework Assignments and Quiz (mini-project)

- All assignments are assigned on Wednesday
  - Assignments due second following Friday at 5pm in EEC170 box
    - 2131 Kemper Hall
  - Most weeks
    - Except for the first and thanksgiving week

Grading

- Grade breakdown
  - Homework Assignments 20%
  - Quiz or mini-projects 10%
  - Midterm Exam: 30%
  - Final: 40%

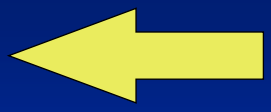
Cheating

- Don’t do it

Course Problems

TALK TO US, EARLY !!!!!

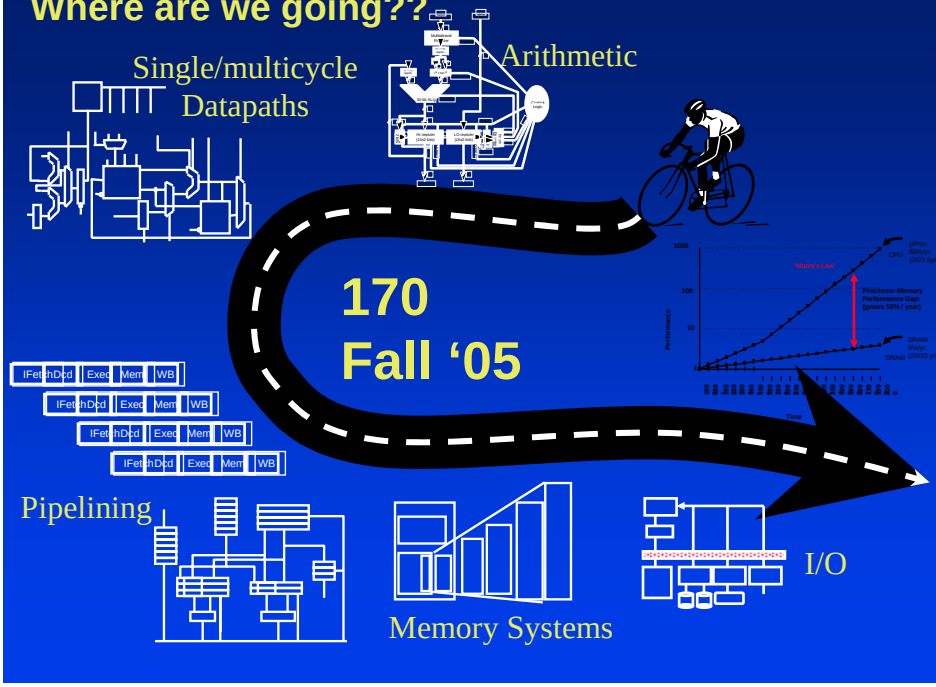
WE ARE HERE TO HELP !!!!



° Can't make midterm or final
- Tell us early.
- The makeup exam will probably be an oral exam with the instructor.
- You don't want to try it unless you have to ☺

° Late Homework Policy
- No late homework is accepted!

Where are we going??



Summary

- All computers consist of five components
  - Processor: (1) datapath and (2) control
  - (3) Memory
  - (4) Input devices and (5) Output devices
- Moore's Law has fueled a dramatic change in computer technology
  - Faster, cheaper computation
  - Complicated computing machines
- Abstraction is the key to design increasingly complicated computing devices

Reading Assignment

- Read chapter 1
  - Try to do some problems
- Review your EEC70 notes
  - We will need them next time!
- Do not need to turn these in