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Ultra-smooth platinum surfaces for nanoscale devices fabricated using chemical mechanical polishing

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ABSTRACT A technique involving two steps of chemical mechanical polishing (CMP) has been developed to produce ultra-smooth metal surfaces with an RMS roughness better than 0.1 nm. A figure of merit termed degree of smoothness (DOS) is proposed for the purpose of quantifying the extent of smoothness of a polished metal surface. A post CMP metal slurry cleaning solution was used for cleaning Pt slurry for the first time and by applying special techniques, a very high quality clean surface was attained. Applications of the polished Pt electrodes in interfacing molecular switching devices with self-assembled monolayers of molecules have been found to dramatically improve the packing and orientation of the molecular monolayer with a huge improvement in the molecular electronics device yields. These smooth metal surfaces may open doors for new opportunities in future nanoscale devices.

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1 Introduction

Chemical mechanical polishing (CMP), first introduced into the semiconductor industry to planarize interlevel dielectrics (ILD), has been very effective in implementing multi-level metallization integration [1]. New techniques and consumables for polishing copper (Cu), tungsten (W) and shallow trench isolation (STI) have revolutionized semiconductor manufacturing [1–9]. Although the process was initially developed for ILD, it began to be used instead of reactive ion etching (RIE) to remove tungsten that was deposited to fill the via opening between metal layers [10]. Over time, the fabrication of inlaid trenches filled with metal, also known as damascene, was developed. All these eventually led to copper interconnects in standard semiconductor processing. Without CMP, Cu could have not been used for interconnects even though it has lower resistivity than aluminum (Al) due to difficulty of etching Cu with RIE.

The CMP process for conventional microelectronics industry has experienced an ongoing development over several years and a great deal has been accomplished in terms of precise control of removal rate, surface smoothness, reduced micro-scratches, local and global uniformity. Although feature sizes are shrinking to diminishing dimensions, the devices and interconnects in a microprocessor or memory array are much larger than the residual surface roughness that an optimum CMP process can offer today. However, as the device feature size further decreases and research community looks for alternative materials for electronic devices, such as DNA, organic molecules or carbon nanotubes, the requirement for CMP is going to be more stringent and the traditional CMP process will need to go through enormous improvements to be applicable in the fabrication of nanodevices. New types of metals such as silver (Ag) and platinum (Pt) are being increasingly explored in the research community. Applications such as metal structures for negative index materials, photonic crystals, molds for nano-imprinting and surface enhanced Raman spectroscopy (SERS) require high level of surface smoothness in the metal features and a sophisticated CMP process is crucial for manufacturable fabrication of such future devices and systems. Many of the future nanodevices are expected to be smaller than the typical grain-size of freshly deposited metals. Figure 1 depicts the surface topology of freshly deposited (a) Au, (b) Ag and (c) Pt surfaces. Clearly, the grain-sizes are larger or comparable to the sizes of typical molecules used in molecular electronic devices and there has been an issue of extremely low device yields due to shorting caused by the spikes and grains of freshly deposited metals. A mechanism is needed to eliminate the surface roughness of metals in order to fabricate predictable and repeatable nano-devices. In this paper, we present our work on the CMP process for polishing Pt surfaces. We applied the polished electrodes for interfacing molecular electronic device and observed a dramatic improvement in the yields of the devices with self-assembled monolayers (SAMs). We present the challenges in Pt polishing, our two-step polishing technique, and the results we obtained which include the smoothest Pt surface ever reported.

2 Polishing procedure

Although scientific understanding of underlying polishing mechanism was not critical for developing effective CMP processes, effort has been made to develop quantita-

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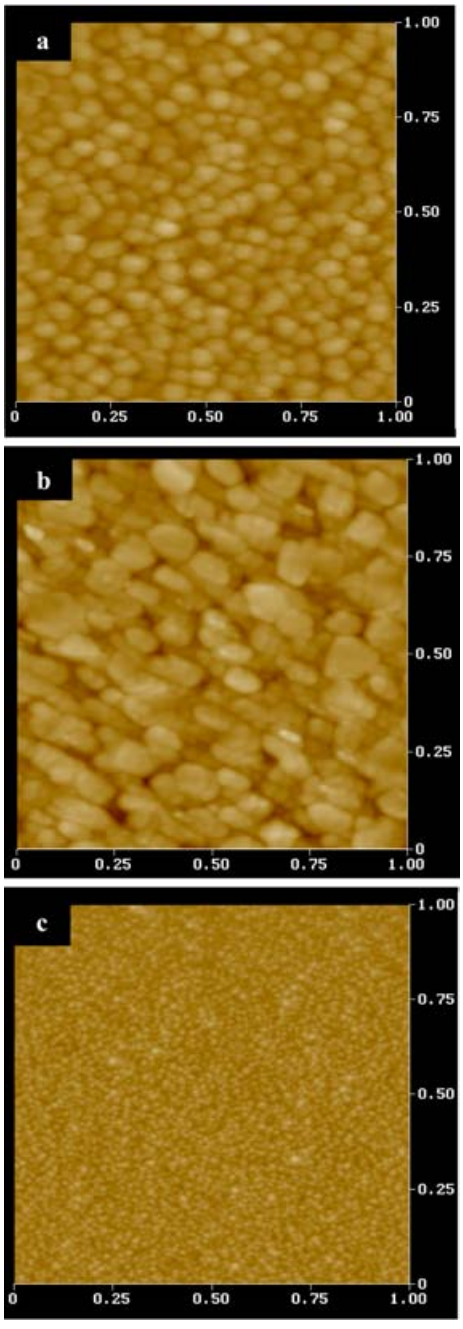

FIGURE 1 Surface topology of freshly deposited (**a**) Au, (**b**) Ag and (**c**) Pt surfaces. The average grain size is 8 nm for Au, 15 nm for Ag and 3 nm for Pt

tive models [11]. Ever-increasing demand is likely to motivate more basic research to understand the CMP mechanism and subsequent success will lead to future waves of success. In a CMP process, a rotating carrier with a wafer faced down is pressed against a moving platen containing a polishing pad with a thin colloidal layer of slurry [12]. The process selectively removes high elevation features more rapidly than low elevations, to result in a planar topology. The polishing processes require careful choice of pad and carrier rotational speed, slurry flow rate, carrier pressure, carrier sweeping frequency for optimum results. For sub-nanometer surface roughness and micro scratch-free polished surface, vibration isolation of the polishing equipment may greatly improve the surface quality.

Metal CMP slurries, in general, use alumina particles suspended in various liquids. Alumina (Al_2O_3) slurries have an inherent capability of removing metal with higher selectivity to other material on a wafer (mainly oxide or Si). However, alumina based slurry is typically poor in colloidal stability and form agglomeration causing a large number of micro and nano-scratches in the metal films. Filtering slurry solution for eliminating possible harmful effects of agglomeration may help reduce surface defects.

There is a trade-off between high removal rate and smoothness of the polished surface. A high removal rate is highly likely to contribute to a high density of micro and nano scratches on a polished surface making it unfunctional for interfacing nano-devices. Our motivation was to generate atomically flat metal surfaces without considering the factor of removal rate. To accomplish the goal, we developed a two step polishing scheme using two different slurries. First, we applied a low pressure mechanical polishing process using a colloidal silica (SiO_2) slurry (Cabot SS-12) and grind-reduced the size of the grains by $\sim 50\%$. Figure 2a depicts the freshly deposited Pt surface that contains multiple grains with a height of ~ 4 nm. Figure 2b depicts the same surface after conducting a mechanical polishing with 1-2 PSI pressure on a $4''$ wafer. The average grain size has been reduced from 2 nm to 1.2 nm and sharp spikes have been considerably eliminated. This polishing step involved only mechanical polishing due

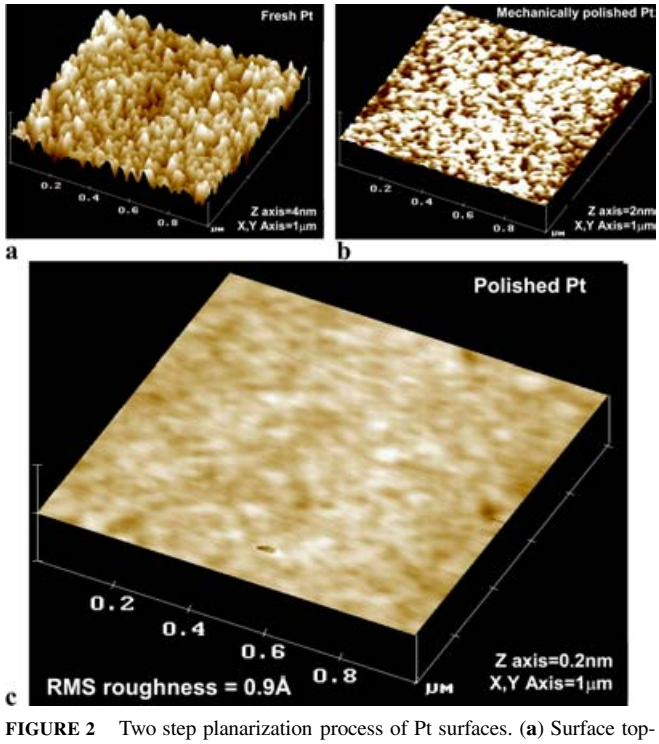

FIGURE 2 Two step planarization process of Pt surfaces. (**a**) Surface topology of freshly deposited Pt surface, which has an RMS roughness of ~ 2 nm with many grains as high as 4 nm. (**b**) Mechanically polished Pt surface. The roughness has been reduced to less than 1.2 nm and most spiky grains are flattened in this step. (**c**) An ultra-smooth Pt surface generated by the two-step CMP process. The RMS roughness of the surface is less than 0.1 nm

to the chemistry of the slurry which was designed for silicon dioxide planarization.

In the 2nd stage of polishing the Pt, we used a proprietary colloidal alumina slurry made by DuPont-EKC (ZCX-206) with a oxidizer (ZCX-206B) mixing with a ratio of 3:7. Pt is difficult to remove due to a very slow oxidation rate and require a long polish time. An average removal rate for Pt was found to be ~ 2 nm/min with a pressure of $\sim$ 2PSI on a 4″ wafer. Although the removal rate was found to be extremely slow, we observed an effectively complete elimination of roughness from Pt surfaces applying a polishing process for 1 min and achieved better than 0.1 nm RMS roughness with an average grain size of 0.5 nm as shown in Fig. 2c. A within-wafer-non-uniformity of $\sim$ 15% has also been measured. No end point detection was used in our polishing process, which was conducted using Logitech CDP equipment. The focus was to generate an ultra-smooth surface and we achieved almost atomically flat Pt surfaces.

In both the steps of polishing, we used a slurry flow rate of 250 ml/min, a rotational speed 35 rpm for both polishing plate and wafer carrier. A 50% sweeping was applied during the polishing process maintaining a low frequency. A pad (Rodel IC-1000/Suba IV) with concentric grooves and a soft bottom provided uniform instantaneous pressure distribution at the wafer–pad interface. In-situ conditioning of the pad was employed during polishing process to ensure elimination of agglomeration of slurry particles.

2.1 *Micro and nano-scratches*

A noble metal such as Pt is hard to remove due to extremely slow oxidation rate. High pressure and rotational speed with high slurry rate has been found to enhance the removal rate of Pt. However, we observed increasing density of micro and nano-scratches on the polished surfaces with increased Pt removal rate. Agglomeration of alumina slurry often causes unevenness in the slurry size which eventually contributes to surface scratches, especially during polishing processes done with high pressure.

Figure 3 depicts some scratch defects caused by large sized slurry particles. At a pressure of around three PSI, the slurry starts to form deep scratch-trenches in the wafer and sometime remains trapped in the trench at higher pressure as shown in Fig. 5. We filtered the slurry with a 2 μm filter and reduced the uneven size distribution of slurries which eventually resulted in a lower number of nano-scratches in the polished

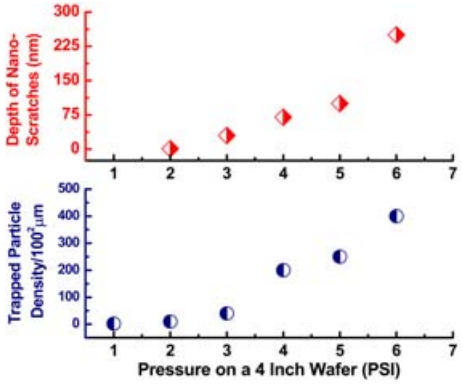

FIGURE 4 Depth of nano-scratches (*top*) and trapped particle density per 100 μm^2 area (*bottom*) versus CMP process pressure on a 4″ wafer. 2 to 3 PSI pressure was found to be good for clean and ultra-smooth Pt surfaces although the removal rate of Pt is extremely low (2 nm/min) for such pressure ranges. The lateral axis is same for both the curves

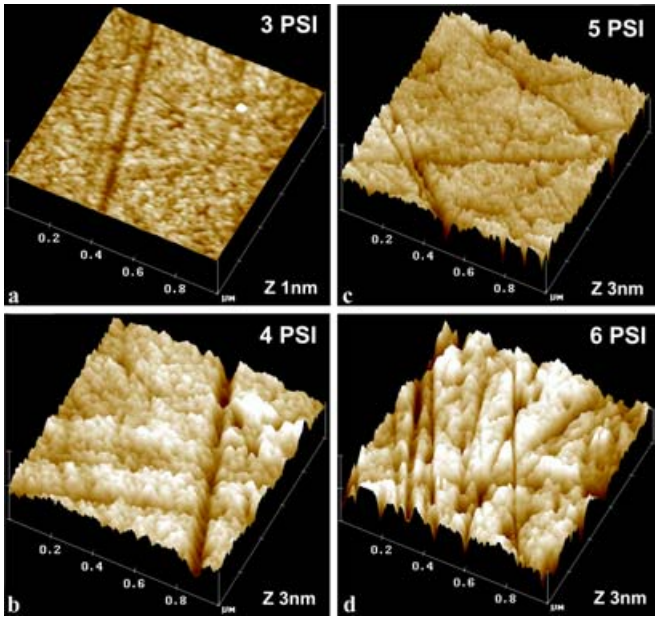

FIGURE 3 Micro and nano-scratches on polished Pt surfaces. For polishing with low pressure such as 1 or 2 PSI, shallow scratches are typically seen with a low density as depicted in (**a**) and (**b**). The scratches are also found to follow a specific orientation during a low pressure process as shown in (**a**). As the pressure is increased, the density of scratches increases. The orientations of scratches are random in (**c**) and (**d**) for polishing pressure of 5 and 6 PSI, respectively

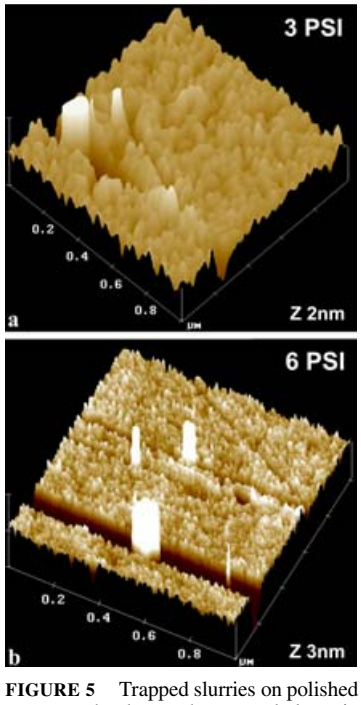

FIGURE 5 Trapped slurries on polished Pt surfaces. The higher the process pressure, the deeper the trapped slurry is embedded. (**a**) A slurry particle is trapped at the metal surface during a CMP process with low pressure of 3PSI. (**b**) Deep penetration and trapping of slurry particles on Pt surface during polishing with high pressure

Process #	Pressure PSI	Trapped particle Density/100 μm^2	Depth of nano-scratch or holes	Nano-scratch orientation
1	6	$\sim$ 400	$\sim$ 200 nm	Random with varying depths, trapped slurry
2	5	$\sim$ 250	$\sim$ 100 nm	Random with trapped slurry
3	4	$\sim$ 200	$\sim$ 70 nm	Random with trapped slurry
4	3	$\sim$ 50	$\sim$ 30 nm	Random
5	2	$\sim$ 10	$\sim$ 1 nm	Directional
6	1	$\sim$ 2	Not measured	

TABLE 1 Correlation between scratch density and depths vs. the applied pressure during the polishing processes. We used a slurry rate of 250 mL/min with a rotational speed of 35 rpm in both plate and carrier

metal surface. It is important to ensure uniformity in the size of slurries to generate an ultra-smooth surface in the polished metals. We also observed nano-holes with varying diameters in the Pt surfaces after a CMP process. Table 1 briefly correlates the process pressure with the average number of nano-scratches and their average depths. It is worth noting that although the thickness of the metal film was $\sim$ 50 nm, trapped slurries could pierce all the way through the metal film penetrating deep into the substrate which was Si wafer coated with a 100 nm thermal SiO_2 layer. Because of the extreme hardness of alumina, these types of scratches are expected when agglomeration process results in wide variation in the sizes and shapes of slurry. Figure 4 plots the depths of nano-scratches and trapped slurry particle density versus the pressure applied during CMP process. We found that two to three PSI pressure is good for generating clean and ultra-smooth Pt surfaces although the removal rate of Pt is extremely low for such pressure ranges.

2.2 *Slurry trapping on a polished metal surface*

Polishing with relatively high pressure using alumina slurry may cause the slurry particle to get trapped in the nano-scratches. We observed a pressure dependent trend in the slurry trapping phenomenon. Trapped slurries are almost impossible to remove with any surface cleaning mechanism and may contribute to serious surface defects. Some of the trapped slurries could even penetrate a few hundred nanometers deep into the substrate. This mechanical process is further aggravated by other factors such as agglomeration of slurry, pad aging, mechanical vibration in the CMP machine. It has been observed that trapped slurries makes the polishing process slower and make it difficult to generate ultra-flat surfaces. Figure 5 depicts AFM images of typical surfaces after slurry trapping takes place during CMP processes with varying pressure. Polishing at high pressure firmly traps slurry particles and any cleaning process fails to remove them.

2.3 *Degree of smoothness*

For highly smooth polished surfaces, an acceptable method for the quantification of smoothness is going to be very helpful for future applications. We propose a new figure of merit termed "degree of smoothness" (DOS) for this purpose. The %DOS can be expressed as:

$$\%\mathrm{DOS} = (\mathrm{GI}_{\mathrm{average}} - \mathrm{GF}_{\mathrm{average}})/\mathrm{GI}_{\mathrm{average}} \times 100\,,$$

where,

$\mathrm{GI}_{\mathrm{average}}$ is the average grain height prior to CMP
$\mathrm{GF}_{\mathrm{average}}$ is the average grain height after the completion of polishing.

In the ideal case, %DOS can be 100% indicating a high level of smoothness. We achieved > 85% DOS in our optimum Pt polishing CMP process with a non-uniformity of $\pm$10% on a 4″ wafer. The surface of Fig. 2b and c depicts $\sim$ 50% and $\sim$ 90% DOS respectively.

3 Post CMP cleaning of Pt surfaces

Residual slurries, abraded pad materials, metal contaminants and chemicals can introduce "yield reducing defects" in conventional semiconductor chips. For nano-device applications such as molecular electronics, residual particles are even more detrimental due to much smaller size of molecules. Typical diameter of slurry particles is $\sim$ 100 nm whereas the size of molecules is two orders of magnitude smaller. Thus, the presence of slurry or other types of contaminants on polished wafers will seriously undermine the purpose of polishing.

A cleaning process needs to circumvent further damage to a polished surface. As a very important step in the polishing process, we kept our wafers wet until the cleaning process was complete. A polished wafer is spray-rinsed with DI water without delay. We observed that if wafers are exposed to air for a few seconds, cleaning process for 100% slurry removal is impossible to conduct subsequent to metal polishing.

Post CMP (PCMP) cleaning of polished metal surface requires more than DI water rinse for removal of slurry particles. It is important to incorporate specialty chemistries to remove residual slurry, trace levels of metal residues and ions. Because of most metal's electrochemical properties, metal ions can be transported and re-deposited widely on the features of polished wafer surface. The need for reduction in rinse water consumption has been aided by recent development of effective PCMP cleaning solutions that overcome or modify the surface charge of the wafer and surface charge of the slurry particles after polishing [13, 14].

Adhesion of alumina slurry particles to a wafer surface depends on several factors such as the dimension of the slurry particle (smaller particles have larger contact area), surface roughness, chemical bonding, electrostatic forces known as the zeta potential and van der Waals forces. Slurry particles on a wet wafer surface, have electrical charges caused by ionic species H^+ or OH^-. An excess of oppositely charged ions in the cleaning solvent balances these ionic species. As a result of these two competing forces, the counter-ions form a dif-

Process #	Cleaning mechanism of Al_2O_3 (Wet wipes are used for brushing)	Average particle count/100 μm^2
1	DI water rinse	> 300
2	DI water and brush	< 100
3	Ultrasonic immersion cleaning	~ 50
4	NH_4OH pH ~ 8–10	> 30
5	Hot DI and PCMP5000, pH ~ 8–10	~ 3

TABLE 2 Particle count per 100 μm^2 for different PCMP cleaning mechanisms

fuse cloud around the particle shifting the zeta potential (z) close to zero. For alumina slurry, a pH level of ~ 8–9 brings the zeta potential to ~ zero. The electrostatic surface charges may vary as a function of particle size, ionic strength and temperature of the rinse solutions and we observed a favorable difference in the cleanliness using hot DI water mixed with a PCMP solution.

A polished wafer surface may possess metal contamination that are bonded either by ionic or covalent bonds. Ammonium hydroxide has traditionally been used to exchange NH_4^+ for the adsorbed metals, removing them from the surface. However, we did not observe a significant capability of cleaning Pt surfaces with this traditional approach.

For complete removal of the slurry and residual metal particles, we applied several methods. These include ultrasonic treatment in DI water, standard soaking and rinsing in ammonium hydroxide (NH_4OH) solution, hot DI water rinse and DI rinse subsequent to applying 10% PCMP5000 solution manufactured by Dupont–EKC (PCMP5000). A gentle brush scrubbing was applied in all cases using cleanroom wipes soaked with PCMP solutions. Particle count in all these different procedure shows a huge variation in the final polished surface with more than 30 particles per 100 μm^2 in the ammonium hydroxide solution and less than 3 particles per 100 μm^2 with PCMP5000 solution. Table 2 summarizes our observation of particle-count on a post-CMP Pt surface. For applications such as molecular electronic devices, high level of cleanliness is crucial. More research is needed for complete understanding of PCMP cleanliness of polished metal surfaces.

4 Discussion and conclusion

We developed a two step Pt polishing mechanism and achieved higher than 90% degree of smoothness with better than 0.1 nm RMS roughness. We then investigated the impact of polished Pt surface on the packing and orientation of self-assembled monolayers (SAMs) formed from alkanethiols. By growing a monolayer of alkanethiols on polished Pt surfaces and fabricating crossbar junctions using evaporated metal as top electrodes, we observed a dramatic improvement in the device yield due to ultra-smooth surfaces. In all other previous cases, we consistently observed a yield below 1% when evaporated metal contacts were used to make molecular switching devices with alkanethiols. Using polished Pt, the yield has improved to more than 35% [15, 16]. In addition, with Langmuir–Blodgett (LB) monolayer, we observed almost 100% device yields in the molecular crossbar devices. Details of the work will be reported elsewhere [17].

Our two-step polishing technique was able to generate an ultra-smooth surface with atomic flatness. However, the metal removal rate has remained extremely low throughout the development of polishing process. New slurry chemistry will be needed for faster removal of Pt without causing any degradation in the surface. A deeper level of understanding will be needed to develop polishing processes without causing nanoscratches and slurry trapping in the finished surface

We are currently working on the development of Ag and Au polishing techniques. For many applications in nanoelectronics and emerging areas bio-electronics, many new metals will play a very important role in interfacing nanostructures. Development of repeatable polishing techniques for ultra-smooth metal surfaces will open new opportunities for the nano-scale devices research community.

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