A Perspective on Nanowire Photodetectors: Current Status, Future Challenges, and Opportunities

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***Abstract*—One-dimensional semiconductor nanostructures (nanowires (NWs), nanotubes, nanopillars, nanorods, etc.) based photodetectors (PDs) have been gaining traction in the research community due to their ease of synthesis and unique optical, mechanical, electrical, and thermal properties. Specifically, the physics and technology of NW PDs offer numerous insights and opportunities for nanoscale optoelectronics, photovoltaics, plasmonics, and emerging negative index metamaterials devices. The successful integration of these NW PDs on CMOS-compatible substrates and various low-cost substrates via direct growth and transfer-printing techniques would further enhance and facilitate the adaptation of this technology module in the semiconductor foundries. In this paper, we review the unique advantages of NW-based PDs, current device integration schemes and practical strategies, recent device demonstrations in lateral and vertical process integration with methods to incorporate NWs in PDs via direct growth (nanoepitaxy) methods and transfer-printing methods, and discuss the numerous technical design challenges. In particular, we present an ultrafast surface-illuminated PD with 11.4-ps full-width at half-maximum (FWHM), edge-illuminated novel waveguide PDs, and some novel concepts of light trapping to provide a full-length discussion on the topics of: 1) low-resistance contact and interfaces for NW integration; 2) high-speed design and impedance matching; and 3) CMOS-compatible mass-manufacturable device fabrication. Finally, we offer a brief outlook into the future opportunities of NW PDs for consumer and military application.**

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I. Introduction

TRADITIONAL R&D activities in photodetectors (PDs) have been largely focused on pursuing miniaturized PDs with high responsivity, large bandwidth, short response time, low noise, and high gain-bandwidth. PDs such as p-n junctions, p-i-n diodes, phototransistors, and avalanche photodiodes are some of the depletion-mode devices widely used in photoreceivers because of their low operational voltages, high sensitivity, and high-speed properties. The absorption coefficient of the active layer material in a PD is typically $\sim 1/\mu$m. In order to ensure substantial absorption of the incident light, and thus, increase the sensitivity and quantum efficiency, the thickness of the active layer of conventional PDs has to be designed accordingly. As an example, in order to achieve quantum efficiency greater than 80%, GaAs PDs need more than 1.8-μm absorption layer thickness (when $\lambda_{\mathrm{absorption}}$ is 840 nm), which is thicker than the dimensions of most thin-film-based devices used in electronics and optoelectronics.

In contrast, detectors with thin absorbing regions are of greater interest for two reasons. First, a thinner absorption layer translates to a shorter carrier transit time and, hence, higher detector speed, although that comes about at the expense of efficiency. Second, in optoelectronic device integration, a thinner layer means greater structural compatibility with the ever-shrinking electronic devices, which could lead to new energy-optimized design options. As a strategy of enhancing photon absorption, the applications of resonant structures in the PD design have been demonstrated [1], [2]. Researchers have also developed waveguide-based detectors to get around the well-known efficiency–speed tradeoff [3], [4] and traveling-wave waveguide-distributed PDs for high power and large bandwidth [5], [6]. Unfortunately, all these approaches offer limited opportunities for device scaling, while adding layers of complexity to the issue of integration with nanoscale electronic components.

Incompatibility in different material systems has been the main barrier in identifying a unitary host material for large-scale integration of electronics and photonics. There has been an intense debate whether to integrate high-performance optoelectronics on Si, Indium Phosphide (InP), or GaAs, and

that debate did not weaken the domination of Si in electronic ICs, although several successful compound semiconductor-based IC chips were effectively integrated in communication and computing systems. The dominant role of silicon is motivating the nanowire (NW) device community to develop the technology based on Si substrate, as it helps in drastically reducing the uncertainties in investments, critical research directions, and resource allocations. Presently, the Si industry is worth about US $200 billion in revenue per year, and that is a result of the past 50 years' evolution of Si technology in design tools, circuit architecture, substrate manufacturing and epitaxy, device processing, packaging, reliability testing, and quality control. Currently, the Si industry spends around $45 billion/year [7] for R&D and this level of R&D spending is not affordable for a new material. Therefore, the integration of nanomaterials on Si will likely remain the dominant trend in the foreseeable future.

On the other hand, much higher charge-carrier mobility (as compared with that of Si), and the more efficient light-emission and absorption characteristics of compound semiconductor because of their direct bandgap (as compared with the indirect bandgap of Si), have been the two important driving forces in the development of heterogeneous devices. To enhance the emission and absorption of light in Si, researchers have attempted to manipulate Si on the nano and quantum scales [8] and to exploit its nonlinear optical properties [9]. However, it seems implausible that these devices will outperform their compound semiconductor counterparts, which currently provide the state-of-the-art optoelectronic devices for the telecommunication market. Thus, the integration of compound semiconductor and Si is crucial to achieve efficient photonic ICs (PIC).

A. New Material—Nanowires

Over the last ten years or more, parallel developments and advances in the "bottom-up" synthesis of 1-dimensional NWs (1-D-NWs) with precise control on the chemical compositions, morphologies, and sizes have enabled researchers to fabricate novel nanodevices, such as NW FETs (NWFETs) [10]–[13], LEDs [14], [15], complimentary inverters [16], complex logic gates [17], lasers [18], chemical sensors [19]–[21], and PDs [22]. Simultaneously, the current state-of-the-art silicon CMOS technology has already been scaled down to nanometer feature sizes and is approaching the physical lower limit of beneficial scaling. These trends motivate a search for new technologies that may allow widespread and cost-effective integration of NWs in devices and circuits for electronic as well as optoelectronic applications.

B. Scope of the Paper

The field of 1-D NWs like so many other emerging research fields has had its fair share of progress through "contradictions, debates, and disagreements." Lack of characterization techniques and conflicts of interpretations on the size- and shape-dependent properties of NWs, which are often very different from bulk materials, further contributed to the contradictions. Over the years, many of the earlier conflicts of interpretation have been resolved to a large degree, while others have been continuously consistent [23]–[25]. Many interesting questions still remain for NW-based devices, among them:

1) What constitutes a linear and reliable contact material for NWs [26]–[28]?
2) Can NWs be grown without catalysts and with engineered bandgaps [29]?
3) Can defect and surface-states-free NWs be grown at arbitrary crystal orientation on any surface [30]–[32]?
4) Can high-speed devices with NWs synthesized via bottom-up methods be designed?
5) Can macro-to-micro-to-nano impedance matching in NW devices be achieved?
6) Can a single NW device be used to map the performance of devices comprising an ensemble of NWs?

There have been many reviews on the field of NWs that have mainly focused on various material growth aspects, mechanisms, and techniques to control the NW crystal growth [33], [34], with the recent exception of an excellent in-depth review paper specifically dedicated to the device physics of NW PDs by Soci *et al*. [35]. In this paper, we shall try to address some of the aforementioned questions with a focus on practical realization of commercially viable NW PDs. We have explicitly identified a wide-range of literature in the field, and aim to provide the reader the overall concepts and general aspects, which are important as a starting point for a discussion on NW-based PDs for communication and sensing systems. In this manner, we hope that our paper provides an additional insight but with a different perspective. We refer the reader to the relevant papers when required, to gain further insight into the specific details of individual topics. Moreover, with the aim of stimulating the discussion around NW PDs, we have also identified specific technical challenges that are in need of urgent solutions.

C. Traditional Heterogeneous Integration

There are numerous approaches developed over the past decades for heterogeneous integration of multiple single-crystal semiconductors with different physical, electrical, and optical characteristics on a single substrate for applications in PDs. There is a significant cost to implement these technologies, and it is not clear that these are scalable and cost-effective solutions to ultralarge-scale nano-optoelectronics. Techniques, such as wafer bonding [36]–[40], epitaxial liftoff [41], [42], and heteroepitaxy [43], [44], have been developed to augment the device performance and offer new capabilities in CMOS integration. However, underlying high cost, lack of substrate flexibility, interface defects, vacancies, and traps caused by material mismatch [45], [46] remain as big challenges. In addition, all of these approaches do not address the other qualitative problems like CMOS process incompatibility and ease of design. Furthermore, the techniques commonly used in single or a few device demonstrations are likely not to be viable for dense device arrays. In short, these methods to monolithically integrate dissimilar materials may well help in integrating an optically suitable material on any substrate, there are underlying cost, reliability issues, and other physical problems that remain.

D. Nanoepitaxy and Bulk Semiconductors

Over the past three decades, researchers have been pursuing techniques for monolithically integrating an assortment of materials on a single substrate to realize high performance and ultrafast electronics and optoelectronics. Earlier attempts on the heteroepitaxial growth of materials could not be realized because of two main reasons: high lattice mismatch and large difference in thermal expansion coefficients for the dissimilar semiconductors. A large lattice mismatch results in: 1) high dislocation density at the interface and thus becomes the preferred site for impurity atoms and 2) high-diffusivity path for dopants and nonradiative recombination centers [43], [47]. The heteroepitaxial growth technique still poses many technical challenges after almost 20 years of intense research [45], [48], [49]. The physical properties of the heteroepitaxial systems are often appealing, but technological barriers remain to be overcome. Repeated top-down attempts, such as wafer bonding [38], [39] and epitaxial liftoff [50], are yet to be adapted as cost-effective and CMOS-compatible solutions.

Misfit dislocations limit the quality of lattice-mismatched heterojunctions in the case of planar thin film growth, while lattice strain, which strictly limits composition and thickness in 3-D and 2-D semiconductor heterostructures, can be significantly relaxed at the nanoscale, thus permitting a wider range of growth materials with their respective properties. For thin-film growth, the most common method to predict critical thickness of the film to be grown is based on the system's strain energy. The NW growth process is completely different from that of thin films and the strain-energy relief is favorably accommodated for coherent growth of the axial NWs with certain diameters and unrestricted lengths [51]. Therefore, nanomaterials can be grown on highly lattice-mismatched substrates because their inherent nanoscale geometries enable rapid relief of effective mismatched strain energy during the growth process [52]–[54]. Nanoscale semiconductor structures with two or three of their dimensions at the nanometer scale are rich in fundamental properties and promise revolutionary new device concepts. Homo- and heterogeneous synthesis of nanomaterials on lattice-matched and mismatched substrates have revealed a wealth of interesting properties and dramatic enhancements of magnetic, electrical, optical, and other properties [55], [56]. Devices fabricated from these nanoscale structures offer significantly improved photonic and electronic performance and, because of their small footprint, are the candidates for device-level integration with Si CMOS technology.

E. Nanowire Heteroepitaxy

With recent rapid progress in the growth of various inorganic NWs mostly using the vapor–liquid–solid (VLS) growth method developed by Wagner *et al.* in the mid 1960s [57]–[60], there have been several studies on the growth of NW heterostructures, such as InAs/InP (3.1% lattice mismatch) [61], GaAs/GaP (3.1% lattice mismatch) [62], InP/Si (8% lattice mismatch) [63], [64], Ge/GaAs (0.1% mismatch) [65], GaAs/Si ($\sim$4% lattice mismatch) [66], and Si/Ge (4% lattice mismatch) [67]. These results indicate that the lattice misfit can be effectively accommodated in NW heterostructures. However, nanoheteroepitaxy is still in the early stage for effective growth of ternary and quaternary materials that helped in making revolutionary advances in traditional optoelectronic devices in the last two decades.

Heteroepitaxial growth of NWs on Si substrates would open a new horizon for the integration of high-performance devices, since Si will remain as the ubiquitous platform for electronics for some time to come. Granted that the technological momentum is helping to provide any kind of 1-D nanomaterials on any substrate, it becomes obvious that we must now look for ways to take advantage of them in designing devices for applications in high-speed electronics, photonics, energy conversion, sensing, and imaging by incorporating a collection of materials on any substrate. The functionality of conventional electronics (e.g., CMOS technology) and photonics can be significantly augmented by using 1-D self-assembled NWs as device channels [11], light emitters, and detectors [68]–[70].

Recent advent of plasmonic [71], [72] and optical superlens (metamaterials) [73]–[76] based techniques to concentrate and guide light beyond the diffraction limit [77] into subwavelength dimensions helped realize a number of nanoscale PDs with both nanodots [72], [78] and NWs [79]. The concept of leaky-mode microcylinder resonators was used to demonstrate and explain the light-trapping phenomenon in subwavelength NWs that effectively circulate resonant photons and absorb them via multiple total internal reflections from the surface of the NW [79]. These novel techniques promise the prospect of high absorbance as well as high operating speed. A combination of these schemes along with NW heteroepitaxy could lead to the realization of substrate-independent NW PDs with high efficiency and bandwidth for future intrachip and interchip communication systems in CMOS photonics, imaging, and other detection applications [80].

In Section II, we will discuss the current NW homogeneous and heterogeneous generic synthesis mechanisms, and practical integration strategies for scalable design of NW PDs. Section III will detail some recent NW PD device demonstrations including some of the devices demonstrated in our group with the aim of highlighting a few prominent design issues. In Section IV, we identify the various technical design challenges associated with the eventual successful commercialization of these devices followed by Section V, where we conclude with a brief outlook into the future opportunities of NW PDs for consumer and military application.

II. Current NW Integration/Interfacing Schemes and Practical Strategies

In Section I, we briefly outlined the importance of NWs and introduced a sampling of NW heterogeneous integration techniques from the literature. In this section, we expand on this functionality and explore the various integration and interfacing techniques to incorporate NWs as the active photon-absorbing element in typical PDs (e.g., photoconductor, photodiode, and phototransistor). Individual and collective electrical contact to a large number of NWs for designing optoelectronic devices, such as PDs, without using nanoprobes or expensive serial interfacing procedures is a crucial issue that was addressed by numerous research groups in the past decade [81]–[85]. A massively

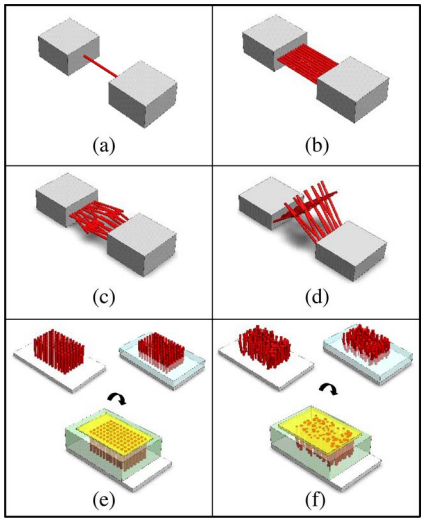

Fig. 1. Generic NW configurations using the direct growth techniques. (a) Single bridged. (b) Multiple ordered. (c) Multiple random—in plane. (d) Multiple random—out of plane. (e) Multiple ordered—vertical. (f) Multiple random—vertical.

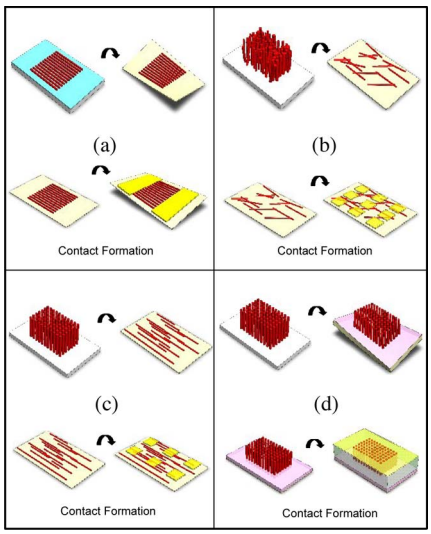

Fig. 2. Generic NW configurations for transfer-printing or pick-and-place techniques. (a) 2D-to-2D ordered. (b) 3D-to-2D random. (c) 3D-to-2D ordered. (d) 3D-to-3D ordered.

parallel, barrier-free, low-noise, and preferably "*in situ*" connections for interfacing NWs of most widely used semiconductor and oxide materials including groups IV, III–V, and II–VI will no doubt aid in the widespread application of NW-based devices well beyond PDs.

A. Nanowire Integration

The main function of integration is to ensure that either a single NW or an ensemble of NWs remains anchored in a robust mechanical attachment while simultaneously providing an electrically low contact resistance. Single-crystal semiconductor NWs are often integrated as the active element into a PD architecture using fabrication methods that can be generally classified as a direct growth technique and transfer-printing (or pick-and-place) technique as generically categorized in Figs. 1 and 2, respectively. These 1-D NWs, with their small physical size and their ability to integrate with mainstream silicon electronics in large numbers, are a better candidate for future large-scale optoelectronic integration.

B. Configurations

In Fig. 1(a)–(f), we present six commonly used configurations of a direct growth technique: a) a single NW grown between two electrodes; b) similar to a), but with multiple-ordered NWs; c) multiple NWs grown randomly in plane; d) multiple NWs grown randomly out of plane; e) vertically grown ordered NWs; and f) vertically grown random NWs. For the schemes e) and f), if a dielectric layer (template) is not present prior to NW growth, then further processing is required for electrical interfacing by depositing an insulating dielectric coating followed by a top electrode contact. For the transfer-printing or pick-and-place technique, as depicted in Fig. 2(a)–(d), there are four commonly used configurations, where the NWs are initially grown or etched on one substrate (mother substrate) and subsequently transferred to a carrier substrate. In Fig. 2(a), the original 2-D ordered "film" of 1-D NWs on the mother substrate are transferred to another 2-D ordered "film" configuration on a carrier substrate (2-D-to-2-D ordered). In Fig. 2(b), the original random vertical 3-D "film" of 1-D NWs on the mother substrate are transferred to a 2-D random "film" on a carrier substrate (3-D-to-2-D random). In Fig. 2(c), the original ordered vertical 3-D "film" of 1-D NWs on the mother substrate are transferred to a 2-D ordered "film" on a carrier substrate (3-D-to-2-D ordered). In Fig. 2(d) the original ordered vertical 3-D "film" of 1-D NWs on the mother substrate are transferred to a 3-D ordered "film" on a carrier substrate (3-D-to-3-D ordered). For configurations (a)–(d), the electrical interface can be formed with or without an additional insulating layer prior to top electrode deposition.

We will first discuss the integration achieved by growing the NWs directly in the position where they will be used. Since in this method, the catalyst material does provide some limitations on the eventual device performance and acceptance of the NW technology and its compatibility with IC fabrication (e.g., for Si photonics applications). We will then focus on the merits and remaining challenges of transfer-printing/pick-and-place method.

1) Direct Growth: For a number of interesting applications, the NWs can be most efficiently integrated when they are grown at the site, where they will be used for final device fabrication. One or both ends of the NW need to be mechanically and electrically connected while the NWs are grown, thus controlling the location and direction of the NWs. The position of the NW base is determined by the position of the catalyst nanoparticle. Lithography-based techniques, such as e-beam lithography or nanoimprint lithography, can be used to define a pattern of nanoparticles. The catalyst nanoparticles can also be formed by depositing a thin film of the catalyst material and annealing to percolate and agglomerate the thin film into nanoparticles. This method to form nanoparticles unfortunately results in a statistically widespread distribution in the NW diameter. As an alternative, preformed catalyst nanoparticles can be used to provide good control over the diameter and uniformity of the

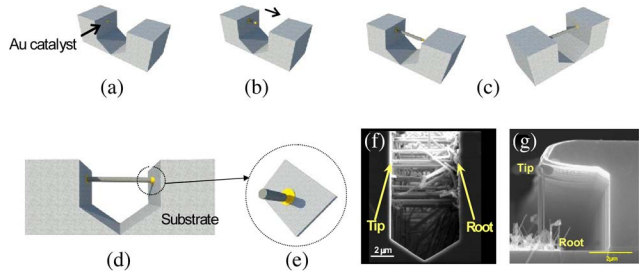

Fig. 3. (a) Angled deposition into a trench deposits catalyst onto the growth sidewall. (b) Catalyst-grown NW produces oriented NW growth. (c) and (d) Continued NW growth causes the NW to bridge the opposing sidewall. (e) As the NW continues to grow, the catalyst disperses away from the NW connection, thus crystallizing to the opposing sidewall. (f) Lateral bridging of Si NW. (g) Vertical bridging of Si NW ("nanocolonnades").

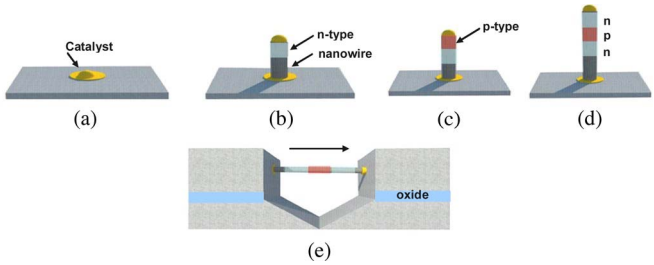

Fig. 4. NW device fabrication between opposing structures. (a) Catalyst deposited onto substrate/sidewall. (b) NW growth proceeds with undoped precursor gas and n-type dopant introduced with precursor gas. NW growth includes the n-type doping gas and NW layer developed remains n-type. (c) p-type dopant introduced in place of the n-type dopant. Grown NW now has a p-type layer. (d) Switching back and forth from n-type and p-type doping precursor gas creates n-p-n device. (e) Growth between opposing structures with this technique can produce NW devices connected between structures.

NWs [86], [87]. Nonetheless, during alloying of the nanoparticles with the substrate and other heat treatments before the start of NW growth, the nanoparticles formed by any technique can migrate and possibly coalesce, adding uncertainty to the NW position and diameter unless the thermal cycles are carefully controlled, or patterned diffusion barriers are used [88].

In 2004, we first demonstrated a technique for making one-directional silicon NW connections [89], which was coined as "bridging" growth [89]–[91]. This technique was performed by placing the growth structure opposite to the connecting structure and growing the NWs directly into the connecting structure. Upon contacting the connecting structure, continuing NW growth eventually pushes the growth through the catalyst and disperses the catalyst away from the NW tip. The NW then makes a bridge by crystallizing directly to the connecting structure without having any of the original catalyst as part of the bridging process. Fig. 3(a)–(e) shows a summary of this technique. Group IV Silicon [92], Group III–V InP [64], and Group II–VI Zinc Oxide (ZnO) [93] semiconductor NWs have been bridged by this technique. SEM images of lateral bridging and vertical bridging technique are shown in Fig. 3(f) and (g). The vertical bridging starts with an "awning" shaped structure fabricated using two doped epitaxial layers of semiconductor materials separated by an insulating layer. Vertically oriented metal-catalyzed NWs, termed "nanocolonnades," are grown from the bottom layer (bottom electrode) and epitaxially connected to the top electrode-–resembling the formation of "stalagmites" [94]. The obvious uniqueness to use bridging NW technique is the ability to directly connect structures using grown silicon NWs, whereas other processes have picked and placed silicon NWs to make similar connections [95]. One of the current challenges in a bridging process is deposition of the catalyst material only into the regions selected for NW growth. Another limitation to this technique is the ability to synthesize these NWs in a way not to damage existing prefabricated devices or to hinder their functions in any postprocessing operations. Overall, the growth of NWs on sidewalls presents new opportunities for utilizing the third dimension (thickness) of a wafer, which for the most part, remains largely unexploited. Based on this method, both surface-illuminated, edge-illuminated, and waveguide NW PDs can be designed and mass-manufactured.

The bridging technique can further be used to integrate junction as well as superlattice NWs using doping precursor gas and alternating the presence of impurity atoms in the growth chamber as demonstrated by Yang *et al.* [96], [97]. Using a similar method, Gudiksen *et al*. successfully fabricated GaP-GaAs NWs [62]. Samuelson *et al*. further demonstrated that this approach is feasible for group III–V materials by fabricating InP–InAs heterojunction NWs [98]. The uniqueness of such devices is obvious, if considered against the photon-absorption properties of silicon for laser devices [99]. Challenges for this type of heterojunction device derive from the limits of the natural lattice misalignments between III–V materials [100]. As shown in Fig. 4, if combined with NW bridging, the NW can become a device connecting two opposing structures.

Oriented NWs have also been demonstrated by Dzbanovsky *et al*. and Englander *et al*. by using an electric field between two silicon surfaces [101], [102]. An advantage of this technique is the ability to grow NWs between any types of electrodes and control the orientation. However, creating an electric field and sustaining silicon plasma between electrodes could present unique industrial challenges. Eventually, for large-scale ICs or integrated sensor applications, the "bridging" process has an added advantage to meet industry requirements of low cost and high throughput. The *in situ* fabricated NW devices offer a massively parallel, self-assembling technique that allows controllable interconnection of the NW devices between electrodes using only relatively coarse lithography.

2) Transfer Printing/Pick-and-Place: A number of different approaches have been demonstrated by several groups to connect NWs in devices and circuits, and produce large arrays as building blocks for large-scale complex systems using the transfer-printing or pick-and-place techniques. One distinct advantage this method provides is the ability to fabricate devices on plastic substrates that are lower in cost, flexible, lightweight, biocompatible, and optically transparent. In this method, NWs are either grown or etched on a starting mother substrate and then harvested or transferred onto a carrier substrate. The transfer-printing method can be done using techniques, such as dry transfer [103]–[111], wet transfer [81], [112]–[115] or contact printing [116]–[127]. Each of the submethod has its unique

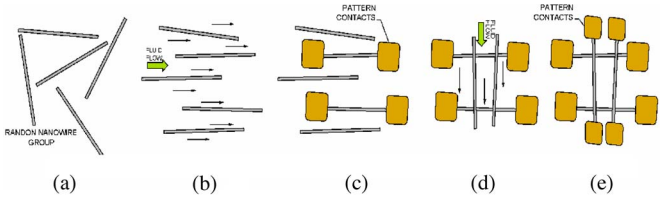

Fig. 5. Example of fluid-assisted NW transfer assembly for producing connections to NWs. (a) Large group of unattached, randomly dispersed NWs on a substrate. (b) NWs are moved and oriented to a single direction by a flowing fluid. (c) Where devices are to be made, selective contact fabrication is performed at both ends of the nanowires. (d) Second set of NWs is then exposed to a flowing fluid, where the direction of the fluid is orthogonal to the patterned NWs. These NWs are intended to be carried and oriented by the flowing fluid and eventually rest on top of the underlying NW devices that have prefabricated contacts. (e) After patterning contacts on the second set of NWs, a device having multiple contacts is realized.

practical challenges and advantages in implementing NW-based devices.

A noteworthy approach of Lieber *et al.* has been at the center of high interest in the NW community [128], [129]. A solution-based hierarchical organization of NW has been demonstrated by the group in order to develop building blocks for nanosystems. An ingenious method of aligning NWs with controlled nanometer to micrometer-scale separation using the Langmuir–Blodgett technique helped transfer the pregrown NWs to planar substrates in a layer-by-layer process to form parallel and crossed NW structures over centimeter-length scales. Subsequently, an efficient patterning method was used to connect the arrays to electrical contacts of controlled dimensions and pitch using photolithography. Diverse applications for enabling a broad range of functional nanosystems have been demonstrated by the group.

In many of the wet transfer demonstrations, NWs were assembled after growth into parallel or crossed arrays by the alignment aided by fluid flow or by applying electric fields as schematically depicted in Fig. 5. Generally, NWs are removed from their original growth locations and dispersed in a liquid, and then transferred to a substrate. Further processing was then required to produce the device structures. This whole procedure, especially the removal and transfer, is time consuming and limits the yield. In almost all cases, electrical contacts were defined with electron-beam lithography on a few selected NWs [130], [131].

Other heterogeneous transfer techniques have been pursued by Rogers *et al.* who have demonstrated the transfer of microstructured single-crystalline silicon ribbons from a silicon-on-insulator (SOI) substrate using polydimethylsiloxane (PDMS) and a soft lithography process to remove structures that were fabricated via planar 2-D dry printing or in combination with wet etching process [116], [117], [121], [123], [132], as depicted in Fig. 6, while Javey *et al.* [109] transferred Si NWs grown on a Si wafer surface via a friction-assisted contact transfer process onto a 2-D surface. Although connecting electrodes to NWs one at a time contributes to understanding the characteristics of NWs and exploring novel device applications, it cannot be used for reproducible mass-fabrication of dense, low-cost device arrays.

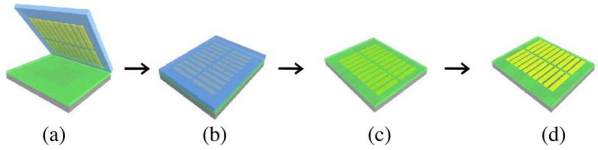

Fig. 6. Example of dry-transfer printing (2-D to 2-D). (a) Carrier substrate (bottom) and the mother substrate (top) are aligned. (b) Two substrates are pressed together. (c) and (d) Transferred structures are then postprocessed and electrical contacts deposited (Adapted from [116]).

All of the earlier cited transfer methods either do not preserve the vertical orientation of the nanowire/pillar array order on the carrier substrate, or cannot be directly translated to vertical process integration, and have been limited to 2-D single-crystal film transfer. Of interest is the possibility of having vertically oriented micro-/nanoscale wires/pillars via transformative "top-down" or synthetic "bottom-up" methods of a variety of materials while consistently preserving the array morphology and order, and subsequently coating a target substrate (ordered 3-D-to-3-D). Spurgeon *et al.* [134] grew arrays of Si NWs on a Si surface and covered the substrate with a PDMS polymer film that was later removed by scraping with a blade. This mechanical removal process still has many challenges in the process of repeatable mass manufacturing on a large area, although the concept of NW mother substrate reusability was clearly validated.

In contrast, we have recently demonstrated such a technique to harvest and transfer vertically aligned single-crystal-semiconductor micro- and nanopillars from a single-crystal substrate (mother substrate) to a low-cost carrier substrate while simultaneously preserving the integrity, order, shape, and fidelity of the transferred pillar arrays [135]. The transfer technique is based on a vertical embossing and lateral fracturing method employing a transfer polymer while ohmic contact formation for electrical addressing was achieved using a composite of metals and/or conducting polymer. The capability of this process was demonstrated by fabricating Si photoconducting devices (area of 25 mm^2) on a glass and polymer surface with a low fill factor contributing to lower leakage current, reduced parasitic capacitance, and higher efficiency of light absorption. The approach offers a more generic method in that the ordered array of the 3-D micro-/nanostructures are preserved in their vertical orientation (direct 3-D-to-3-D) after transfer while increasing the volume density of the final device. There are no restrictions to use any specific starting mother substrates or carrier substrates (such as SOI as was required by others) and involve ambient- and/or low-temperature processes ($<250\,^{\circ}C$). The choice of the transfer polymers (mainly insulating polymers) from off the shelf are not limited to PDMS, polymethylmetacrylate, polyimide, polystyrene, polycarbonate, or SU-8.

Fig. 7(a) and (b) illustrates the comparison between the 3-D-to-3-D-ordered transfer methods and a possible realization of a multiwavelength image sensor from this technique [see Fig. 7(c)]. The SEM images of the fracture-transferred pillars on the carrier substrate and the surface of the mother substrate are shown in Fig. 8. In summary, this approach offers several important features such as:

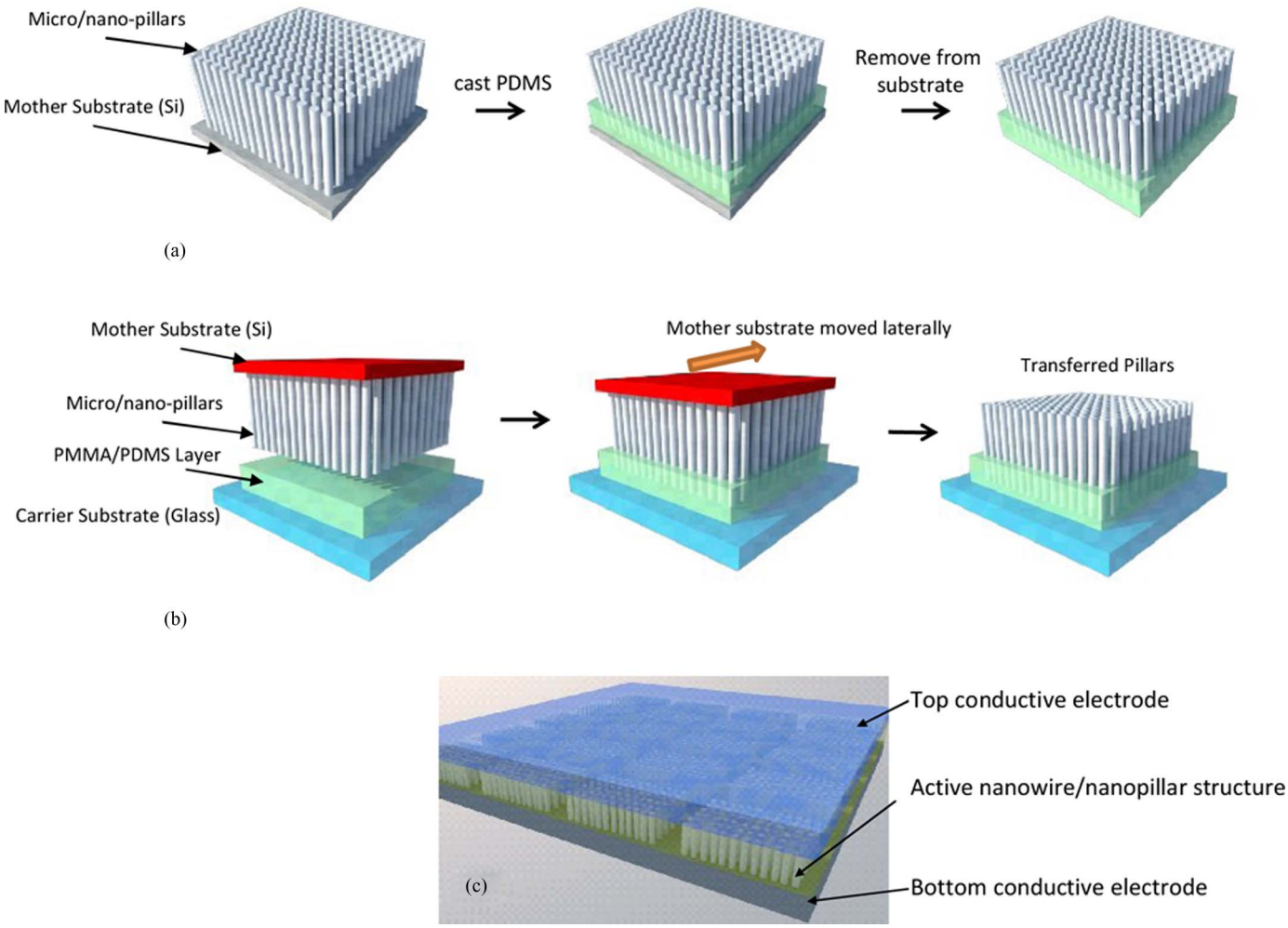

Fig. 7. (a) Transfer of Si NWs from mother substrate into a PDMS layer via doctor blade scraping (adapted from [134]). (b) Transfer of NW via fracture using a polymer transfer layer (adapted from [135]). (c) Illustration of a possible photon-trap imaging device from the above transfer schemes. An ensemble of NW devices can be collectively transferred and interfaced with individual pixels of a read-out integrated circuitry for designing image sensors or a focal-plane array.

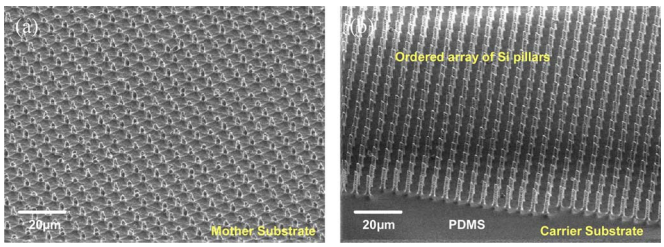

Fig. 8. (a) SEM images of mother substrate after transfer printing and (b) fractured transferred Si pillars on PDMS-coated carrier substrate.

1) Low-temperature device fabrication with highly crystalline materials that reduces the impact of thermal expansion and shrinkage. This becomes critical when devices are fabricated on plastics, sheet metal, and other low-cost substrates, and in a multilayer-stack with different semiconductors.
2) Lower leakage current and reduced parasitic capacitance, potentially from the low fill factor.
3) Effective photon-trapping and absorption leading to higher efficiency.
4) Reusability of expensive substrate for repeated reproduction of 1-D nanowires/pillars contributing to significantly reduced material consumption.

III. Recent Device Demonstrations

The applications of NWs in photonics have been detailed in [136]–[142]. In this section, we review the recent literature on NW PDs using either a single NW or an ensemble of NWs, as the active optical element is designed based on the approaches described in Section II. We can categorize the devices reported so far, although this categorization is incomplete, and some items could also appear in multiple categories.

A. Review of Various NW PDs

1) NW PDs via Direct Growth: A range of substrates have been used in the manufacturing of NW-based devices ranging from semiconductor crystalline wafers, with or without seed templates, metal foils (e.g., stainless steel) [143], glass [144],

quartz [66], and flexible rubber [145]. In the direct growth approach, Tsakalakos *et al*. [143] grew randomly oriented Si NWs on a metal foil at 600 °C–800 °C using a Ta_2N buffer layer. Based on a similar approach, we demonstrated an ultrafast photoconductor on silicon dioxide substrate with a response above 30 GHz [22]. Chueh *et al*. grew Ge NWs directly on low-temperature substrates, including plastics and rubber [145].

The following are some examples of NW-based PDs of different materials demonstrated via the direct growth method: NWs of InAs [147], NWs of Si [148]–[152], nanorods of GaN [153], InP NWs/polymer hybrid photodiode [154], InN nanorod/poly(3-hexylthiophene) hybrids [155], NWs of nc-CdSe [156], NWs of Ge [157], random network of silicon NWs [158], nanostructured amorphous-silicon (a-Si:H)/polymer hybrid photocells [159], nanopillars of GaInAs/InP [160], NWs of GaAs [161], NWs of GaN [162], NW network of ZnCdSe [163], nanorods of In_2S_3 [164], GaN NW pin photodiode [165], nanorods of ZnO [166]–[169], silicon NW phototransistor [170], [171], and nanorods array of p-GaN/InGaN/n-GaN [172].

2) NW PDs via Transfer Printing: There have also been equal efforts on NW PDs fabricated on carrier substrates from transfer-printed/pick-and-place techniques. Photoresponse from InSe NWs has been shown by Wang *et al*. [173] who synthesized InSe NWs without catalyst via a physical vapor transport system in a horizontal tube furnace with In_2Se_3 as the precursor. Huang *et al*. [146] embedded Si NWs into a polymer [poly(3-hexylthiophene)] for enhancing the performance of hybrid photovoltaic devices. Zhai *et al*. [174] pursued a similar thermal evaporation method but with Au nanoparticle catalyst. Others include InP NW PDs [136], NWs of CdTe [175], ultraviolet PDs based on single GaN nanorod p-n junctions [176], InAs/InAsP NWs [177], aligned assemblies of core-shell CdSe/CdS nanorods [178], Ge NW with CdS nanoparticle heterojunction [179], single InP NW devices with back-to-back Schottky barriers [180], Se NWs [181], Ge NW PDs [182], [183], InSb-NW-array PDs [184], CdZnS NW networks [185], metal-semiconductor-metal PDs made from an individual CdS NW [186], Ge NW Schottky PDs [79], [187], Bi_2S_3 NWs [188], 3-D-to-3-D-transferred Si photoconductor [135], and InP NWs [189].

B. InP NW PDs on Amorphous Substrates

Kobayashi *et al*. [144] introduced a new method of incorporating III–V NWs on a nonsingle crystalline surface that directly relaxes any lattice-matching conditions, and reported the demonstration of a device for high-speed photodetection based on InP NWs grown in the form of nanobridges [92] between prefabricated electrodes of hydrogenated microcrystalline silicon (μc-Si:H) deposited on an amorphous SiO_2 surface [32], [66], [190].

Fig. 9(a) and (b) depicts an illustration of the NW photoconductive device integrated on a high-speed coplanar waveguide (CPW) transmission line with 50-Ω characteristic impedance to facilitate dc and high-frequency measurements. A close-up illustration of the active photoconductive region is shown in Fig. 9(c) and (d), which consists of a number of intersecting InP NW photoconductors over a 2-μm gap. That device was characterized to have a de-embedded temporal response of 14-ps full-width at half-maximum (FWHM) when triggered by a 780-nm laser pulse [22].

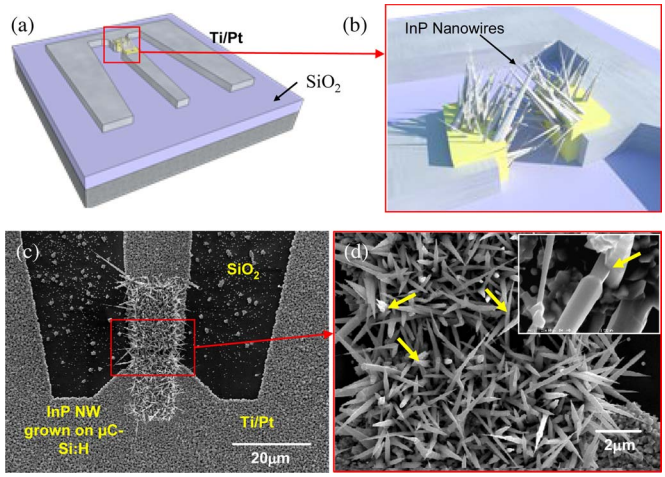

Fig. 9. (a) and (b) show the illustration of the high-speed InP NW photodetector. (c) SEM image of InP NWs grown randomly on the μc-Si:H electrodes because of the lack of long-range translational crystallographic symmetry. The air-bridged NWs form the photosensitive "active device area." (d) Enlarged view of the device active area. Arrows indicate the fused nanobridges forming a closed resistive current path. Inset: detailed view of a "weld."

First, the CPW pattern was made with a 3-nm Ti film and a 100-nm Pt film on a 2-μm thermal oxide (SiO_2) thermally grown on a silicon substrate. For the InP NW seed template, a 500-nm-thick n-type hydrogenated silicon film (n-Si:H) (achieved with phosphorus doping) was deposited by plasma-enhanced chemical vapor deposition (PECVD) onto the patterned Pt/Ti electrodes at ∼400 °C with source gases of silane (SiH_4), hydrogen, and phosphine (PH_3). The template electrode was then formed leaving two isolated segments of n-Si:H, but electrically connected to the Ti/Pt electrodes only in the active PD regions. The NW catalyst was deposited with a suspension of colloidal gold with ∼10 nm diameter in toluene. Using a low-pressure metal organic CVD (LP-MOCVD), the deposited InP grew into randomly oriented InP NWs formed selectively onto the n-Si:H segments, as shown in Fig. 9(c). Although the NWs grew randomly, a significant number eventually "welded" as they grew toward each other across the n-Si:H gap segments, thereby establishing electrical continuity over the gap between the two n-Si:H segments. Detailed characteristics of the material growth are reported in [144].

Fig. 10 shows the schematic of the setup and measured pulse response when the device, with a gap of 0.7 μm, was biased at 1 V using a 45-GHz bias-T. The photoresponse signal was extracted through a CPW microwave probe (Cascade Microtech GSG-50). For the high-speed characterizations, we used a pulsed-laser source from a mode-locked fiber laser (Calmar Optcom) having a wavelength of 780 nm, total output power of ∼90 μW, a pulsewidth of 1 ps, and repetition rate of 20 MHz. Using a single-mode lensed fiber tip on a microwave probe station, the laser pulse was focused from the top surface via

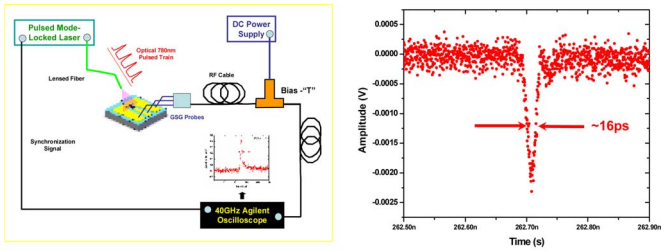

Fig. 10. (a) Schematic of the high-speed temporal response experiment. (b) Pulse response ($\tau_{\mathrm{meas}} \sim 16$ ps), $\tau_{\mathrm{actual}} \sim 11.4$ ps of the InP NW photoconductor (0.7 μm gap) triggered by ultrashort 780-nm laser pulses of width 1 ps.

free-space coupling onto the active region of the photoconductor. The center of the laser beam was aligned with a translational stage to maximize the photocurrent of a device within an area of 10 μm $\times$ 2 μm. The resulting photoresponse electrical pulses were observed on a 40-GHz oscilloscope (Agilent 86109A).

The actual response time for the NW PD can be extracted based on the following equation from [191]:

$$\tau_{\mathrm{meas}} = \sqrt{\tau_{\mathrm{actual}}^2 + \tau_{\mathrm{scope}}^2 + \tau_{\mathrm{optical}}^2} \tag{1}$$

where τ_{meas}, τ_{actual}, τ_{scope}, and τ_{optical} are the measured, actual, oscilloscope, and optical pulsewidths in time, respectively. The measured FWHM from the oscilloscope was 16 ps and considering the 11.2-ps FWHM response for the 40-GHz oscilloscope and the laser pulsewidth of 1 ps, the device's temporal response was estimated to be 11.4 ps at 780 nm. The response estimate is conservative, since we have neglected the microwave components and laser timing jitter that contribute to the measured pulsewidth.

C. Waveguide-Integrated Si NW PDs

Grego *et al.* recently reported the first monolithic waveguide-integrated photoconductors with Si NWs on an amorphous substrate [192], [193]. This is significant because it will enable new building blocks for a self-contained CMOS-compatible photonic chip for both light guiding and detecting capability for high-speed optical interconnects [194]–[200]. NWs have been shown to have the capability to waveguide photons [201]–[207] and plasmons [200], [208]–[210], and therefore, besides photodetection, they may also act as waveguide bridges between two waveguides integrated into optical interconnection devices.

As shown in Fig. 11(a)–(c), the PD comprises a passive optical waveguide designed for guiding 780-nm photons and laterally oriented photoconducting Si NWs. The waveguide is designed with a SiO_xN_y core layer and an amorphous SiO_2 cladding layer. Deep trenches were patterned in the waveguides by reactive ion etching (RIE). Subsequently, a highly p-doped polysilicon layer was deposited selectively on the vertical sidewalls of the trenches by a directional RIE-based etch back after a conformal thin film deposition. A selective deposition of Au film on the sidewalls at a tilt angle was done for catalyst-assisted NW growth. By employing a VLS method, undoped Si NWs were grown at 680 °C from the annealed Au thin-film catalyst.

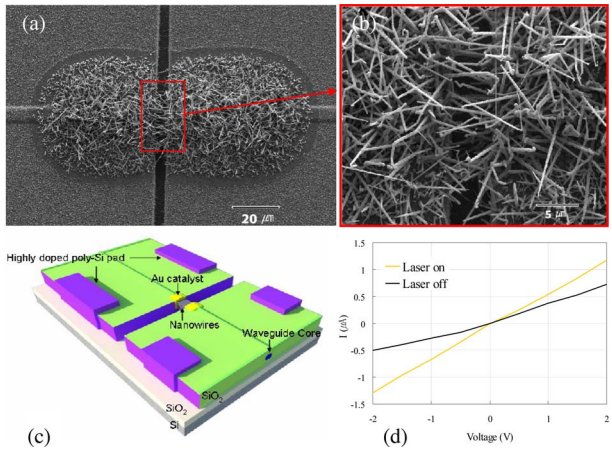

Fig. 11. SEM images for NW-integrated waveguide device grown at 680 °C. (a) Top view of the microtrench with bridged NW and catalyst pads with NWs grown on the vertical sidewalls as well as on top of the upper cladding of the waveguide. (b) Close-up view of bridged NWs. (c) Schematic of the waveguide photodetector. (d) *I–V* characterization of waveguide-integrated NWs photoconductors across a 7-μm trench when illuminated with a 2-mW laser input of wavelength 780 nm.

The NWs were grown without any globally specific orientation, since the growth template is polycrystalline silicon.

The device photoresponse was measured by probing the two electrodes bridged by the Si NWs while coupling the waveguide with a 2-mW laser input of 780-nm wavelength . The NW density that bridges the waveguide trenches was controlled by varying the diameter of the NW. Higher densities were achieved with NWs of an average diameter of $\sim$100 nm as compared to lower densities with much thicker diameter NWs of $\sim$900 nm. The devices with thicker NWs (low density) showed a much smaller increase in its photoresponse when normalized to the dark current at a bias of 5 V. This can be attributed to lower number of bridged photoconducting NWs and higher optical power loss by light scattering. On the other hand, devices with dense thin NWs showed much less reflectance and higher photosensitivity. The responsivity of the dense thin NW sample was about 0.03 A/W at 5-V bias for a waveguide illumination of 300 μW.

Considering the NW's doping concentration (nominally undoped) and the density of bridged connections [211], the dark current level of the devices seems much higher than that of a Si-NW PD fabricated by RIE using Ni nanodots as a mask [212]. This leakage current is most likely due to the surface states and defects on the NWs and un-catalyzed growth of thin films between the electrodes (e.g., amorphous and nanocrystalline Si on the NWs as well as on the substrates). Such an un-catalyzed film generates leakage paths among different terminals of a device as well as among adjacent devices in a wafer resulting in higher noise and crosstalk [90], [213]–[215].

In order to reduce the surface states of Si NWs, many experimental efforts have focused on high-temperature annealing and hydrogen passivation [216], [217]. The process of doping the NWs can directly contribute to higher carrier concentrations and possibly prevent complete depletion of the NW, and hence provide a stronger surface electric field for the effective

separation of carriers at the surface [218]. This procedure instead may increase the risk of leakage paths due to the uncatalyzed growth of polysilicon. By reducing the NW growth temperature, the uncatalyzed polysilicon deposition on the substrate and on the NW may be reduced as well. Moreover, the lower growth temperature results in a decrease of the average NW diameter, thus reducing the reflection of the incident photons [219]. However, thinner NWs are more prone to being completely depleted [220]. The tradeoff between leakage current and photoconductivity should be considered for optimizing the performance of waveguide integrated NW PDs.

The photodetection results presented in Fig. 11(d) demonstrate the feasibility of NW-integrated active optoelectronics devices fabricated with a scalable process. The photodetection performance can be improved in devices by using doped Si NWs, as opposed to the intrinsic Si used for this study, as well as the optimization process. The electrical probing of the devices is complicated by parasitic resistance at interfaces as demonstrated by the differences in two- and four-terminal measurements. Efforts are currently underway to improve the electrical contact with a new device design layout.

Further progress in this device requires an understanding of how passive waveguides and NWs interact with photons at the optical index transition, and how propagating optical modes from a micrometer-size waveguide switches to nanoscale semiconductor wires, and the impact of misorientation and nonuniformity in the distribution of the NWs. Investigation on the effects of light scattering, photon trapping, and absorption with the use of index-matching material may assist in improving the performance of these devices [142], [219], [221]–[223]. Photon propagation in a waveguide carries a specific polarization and as such NWs oriented along the direction of the waveguide will demonstrate varying coupling efficiency for different polarizations [34], [189], [224]–[228]. Hence, it is also important to optimize the polarization preference of both the waveguide and the NWs for optimum performance.

D. Oxide-Based NW PDs

1) Zinc-Oxide-Based PDs: ZnO NW devices are an important class of PDs. Due to their wide bandgap (3.37 eV at room temperature), diverse processing technologies, and the capability of operating at high temperatures and in harsh environments, ZnO NWs are attracting a lot of attention for the realization of transparent conducting electrodes and UV PDs. 1-D nanomaterials, such as NWs [85], [229], nanorods [230], and nanotubes [231], have stirred up interest because of the wide range of applications and possibilities. Although this section will primarily focus on PDs, ZnO NWs are also significant in gas and chemical sensing due to the strong influence of surface chemistry on the conductive and photoconductive properties inherent in ZnO [232]–[234]. ZnO NWs have also been used in making dye-sensitized solar cells [235]–[237], FETs [238], [239], and biosensors [240] among other devices.

2) Mechanism of Photodetection in Metal Oxides: High photoconductive responses have been observed upon exposure to UV light and relates to 4–6 orders of magnitude decrease in resistivity [241]. Relatively long relaxation time has also been observed, which relates to carrier trapping. The density of the defect states is known to have a significant effect on the photocarrier lifetime and photoresponse speed [242]. It is widely accepted that enhanced photosensitivity in ZnO NWs is due to oxygen molecules adsorbed onto the ZnO surfaces that captures free electrons from n-type ZnO [241], [243], [244]. Light polarization dependence of the photoconductivity has been observed for SnO_2 [245], $ZnGa_2O_4$ [246], β-Ga_2O_3 [247], MgZnO [248], V_2O_5 [249], and In_2O_3 [250]. These are especially important for the development of visible-blind PDs.

3) Growth Methods: Highly dense vertical ZnO NW arrays allow for larger surface coverage so that larger photocurrent signals can be detected. In order to fabricate highly dense NW arrays, usually ZnO buffer layers are deposited onto a substrate by CVD methods. The ZnO NWs are then coated by filling material, such as spin-on-glass, to allow deposition of the top electrode to prevent electrical shortage. ZnO NWs produced by CVD technology have been used by many groups for a large variety of PD applications [85], [244], [251]–[253]. NWs grown using the CVD method show that for a certain selection of synthesis conditions, the conductivity of ZnO NWs are sensitive to UV light exposure. This method, however, requires time-consuming, step-by-step fabrication techniques, which makes them challenging for large-scale manufacturing purposes.

Liang *et al*. grew high-quality ZnO epitaxial films on sapphire substrates to make UV PDs, which exhibited microsecond-scale response speed [254]. Achieving such high crystal quality of ZnO thin films is still challenging because no high-quality and low-cost substrates still exist for lattice-matched growth. These thin films are usually deposited by MOCVD, pulsed-laser deposition (PLD), or RF-sputtering techniques. ZnO thin-film photosensitivity also depends heavily on stoichiometry, trap densities, and gas adsorption and desorption on the crystal surfaces. A very slow response time of UV PDs (few minutes to several hours) is often seen in polycrystalline ZnO thin films [255]–[257].

ZnO NWs are relatively easier to synthesize than other metal oxide materials, such as gallium oxide (β-Ga_2O_3) [258], zinc gallate ($ZnGa_2O_4$) [246], and MgZnO [248], and as such, they are of great technological interest for the development of detectors that have an abrupt long-wavelength cutoff at $\sim$370 nm. These visible-blind PDs have responsivity values as high as 0.009 A/W at 360 nm. Fabrication of ZnO nanodevices using current lithography techniques to form metal contacts to both terminals of a single or an array of ZnO NWs has been thoroughly researched. To improve photoconductivity using this method, a theoretical and experimental study by Prades *et al*. [259] has suggested that following different fabrication strategies, such as diminishing the distance between the electrical contacts, increasing the width of the photoactive area, or improving the electrical mobility of the nanomaterials, enhances the response of photoconductors.

Solution-based processes have certain advantages over the conventional crystalline semiconductor devices in terms of ease of fabrication, large device area, growth on flexible substrates, and extremely low cost [168], [243], [260]–[262]. Of these,

Fig. 12. Growth of NWs via sonochemcial method on a wide variety of common substrates such as Si- and Cr-coated substrates. A seed layer is first deposited and NWs are observed to grow from the deposited seed layer.

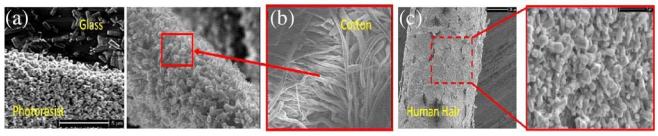

Fig. 13. ZnO NWs grown on (a) photoresist, (b) cotton, and (c) human hair. Such growth flexibility paves the way for multiple applications, especially in piezoelectric nanogenerators.

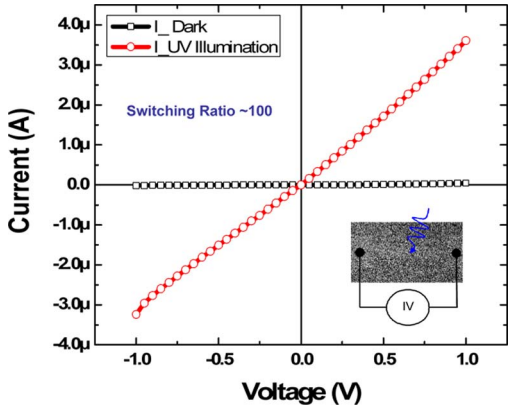

Fig. 14. Current-voltage *I–V* characteristics of a network of ZnO NW photodetector formed by sonochemical growth on prepatterned electrodes on SiO_2 with and without UV illumination (365 nm at 0.3 mW/cm^2). The inset shows the test schematic.

the most widely reported is the hydrothermal, hot-plate method [237], [263]–[265]. Unlike the vapor-phase synthesis method, the hydrothermal method of growing ZnO NWs can be performed at much lower temperatures. The reaction time required for this synthesis of ZnO NWs, however, can take several hours (or even days) [265].

The sonochemical method for growth of ZnO NWs has received little attention in recent years. For fast process, high density, uniform growth of ZnO NW on virtually any substrate, we use a simple and inexpensive method of growing ZnO NW in less than 30 min at ambient conditions. This allows for fast production of ZnO NWs for device applications, such as gas sensors [233], hybrid p-n junctions [266], UV PD [262], and other devices [235]. We recently reported on the sonochemical technique to deposit a ZnO seed-layer and grow ZnO NWs using a single step [261]. This technique allows us to deposit on virtually any substrate that can withstand alcohol and/or water treatment. In Fig. 12, we show the ability to synthesize vertically oriented ZnO NWs on Si- and Cr-coated substrates (a cross-section of ZnO NWs grown on Si is also shown).

Fig. 13 shows the results of ZnO NW growth on unconventional materials, such as a polymer, cotton, and even human hair using only an aqueous growth solution with an average growth rate of ∼600 nm/h. Compared with other room-ambient methods, this growth time is significantly smaller than other reported sonication syntheses [168]. Our growth rate is >10 times faster than that of conventional hydrothermal methods, which has a growth rate of ∼40 nm/h [265]. We fabricated a ZnO NW PD using the sonochemical method with the same chemistry as for the samples depicted in Fig. 13 and the device demonstrated a large photoresponse to UV light (shown in Fig. 14).

4) Challenges: Significant progress has been made in the past few years in the area of UV-photodetection, electronic, and optical properties, and assembly of devices based on ZnO NWs. Although the sonochemical method allows for ZnO NW growth on virtually any substrate, there is less than desired control over the direction of growth and aspect ratio of these NWs. Fig. 12 shows the aspect ratio of ZnO NWs to be closely comparable to the hydrothermal method [267], [268].

Interesting applications and devices can be envisioned, if a simple and cost-effective process can be developed for precision p-doping of ZnO NWs. Successfully, p-doping ZnO material has been a severe challenge, even for other synthesis techniques [269]. A more controlled method of growth, which precisely allows us to grow ZnO NWs in place will impact the cost and device fabrication. To address this challenge, self-patterned NW growth [253], transferring techniques [270], dielectrophoresis alignment [271], magnetic alignment [272], and other techniques [273]–[275] are currently being used. Due to the complexity and cost of these processes, it would be difficult to implement this at a large scale. A fast, inexpensive process to grow highly dense ZnO NWs with precise positioning and control of aspect ratio and density should be further investigated.

5) Recent Development and Future Prospects: Recently, there has been interesting developments over ZnO NWs response to white light irradiation ($\lambda > 400$ nm). Liu *et al*. [276] reported a series of measurements on a ZnO-NW-based FET device, which has response to visible light under different environments (air, vacuum, N_2, and O_2). ZnO:P NWs can play an important and significant role in optoelectronics, since these NWs can be changed from n-type to p-type with an increase in phosphorus concentration [277]. If a feasible and rapid process is developed to dope ZnO NWs with higher concentration, it would rapidly change the way that ZnO NW PDs are deployed in complex systems.

Hybrid nanostructures are showing signs of improvement in recent years. NW photodiodes composed of ZnO core/ZnSe shell on transparent conductive oxide substrate [278] have stirred up a lot of interest for solar power conversion applications [140], [279]. Hybrid structures, like those fabricated by Ok *et al*. [280], can harness the attractive properties of ZnO NWs and carbon nanotubes (CNTs) along with high volumetric efficiency over large areas. This can potentially allow for large 3-D integrated nanonetworks. With the hierarchical assembly of nanostructures with exquisite spatial control, new optical

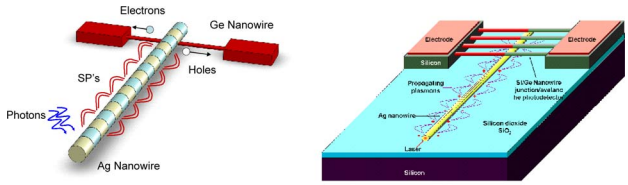

Fig. 15. (a) Schematic representation of a Ag NW, acting as a launching pad for SPs and a crossing Ge NW, which supports an electrical current whenever electron–hole pairs are excited by the SP electric field at the Ag–Ge contact (adapted from [295]). (b) Schematics of a possible distributed photodetector based on Ag NW coupled into a series of NW photodetectors for efficient detection of SPPs.

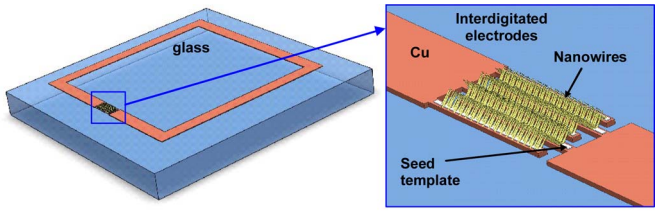

Fig. 16. (a) Schematic of an integrated single SRR unit cell with interdigitated gap on glass substrate for integrating ultrafast photoconductive NW switches. (b) A close-up view of the interdigitated gap electrode showing the intersected NWs on seed template.

and electronic [241] applications ranging from biological [240], chemical sensing [233] to imaging [281] can be achieved.

E. Plasmonic NW PDs

An exciting new research area in nano-optoelectronics is represented by NW plasmonics that promises high integration density of nanophotonic devices. When free electrons on the surface of a metal NW are impinged by light of a specific wavelength, they generate a surface plasmon polariton (SPP), a surface wave resulting from collective electron oscillation. SPPs can propagate for long distances along metallic NWs, provided they do not encounter any defects in the structure [282]–[285]. Ongoing efforts are directed toward the development of nanoscale photonic circuits based on integration of NWs with propagating SPPs that represent localized light below the diffraction limit. Controlling surface plasmons and guiding them through a specific path could lead to the optical equivalent of electronic circuits.

In the recent past, several methods for miniaturizing the size of optical waveguides with plasmonics have been reported including particle arrays [286], [287], thin metal films [288], [289], and metal NWs [290]–[292]. Silver NWs have unique properties that make them particularly attractive for nanoscale confinement and guiding of light to nanoscale objects due to their smooth surface that contributed to lower propagation loss than metallic waveguides fabricated by electron-beam lithography [293]. For practical applications in a system, plasmonic waveguides need to couple light to a nanoscale detector, and researchers proposed nanodots [294] and NWs [295]–[297] as potential candidates for plasmonic detection schemes. Falk *et al.* demonstrated a NW plasmonic PD that consists of a silver NW ($\sim$100 nm in diameter) that acts as a plasmonic waveguide and a crossing Ge NW that is connected to two metal pads, as shown in Fig. 15(a) [295]. When SPPs guided along the Ag NW to the Ag–Ge region excites electron–hole pairs in the Ge NW, it results in a detectable current between the electrodes. A calculated energy transfer of 23% is achieved using a single Ge NW photoconductor.

The current pick-and-place approach allows the coupling of one semiconductor NW to a single Ag nanorod. A process that allows the coupling of a single Ag NW to multiple semiconductor NWs can be developed based on the NW bridging method [89] as depicted in Fig. 15(b). To achieve this, a plasmonic waveguide via Ag NW or nanoribbon can be positioned using several methods including DNA-templated metal NW synthesis [298], [299]. Ag NWs can be physically positioned either below or on the surface of the detectors subsequent to the detector fabrication. For the characterization of the SPPs detectors, cylindrically symmetric SPP can be launched by illuminating the farthest end of the Ag NW with a tunable laser, while the detectors can be monitored for SPP-induced photocurrents. This device will be analogous to a distributed PD [300]. This arrangement of distributed SPP detectors will allow an uncoupled and undetected SPPs in the first NW to be detected in subsequent NWs connected in series along the direction of the metallic NW waveguide. Multiple NWs along the axial direction are expected to enhance the efficiency to above 90% by absorbing uncoupled/undetected SPP in a series of NW detectors.

F. NW PDs for Metamaterial Applications

Semiconductor nanostructures (NWs, nanotubes, nanopillars, nanoneedles, nanorods, etc.) may also offer numerous opportunities for nanoscale optoelectronic and emerging negative index metamaterials devices [301]. The integration of these semiconductor nanostructures, with passive and active metamaterials would be of great interest in modulation and switching applications. In this section, methods to incorporate nanostructures with split-ring resonators (SRR) via nanoheteroepitaxy will be briefly described. NWs of silicon (Si) were grown using the VLS method with a nanocrystalline seed template (as described in Section III-B) while ZnO NWs were grown using sonochemistry (as described in Section III-D). The NWs can be grown in between the smaller split gaps of a single SRR formed by interdigitated fingers thus bridging the fingers electrically as shown in Fig. 16. Optical signal can then be used for switching the SRR into a closed SRR (CSRR) that in effect ideally eliminates the magnetic resonance and thus the negative permeability of the metamaterial [302].

The ZnO NWs were grown using the sonochemistry method described earlier on a glass substrate with patterned photoresist mask for the split gap. After the growth period, the photoresist mask was lifted off in an acetone bath. After the liftoff process, only the split gap contained a continuous network of ZnO NW coating. In this case, the photosensitive area becomes a thin film of interconnected NWs. The randomly oriented single-crystal silicon NWs were grown on an amorphous seed layer of

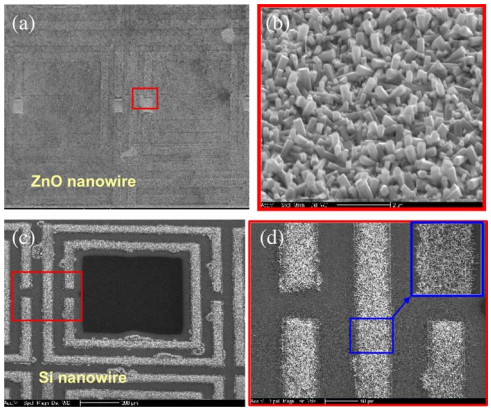

Fig. 17. NW integrated on metamaterial SRRs. (a) Ultrasonic growth of ZnO NW on rectangular split ring gaps of 3-nm Ti/100-nm Au on SiO_2 surface. (b) Close-up of ZnO NW. (c) Dense network of silicon NWs grown from templates of evaporated amorphous silicon on the SRR with (d) showing the close-up image.

evaporated silicon. The evaporated silicon growth template can be deposited on nonsingle-crystal substrates chosen from such materials as glass, metal, or ceramics. Fig. 17 shows the ZnO and Si NWs integrated on the SRR.

Although the high-speed response of either ZnO NW or SiNW presented in this section is not known at present, published literature [303]–[306] provides a promising path to achieve it. An optimized design and process recipe for direct growth of ZnO NW photoconductor using the sonochemistry process or CVD growth of Si NWs using evaporated amorphous Si as a seed template at high temperatures of 600 °C–800 °C can pave the way to an efficient photoconductive switch for a functional metamaterial modulator on arbitrary low-cost surfaces with improved cost benefit and comparable efficiency to bulk-crystalline-based devices.

IV. Device Design Challenges

The design and fabrication of high-performance NW PDs for communication, sensing, and imaging systems present several serious challenges. At the device level, there are still major hurdles that researchers are currently addressing, for instance: 1) the realization of reliable compound semiconductor NWs with desirable composition; 2) forming low-noise and low-resistivity contacts; 3) controlling polarization properties; 4) efficiently coupling and trapping light; 5) controlling surfaces, defects, and NW orientations for optimum mobility; and 6) impedance matching for high-speed operations. Obviously, the optimal design, fabrication, and integration process must be economically viable for CMOS applications. The stability of the resulting nanoheterostructures against high-temperature processes is also a very critical parameter that should be considered when successive processing steps involve high-temperature treatment. The challenges and limitations imposed by these parameters and their impact on the devices fabricated via various heterogeneous integration processes are discussed in the following sections.

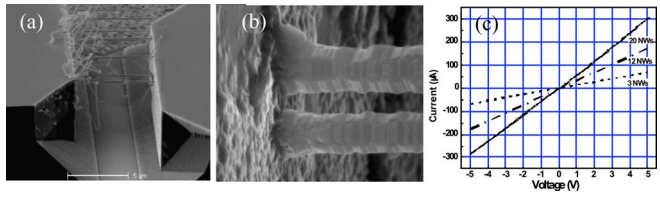

Fig. 18. (a) "Nanobridges" across electrically isolated electrodes. The Au-nucleated NWs grow mostly perpendicular to the (1 1 1) sidewalls from left to right in these SEM views. (b) SEM micrograph of an actual contact of the NW to the Si electrode. Contact quality has a significant bearing on the R_{contact}. (c) Highly linear *I–V* characteristics of the bridged Si NWs.

A. Low-Resistance and Low-Noise Contacts

A key barrier to wide-scale integration of functional NWs in devices and systems is the difficulty in forming reproducible and efficient contacts. Unlike the research-based approach of sequentially connecting electrodes to individual NWs for device physics studies, a massively parallel and manufacturable interfacing technique is crucial for reproducible fabrication of dense and low-cost nanodevice arrays. Ideally, an integration scheme should be universal and compatible with the existing IC processing techniques. It is also very important that the mass-manufacturing technique allows precise control on the NW length, density per unit area, contact resistance, and mechanical properties of the fabricated NWs.

We developed a novel epitaxial interfacing technique for integrating semiconductor NWs in devices that resulted in highly reproducible and ohmic contacts and contributed to exceptionally low noise. Two electrically isolated and opposing vertical Si surfaces were fabricated using optical lithography along with wet and dry etching and grew lateral NWs from one surface and epitaxially connected them to the other, forming mechanically robust and electrically continuous "nanobridges." Both group IV and III–V NWs were bridged between Si electrodes [64], [92]. Based on our *I–V* measurements and a constructed model, we calculated the specific contact resistance to be in the range of $4 \times 10^{-6}\ \Omega{\cdot}\mathrm{cm}^2$ for bridged Si NWs. This value is more than two orders of magnitudes lower than that of other approaches of evaporating metals on semiconductor NWs for contact formation. We also showed that the contact resistance depends on the effective conducting cross-sectional area, and hence, is influenced by the presence of a surface depletion layer [27]. Individual electrical access to nanodevices without recourse to nanoprobes or tedious and expensive serial interfacing procedures has thus been achieved. He *et al*. [307], and Englander *et al*. [308] also reported similar techniques for interfacing Si NWs. Our bridged NWs have demonstrated highly linear contact characteristics along with potential benefits of their good mechanical robustness, precise control on the lengths, and ease of integration in the Si-processing technology. This interfacing technique emerges as a promising candidate to realize massively parallel and mass-manufacturable synthetic "bottom-up" technique for high-density integration of NW-based devices and circuits beyond the capability of conventional technologies with a small fraction of the present-day fabrication cost. Fig. 18 shows the NW bridging technique.

An empirical model was developed to estimate the impact of contact resistance for bridged NW structures based on the *I–V* data from our Si nanobridges. We found that the contact resistance depends on the effective conducting cross-sectional area of the NW, i.e., it is influenced by the presence of a surface charge-induced depletion layer on the NW surface. It was also evident that the contact resistance becomes significant as the wire diameter is scaled. Commonly adopted techniques of contacting the NWs placed on insulating substrate with evaporated metals often lead to Schottky barriers at the interface, which are hard to overcome. Bridged Si NWs have demonstrated highly linear Ohmic contact characteristics along with potential benefits of their good mechanical robustness, and ease of integration with Si technology. These unique attributes of the epitaxially interfaced nanobridges position them as attractive choice for realization of mass-manufacturable nanoscale devices such as NW PDs.

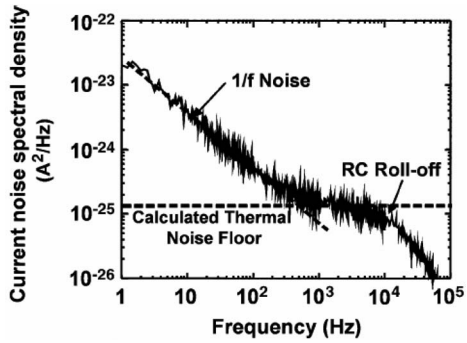

Fig. 19. Typical plot of bridged SiNW current noise spectral density [309]. The excess noise (1/*f*) observed at low frequencies can be interpreted in terms of bulk- and contact-noise contributions, with the former comparable, in terms of Hooge parameter values, to the low noise levels observed in high-quality silicon devices. Lowering the contact resistance will further improve the noise performance.

B. Contact Resistance and Noise in PDs

Noise is the random fluctuating component of a voltage or current in a device, which can be caused by different mechanisms, for example, carrier mobility fluctuation and carrier trapping–detrapping. The noise property of modern nanoscale devices is even more important because they typically operate at a lower voltage, so the SNR becomes critical. We earlier reported the characterization work on the 1/*f* noise of welded NWs and compared them with that of CNTs and NW-based devices fabricated using the existing research-based interfacing method (metal evaporation on NWs) [92]. Although it was widely speculated that the CNTs would be relatively less "noisy" owing to their stable carbon–carbon bonds, our results show that, on the contrary, they are very noisy. Similarly, the noise level of conventional NW devices fabricated by evaporating metal for contacts was also found to be very high. The noise level in our self-welded Si NWs was found to be at least two orders of magnitude better than that of CNTs and NW devices [309]. The superior characteristics were the result of the highly epitaxial bonding or welding between two NWs and NW-electrodes. These results substantiate our endeavor for employing the bridging/welding techniques for designing NW-based electronic and photonic devices.

In a PD, the ultimate limit to the detectability of weak signals is set by the noise that obscures the desired signal in a communication link. The noise measurement can yield a lot of information about the manufacturing process and the inner workings of a device. For example, the 1/*f* noise in a MOSFET is related to the impurity-related trap density at the oxide interface and can be used to identify problems in the manufacturing process. Also, noise measurement can be used as a figure of merit; the applicability of a certain technology can be limited by the noise the devices produce (see Fig. 19) [309]. This observation also shows the importance of a good understanding of noise characteristics of semiconductor NWs. Any interfacing technique needs to address this crucial issue before it can be applied in a wide range of applications. In addition, an in-depth understanding of the doping distribution is crucial for accurate prediction of the device parameters, such as breakdown voltage of a junction device. The specific pattern of doping in NW can be directly correlated to the noise characteristics of NW-based devices.

C. Photon-Trapping for Enhancement of Photo Absorption

Traditional PDs are fabricated from 2-D, epitaxial, thin-film structures and in order to increase the likelihood of photon absorption, their top surfaces are generally coated with a single or multilayer antireflection (AR) film. In some cases, relief structures with average periods less than the incident wavelength are fabricated on the top surfaces and serve as an AR coating. New device architectures inspired by nature (e.g., moth eyes) and based on micro-/nanopillars can reduce reflection and enhance sensitivity. With an appropriate fill ratio, a broad range of wavelengths and incident angles can be accommodated to efficiently trap photons for enhanced absorption [219]. With a fill ratio (total pillar area/total detector area) lower than 1, dark current of a PD can be significantly suppressed due to the total semiconductor volume reduction (dark current is proportional to the material volume). This would increase the SNR of the detectors, and particularly for infrared detectors, may offer an interesting advantage of increasing the temperature of operation, if challenges such as surface leakage and traps associated with the pillar design can be properly addressed.

Unlike the flat surfaces that are illuminated in a conventional PD, NW-based devices offer the potential for trapping the incident photons by multiple reflections and scattering in the dense network of NWs until the photons are completely absorbed. Zhang *et al.* showed that the fraction of incident photon energy overlapping with the NW volume could be significantly higher than the fill ratio due to high confinement of energy in the high refractive index medium of NWs [171].

We conducted experiments to verify the contribution of a NW-coated surface in suppressing reflection of wide spectrum of photons using a reference GaAs substrate and a second GaAs substrate with InP NW coating on it. The optical spectral reflectance of the NW-coated GaAs and a reference polished GaAs

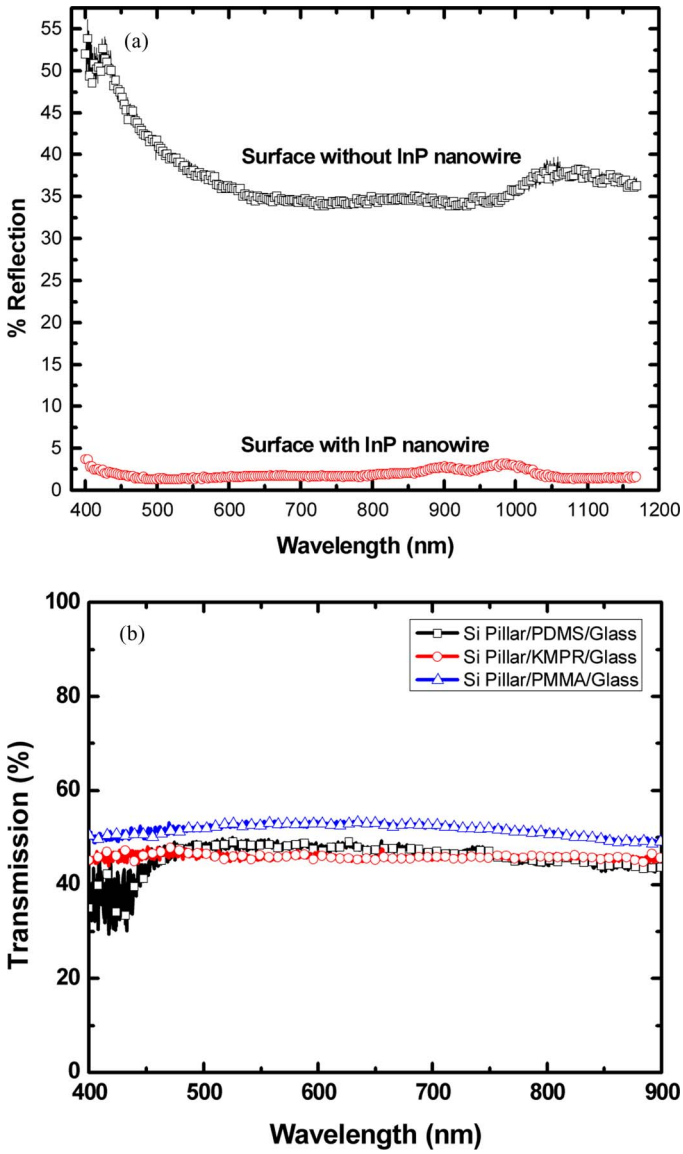

Fig. 20. (a) Optical reflectance of a bare surface and InP-NW-coated surface. A NW-coated (1 0 0)-oriented GaAs surface shows greatly reduced reflectance over the spectrum ranging from 400 to 1150 nm. (b) Optical transmission data at normal incidence for the transferred devices in the shape of micropillars onto the respective polymer-coated carrier substrates. The transmission curve of each sample is normalized to its individual reference without the device (micropillars). The devices on each sample absorb a fraction of incident photons, reducing the total transmission [135].

substrate is presented in Fig. 20(a). On (1 0 0)-GaAs, InP NWs grew along two equivalent (1 1 1) directions of the substrate and showed a dramatically reduced reflectance over the spectral range from 400 to 1150 nm, even without using any AR coating. In the device that was designed with InP NWs on n-Si:H electrodes, as was described in Section III-B, InP NWs grew with a high degree of randomness in their orientations and can offer an intrinsic capability for significantly reduced reflection loss. We also fabricated highly oriented micropillar-based structure with a pillar size of $\sim$10 μm and diameter of $\sim$1 μm and subsequently transferred to a thin polymer film. Optical absorption and transmission measurements show enhanced absorption and reduced reflection as illustrated in Fig. 20(b) [135].

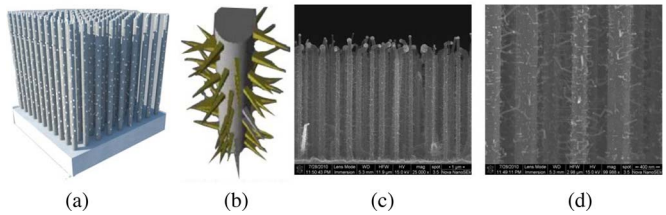

Fig. 21. (a) Al_2O_3 nanoparticles used for enhancing light absorption via photon scattering [310]. (b) Schematics of secondary Si-whiskered NWs grown on silicon NWs for photon trapping and scattering. (c) and (d) SEM images of the secondary Si nanowhiskers on NWs.

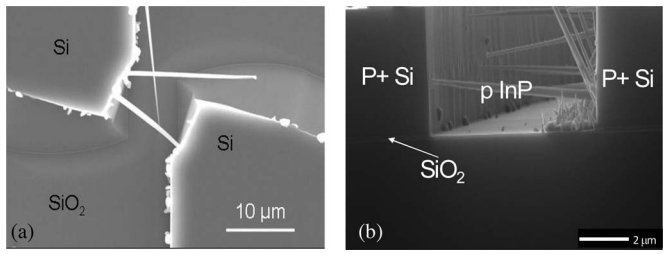

Fig. 22. SEM image of p-type InP NWs grown between degenerately doped Si electrodes (p^+ Si). NWs grew faster in the direction orthogonal to the (1 1 1) side walls and quickly made bridges to the opposite wall. Some NWs grew in the equivalent directions and could not make a bridge. (a) Top view. (b) Tilted side-view.

Although some randomization in the orientation and dielectric coating of the pillar walls may help increase the optical absorption, some scatterers are needed to eliminate the angular sensitivity and enhance the absorption at normal incidence. Kelzenberg *et al.* recently reported the use of Al_2O_3 particles to scatter the light to enhance photon–pillar interactions even when the fill ratio is very low [310]. The wide bandgap of the Al_2O_3 particles suppresses absorption in the particles and increases photon absorption in the semiconductor NWs. These wide-bandgap scattering particles can be replaced with direct growth of nanoscale whiskers along the length of the NWs.

Most NWs are synthesized using catalysts, and nanoparticles of metal–semiconductor eutectic alloy are formed on the NW surfaces under specific growth conditions. These eutectic alloys on the surface of NWs can be used as catalysts to enable one-step growth of branched NWs, as shown in Fig. 21. Based on the same principle demonstrated by Kelzenberg *et al.* [310], the branches can be used for enhanced light scattering in NW PDs. With a dimension below the quantum confinement regime, the scattering branches can also be prevented from photo absorption. Our experimental results on enhanced detection based on whiskered NWs will be reported elsewhere.

D. Surface Traps, Passivation, and Persistent Photoconductivity

In applications, such as PDs, laser diodes, and modulators for high-speed optical data communication, the device must be highly responsive to photoexcitation and quickly relax to the dark state immediately after the light source is shut off. We investigated InP NWs bridged between single crystal silicon electrodes under UV and visible laser illuminations and found that

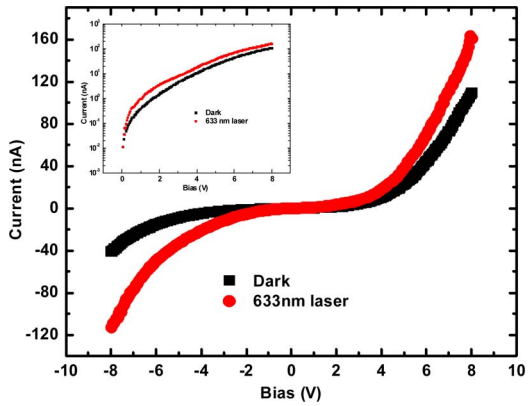

Fig. 23. *I–V* characteristics of InP NWs bridged between single crystal Si electrodes under dark ambient and 633-nm He–Ne laser excitation. Inset is the log-linear plot. From the *I–V* characteristics, it is evident that the devices are highly photoresponsive.

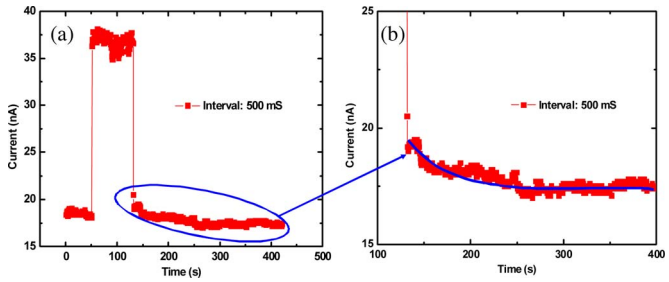

Fig. 24. (a) Persistent photocurrent (PPC) experimental data of InP NWs bridged between single-crystal Si electrodes with 633-nm laser at room temperature under 5-V bias. Laser illumination was held for 90 s. Data points were collected at an interval of 500-ms set in the Keithley 237 data acquisition system. (b) Zoomed-in view of the excess photocurrent decay region. Exponential decay profile is evident. Using exponential fit of the excess photocurrent data, a decay constant of $\sim 9.8 \times 10^{-2}$/s is extracted. Observed relaxation time is about $\sim$50 s.

photogenerated excess carriers do not recombine immediately after the light source is turned off, rather the excess photocurrent decays slowly and it takes tens of seconds to reach the dark current level. The effect, called persistent photoconductivity (PPC), is observed when charge carriers in a material are photoexcited above the ground energy and maintain the excited nonequilibrium state for a long time due to their delayed relaxation to the ground state [311]–[315]. PPC originates from the long recombination time due to carrier trapping. Both bulk defects, such as vacancies, impurities, and surface states can collectively contribute to the long trapping of photogenerated excess carriers and manifest as a temporary boost in dark conductivity, which may exist for days or even years [316]. PPC studies have been reported for some structures, e.g., GaN thin films [311], [313], [314], [317]–[320], InGaN epitaxial films [315], GaN-NWs [321], and InP NWs [322].

In order to understand the PPC in InP NWs, we patterned (1 1 1)-oriented vertical Si electrodes on a (1 1 0)-oriented SOI wafer using conventional photolithography and wet etching and then grew p-doped bridging InP NWs between the electrodes. Fig. 22 shows a SEM image of an InP nanobridge fabricated between the (1 1 1)-oriented Si electrodes. The preferential growth direction is $<1\,1\,1>$ because of the high density of silicon atoms on the (1 1 1) plane.

As optical sources, a 325-nm He–Cd UV and a 633-nm He–Ne lasers were selected to provide optical excitations above InP bandgap energy of $\sim$920 nm (1.34 eV). Output power of the ultraviolet and visible laser sources were 1 and 2 mW with a beam diameter of $\sim$10 and $\sim$5 μm, respectively. All the measurements were performed with dc bias at room temperature in a standard probe station with a photoluminescence setup. Data acquisition was performed using an Agilent 4156C- precision semiconductor parameter analyzer and Keithley SMU 237 with associated software controlled computer system. The laser ON–OFF time was controlled by a Uniblitz (Model: T132) shutter–driver timer for precision timing.

The Si electrode regions were degenerately p-doped with a doping density of $\sim 10^{20}$ cm^{-3}. The high doping renders the electrodes essentially metallic and ensures that no significant optical excitation can supersede the doping-oriented conductivity of these electrodes. Consequently, all the photocurrent in the devices is the contribution of the photoexcited carriers in the InP NWs. Photoresponse of the devices was tested and the results are shown in Fig. 23. With 633-nm laser excitation, a discernible increase in the current is observed and confirms that the NWs are highly responsive to the monochromatic laser light.

The room-temperature PPC experimental results with 633-nm laser at 5 V bias are shown in Fig. 24. Decay constants from experimental data were estimated to be $\sim 9.8 \times 10^{-2}$ s^{-1} and a relaxation time of $\sim$50 s was noted. Relaxation time is the time required by the charge carriers to return to the original states from where they had been photoexcited. The PPC experimental results with 325-nm UV laser are presented in Fig. 25 for a bias of 5 V. The extracted decay constant is $\sim 2.8 \times 10^{-3}$ s^{-1} with a relaxation time of $\sim$110 s. A smaller decay constant means a longer time is required for the excess photocurrent to decay to the dark current level. A comparison of relaxation times with 633- and 325-nm lasers reveals that photoexcited carriers with 325-nm laser required almost twice as long as the time taken with 633-nm laser to decay to the dark current level. The longer relaxation time associated with 325-nm laser excitation is due to the higher energy of the photons from UV laser compared to the energy of the photons from the visible laser. High-energy UV photons excite charge carriers to higher energy states and their subsequent relaxation takes longer time compared to the case with visible photons.

In either case, the slow carrier recombination can be attributed to the carrier trapping in defects in NW bulk and in the interface between the NWs and Si electrodes. When carriers are trapped, the surface potential changes and the escape of the trapped carriers are delayed. The defects inside the InP NWs in our devices may be similar to those reported by Chen *et al*. for GaN thin film [313]. The high lattice mismatch ($\sim$8.1%) between InP and Si causes dislocation defects at the InP/Si heterointerface [52]. The dislocation defects can act as traps and contribute to the PPC effect in our devices in a way similar to that reported by Beadie *et al*. [311].

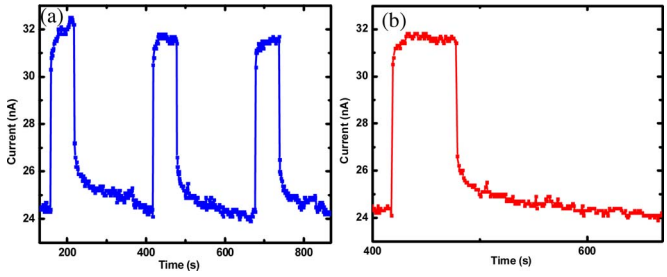

Fig. 25. (a) PPC experimental data of InP NWs bridged between single-crystal Si electrodes with 325-nm UV laser at room temperature under 5-V bias. Laser ON-time was 60 s followed by an OFF-time of 200 s. (b) Zoomed-in view of the middle cycle. Exponential fitting of the excess photocurrent decay profile gives a decay constant of $\sim 2.8 \times 10^{-3}$/s. Observed relaxation time is about $\sim$110 s.

The aforementioned results offer some insight and new understanding into the trap physics of NWs and nanoheteroepitaxial junctions, which is critical for applications of these materials in photonic devices, such as PDs. The impact of PPC has been found to increase the photoconducting gain and response of PDs by orders of magnitude [259], although it can cause detrimental effect to the dynamic response (bandwidth) of the devices.

E. High-Speed Design Challenges and Impedance Matching

At nanoscale, the resistance and parasitic elements of a NW are substantial. For example, kinetic inductance per unit length of a typical CNT is 16 nH/μm and copper sheet resistance of 150-nm line pitch is $\sim$150–200 Ω/sq. The *RC* delays of 90-nm metal interconnect with a line pitch of 300-nm exponentially increases beyond 100 ps/mm^2. Although the length of NWs in practical detectors will be a few micrometers to deep submicrometers in length, the parasitics and *RC* delay can cause degradation to signal integrity in the gigahertz frequency regime. In the past decade, theorists have attempted to model the high-frequency properties of NWs and nanotubes [323]–[328]. Burke employed Luttinger liquid theory to extract distributed transmission-line models for CNTs in the gigahertz regime [324]. Miyamoto *et al*. used a classical treatment of Maxwell's equations to evaluate the resistance and self-inductance of a conducting CNT [326]. However, the reported theoretical and numerical modeling has not been verified with extensive experimental results. Further, these results have been based on ideal NW structures and are not specific to technologies suitable for nanoscale semiconductor p-n or p-i-n junctions.

Whenever a high-frequency signal is coupled in and out of a nanodevice, there is a natural impedance mismatch because any technology with nanometer feature sizes is much less than the wavelength under consideration [329]. This implies that high-speed characterization, which is typically based on reflection, transmission, or scattering measurements, gives rise to very small signals making it very challenging to measure the nanodevice at high speed. One approach to solve this challenge is to develop excellent calibration techniques that fully characterize all of the parasitics before measuring the actual device. Lack of systematic high-frequency characterization tools for measuring the resistance and other parasitic elements of NW-based devices is a major hurdle that needs to be addressed. An acceptable design rule for *macro-to-micro-to-nano*-scale devices and developing an equivalent-circuit model for impedance prematching are crucial for measuring the temporal response of NW-based PD under ultrafast optical excitations. In addition to helping with the characterization of PDs, these measurements will lead to a fundamental understanding of high-frequency electrical transport in NWs and nanoscale junctions with dimensions $\sim$10 nm.

Highstrete *et al.* conducted RF measurement of NWs and nanotubes from 0.5 to 50 GHz between 4 and 293 K temperature ranges and measured the interface-state-dominated conductance that increased with increasing frequencies [330], [331]. These measurements are challenging in large part because of the difficulty in calibrating and measuring systems with impedance much larger than 50 Ω. The typical resistances of NWs are in the range of several kilo-ohms making them mismatched in impedance with measurement systems that are typically 50 Ω in characteristic impedance. Though these high-resistance values may seem to restrict the operational speed of nanoelectronics, the capacitance for these devices is also generally small, as is the typical length. This gives rise to very small *RC* times, and very short transit times, of order picoseconds or less. Consequently, the speed limit could be very large, up to the terahertz range.

As described in Section III-B, during the growth of InP NWs, the deposited metal electrodes of 3-nm Ti/100-nm Pt subjected to temperatures $\sim$430 °C and together with the uncatalyzed thin layer of InP being deposited changes the sheet resistance of the CPW metal lines in some devices. From Fig. 26(a), the best measured pulse response gave a FWHM of 16 ps, but as shown in Fig. 26(c)–(e), the impedance mismatch and the changes in the *RC* time constant as the probes are moved further away from the NW region clearly deteriorates the pulse response. This was observed when a device with a gap of 0.7 μm was probed at three different locations, as shown in Fig. 26(b). If the GSG probes are positioned very close (down to nanoscale) to the active NW photoconductors, the pulse looks very symmetric with strong voltage amplitude of 3.6 mV. As the probe is moved away from the active region of the device along the CPW transmission line, the electrical pulse generated by the photoconductor gradually loses amplitude and a long tail (fall time) starts to dominate the pulse profile. The pulse magnitude was found to be 2.1 mV at a distance of $\sim$200 μm and 1.6 mV at a distance of $\sim$400 μm. The measurement shows that the high-speed nanocomponents of the electrical pulse cannot successfully make impedance-matched transition from the active device to the passive CPW due to high-impedance mismatch between them. In fact, considerable reflection dominates the pulse profile, even when probed close to the PD, when a symmetric pulse shape is observed with a measured pulsewidth of 16 ps.

It was pointed out that the coupling of nanodevices to the macro or micro world is usually slow or narrowband, though the coupling between nanoelectronic devices can be extremely fast. For coupling close to our active photoconducting device when the distance between the probe and the devices is down to nanoscale, the capacitive loading from the device to the probe

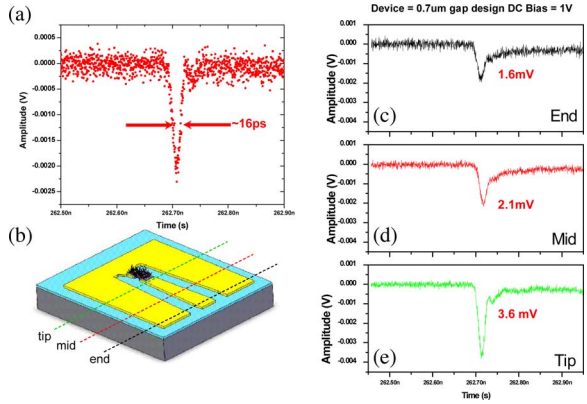

Fig. 26 (a) High-speed pulse response ($\tau_{\rm meas} \sim 16$ ps, $\tau_{\rm actual} \sim 11.4$ ps) of the InP NW photoconductor (0.7 μm gap) triggered by ultrashort 780-nm laser pulses of width 1 ps. (b) Probing locations on the device. Pulse responses measured at the (c) tip, (d) middle, and (e) end. The device was biased at 1 V.

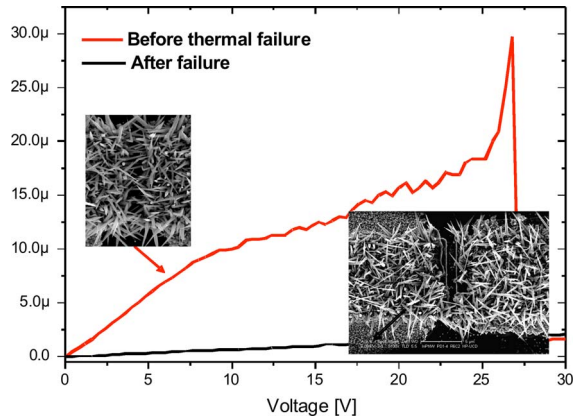

Fig. 27. *I–V* characteristics of InP NWs before and after thermal breakdown due to joule heating from the photocurrent when illuminated with the pulsed laser.

is minimized and signal coupling is very efficient. As the probe is moved away from the active device, the effect of narrowband coupling compounded with larger capacitive loading severely impacts the signal amplitude. We also attribute this observation to macroscopic disorder from statistical variations of electronic properties within the ensemble of photoconducting NWs, such as individual NW resistivity and coupling capacitance, and dislocation.

F. High Current Capacity and Reliability of NWs

The operational reliability of NW-based PDs from Joule self-heating and high photocurrent is an important performance parameter for high power NW PDs. Typically the high current density in conventional metals can create voids by electromigration and most fail due to Joule heating at $\sim 10^3$ to 10^4 A/cm^2. There have been efforts to characterize the maximum current density of some individual NWs, for example, PtSi NW [332], Si NW [333], [334], NiSi NW [335], and GaN NW [336], [337]. In exploring the application limits of the InP NW photoconductive switch (see Section III-B), the maximum photoresponse current and thermal breakdown of the device with dc bias under a 780-nm pulsed-laser illumination were studied. The 20-MHz repetition rate of the pulsed laser, for the purposes of the dc *I–V* measurements, appears as uniform illumination. As shown in the *I–V* measurement of Fig. 27, before the thermal failure, from 0 to 8 V, the resistance was constant at $\sim$0.8 MΩ, and subsequently, each individual welded connection that yields an electrical continuity and that is part of the overall parallel network of bridged NWs begins to melt off sequentially as evident from the "sawtooth" like *I–V* behavior. Catastrophic material breakdown was observed at $\sim$27 V ($\sim$13.5 V/μm) with a drastic fall in current magnitude from 30 μA to $\sim$500 nA at the point of breakdown, where the last few bridged NWs still formed a complete resistive circuit. The second linear region after $\sim$27 V corresponds to a resistance of $\sim$15 MΩ. When the laser illumination was turned OFF, the eventual resistance was $\sim$245 MΩ.

The breakdown mechanism was influenced by the laser illumination and it occurred at a considerably low voltage. The pulsed-laser excitation enhanced the I^2R (Ohmic) Joule heating, and a very fast carrier multiplication created an intense local heating, and eventually enhanced the breakdown mechanism. The presence of photocurrent during the *I–V* measurement led to a larger Joule heating, $\sim (I_{\rm dc} + I_{\rm ph})^2 R_{\rm tot}$, that localized the power dissipation within the NW–intersection areas and increased the temperature significantly. This temperature gradient enhanced the electromigration and diffusion of materials (Indium) to the extent that the resistance and current density increased (due to the constriction in the cross-sectional area) causing the Joule heating to increase as well. The mechanism becomes self-perpetuating, and rapidly leads to the thermally induced failure of the photoconductors.

A general expression may be written for the Joule heating as follows:

$$P_{\rm elec} t = (I_{\rm dc} + I_{\rm ph})^2 \, R_{\rm tot} t \tag{2}$$

where $P_{\rm elec}$ is the electrical power, $I_{\rm dc}$ is the direct current, $I_{\rm ph}$ is the photocurrent, $R_{\rm tot}$ is the total resistance of the NW, and t is the duration of the applied current. From [144], since there are two distinct InP crystal lattices (pyramidal and hexagonal), the resistance for a single-bridged InP NW can be approximately expressed as follows:

$$R_{\rm nw} = \int_0^L \frac{\rho\,(T)}{A\,(x,y)} dx \text{ and } \frac{1}{\rho} = q\mu\,(T)\,n\,(T) \tag{3}$$

where ρ is the resistivity that depends on the mobility (μ) and carrier density (n) (both functions of temperature T), L is the equivalent NW length, and $A(x, y)$ is the nonuniform cross-sectional area. The total resistance for the intersected NWs, neglecting the contact resistance can be obtained from (3). Thermal breakdown occurs when the electrical power ($P_{\rm elect}$) exceeds the InP NW melting energy expressed by the following equation [338]:

$$P_{\rm crit} t = C_p m_{\rm crit} \Delta T + H_f m_{\rm crit} \tag{4}$$

where $P_{\rm crit} t$ is the critical energy to melt the NW, C_p is the specific heat capacity, $m_{\rm crit}$ is the critical mass of the NW regions to be melted, ΔT is the change in temperature from room

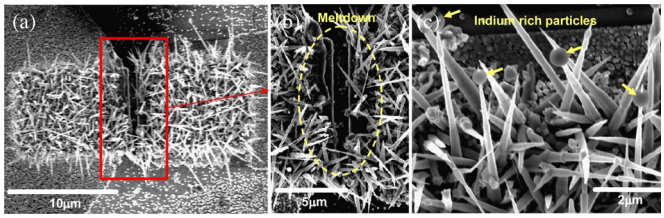

Fig. 28. (a) SEM image of InP NWs that has undergone thermal breakdown due to catastrophic Joule heating. (b) Marked areas clearly show the melted material. (c) Heat was sufficient enough to decompose InP forming indium-rich spherical particles. Each bridged NW in the network acts as an electrical fuse.

temperature to the melting temperature, and H_f is the InP latent heat of fusion. Since most of these parameters are not known, only a qualitative analysis can be undertaken [333].

SEM images (see Fig. 28) show molten materials formed on the electrode edges and a high density of nanoscale spherical particles observed on the surfaces and in the upper parts of the freestanding NWs within the active area. During the SEM imaging, the structures were found to be mechanically unstable indicating a possibility of indium fusion during the breakdown process and formation of indium-rich spherical particles.

G. Controlling Orientations for Optimum Mobility

Some orientations of NWs offer higher mobilities than others. For example, among the various oriented NWs, electron and hole mobility for Si <1 1 0> NWs are calculated to be larger by nearly two orders of magnitude than those of SiNWs with other orientations having similar diameter. Thus, any NW PD with such orientation will offer an improved bandwidth. However, it is not always easy to synthesize NWs with preferred orientation. We recently observed that the orientation of NWs can be changed from <1 1 1> direction to <1 1 0> direction on a Si (1 1 0) substrate by increasing the growth temperature above ~610 °C and by changing Au–Si eutectic phases. Fig. 29 depicts the orientation dependence of NWs on physical growth parameters. Details of this study have recently been reported by Kwon *et al*. [31].

H. Catalyst for NW Synthesis—Issues of Device Contamination and Impact on Performance

Using a metal catalyst for nanowire growth has been demonstrated to be an excellent method for 1-D-oriented NW structures in most material systems [339]–[342]. An important aspect to the formation of these 1-D NWs relates to their crystallization: the evolution of a solid from a vapor, a liquid, or a solid phase undergoing nucleation and growth. As the concentration of the building blocks (atoms, ions, or molecules) of a solid becomes adequately high, they combine into small nuclei or clusters through homogeneous nucleation [137], [343]. These clusters serve as seeds for further growth to form larger clusters. A metal catalyst acts as a high-energy site for decomposition of a NW material containing precursor gas, which deposits the NW material onto the catalyst surface [59], [344]. Adsorption (or surface transport) of the NW growth material into (or around)

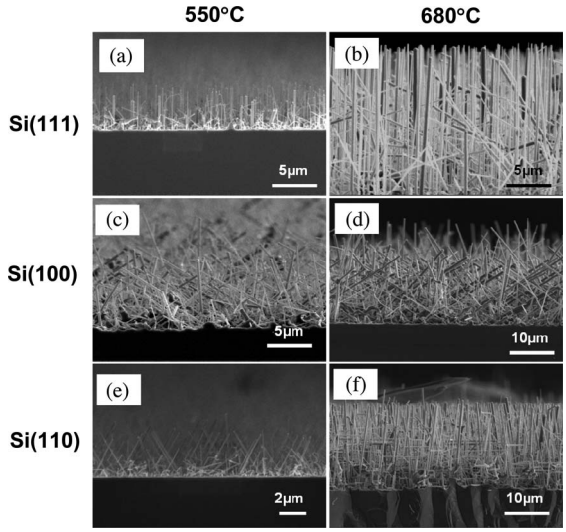

Fig. 29. Cross-sectional scanning microscope image of Si NWs grown on Si (1 1 1) with growth temperature of (a) 550 °C and (b) 680 °C. Si NWs grown on Si (1 0 0) with growth temperature of (c) 550 °C and (d) 680 °C. Si NWs grown on Si (1 1 0) with growth temperature of (e) 550 °C and and (f) 680 °C.

the catalyst, and deposition onto the substrate at the catalyst–substrate interface is called the VLS method [59], [339], [344].

The VLS method has allowed the development of a wide variety of NW materials; group IV (Si [340], [345], Ge [340], [346], [347]), II–VI (ZnO, CdS) [348], [349], III–V (GaN, GaAs, InP) [348], [350]–[353], and alloy compound semiconductors [354], [355]. Particularly for Si NW growth, various kinds of metal catalysts, such as Au [59], [131], [335], [339], [356]–[358], Ag [57], [339], [359], [360], Al [360]–[362], Cu [339], [358], [363], [364], Fe [365]–[367], Ga [58], [360], [361], In [360], [368], [369], Ni [59], [339], [359], [360], [370], Pd [59], [339], [358], [360], [371], Pt [59], [214], [339], [358]–[360], [372], Ti [373], [374], and Zn [131], [360], have been studied.

The selection of a proper metal catalyst must be carefully considered due to restrictions, which limit the NW synthesis process to within a specific temperature range. The standard catalyst used—Au, allows a wide span of synthesis temperature above 363 °C depending on silicon-source gases. Al is one of the promising catalysts for its low processing temperature and superior NW quality as long as oxidation of Al is suppressed during synthesis [362]. Cu and Ti are also good candidates, but require high growth temperatures and do not fully satisfy the conventional CMOS fabrication technologies. Various combinations of metal catalysts could lead to further possibilities in NW synthesis, despite few studies on metal alloy catalyst being reported [367], [375]. Fig. 30 shows the impact of various metal catalysts on the growth temperature and energy band of silicon NWs.

Catalyst-free synthesis has also been studied in order to prevent catalyst contamination in NWs. It is developed mainly to construct compound semiconductor nanomaterials using CVD [376], vapor-phase epitaxy [377], [378], laser ablation [379], and molecular beam epitaxy [380]–[382]. Although contamination in nanomaterials is eliminated, it has been reported that growing elementary semiconductor NWs, such as Si and Ge NWs, is relatively more challenging because these techniques

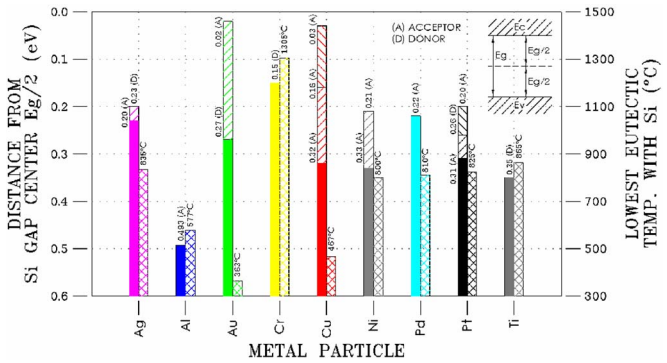

Fig. 30. Impact of various metal catalysts on the growth temperature and energy band of silicon NWs. The left bars show possible ionization energy levels that can be introduced when a metal is alloyed with silicon. The right bars show the lowest recorded liquid eutectic temperature when mixed with silicon.

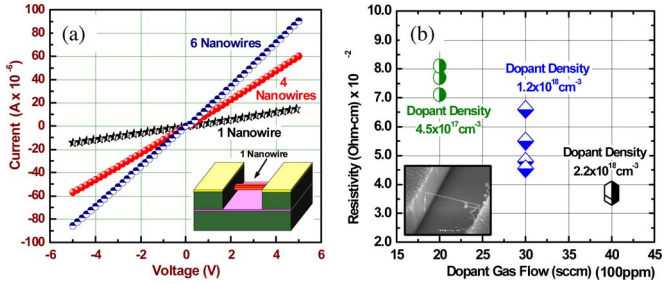

Fig. 31 (a) Measured linear *I–V* characteristics between bridged electrodes spaced 10 μm apart with varying numbers of NWs ($d \sim 100$ nm). (b) Resistivity versus the B_2H_6 gas flow showing a good correlation between dopant density and measured resistivity.

make use of an oxide as a seed layer, which results in poor orientation and distribution of NWs in comparison to catalyst-assisted methods [383], [384].

Depending on the catalyst, various impurities may be introduced into the NW. For instance, Yu *et al*. found that Si NWs are doped with Au atoms by thermal diffusion during their synthesis [131]. Au catalyst would be coated by 1–1.5 gold monolayers on the wire surface [357], which are located at the interface of Si NWs and native oxide on the surface of the NW [385]. Even though it is shown that the thermal diffusion of metal catalysts on the NW surface can be prevented by controlling physical parameters, such as growth temperature, partial pressure of source gases, and catalyst size [386], it is a challenge to block metal catalyst atoms from diffusing into NWs during the NW synthesis. This is due to the solubility of a metal in a NW, which is significantly higher than that in a bulk material [387], [389] and it would be almost impossible to stop the thermal diffusion of impurities.

The fundamental motivation for reducing metal contamination in semiconductors is that it causes degradation to the devices and impacts the reliability [388]. A critical degradation of the gate dielectric layer could happen due to the large diffusivity of Au at the interface of oxide and semiconductor in MOS devices [390]. The metal impurities generate deep-level traps located around intrinsic energy level in the bandgap. Deep-level traps enhance recombination of generated carriers such that p-n-junction leakage current increases [391], [392]. They also limit the minority carrier lifetime and the diffusion length [392]. Deep-level traps, however, are advantageous to improve photoconductivity of NWs. Electrical properties of NWs, due to the high surface-to-volume ratio and small radius size, are very sensitive to surface-state configurations [10], [393]. Moreover, a large density of surface trap states significantly increases the photoconductivity gain of NWs by extending the photocarrier lifetime and enhancing charge separation [259], [394], [395]. As a result, metal catalyst contamination may not completely impede the development of NW PD devices. Further studies on the effects of metal catalyst contamination on the magnitude of photoconductive gain and device reliability are still required to fabricate more efficient NW PDs.

I. Challenges in the Doping of NWs

Both p-type as well as n-type doping of NWs has been demonstrated qualitatively for Si [10], GaAs [396], InP [62], and GaN [397] NWs. CVD is used frequently for catalyst-based synthesis of semiconductor NWs. Two main methods are used to dope NWs—the vapor–solid (VS) mechanism and the VLS mechanism. The VS mechanism allows for the dopant atoms to be directly deposited onto the NW surface, while in the VLS method, the dopant atoms dissolved in the catalyst are then incorporated into the liquid–solid interface, which is formed during the growth of the NWs. These two methods have different rates of diffusion [215]. Flow rate of doping gases contribute to different doping concentrations (as shown in the Fig. 31) and it remains dependent on other physical parameters of the CVD chamber.

To create a high-mobility carrier gas in NWs, radial band structure engineering has been used in undoped NWs [398], [399]. This method, however, cannot be controlled efficiently and is only feasible for materials, which can be engineered with suitable band energies. To overcome this problem of not being able to acquire qualitative control of doping levels in NWs, remote p-doping of InAs NWs has been achieved by a p-doped InP shell grown epitaxially on the core NW [400]. Controlled doping of Si NWs has been achieved by using a laser catalytic growth method to controllably introduce either boron or phosphorus dopants into silicon NWs [401].

With the VLS growth, it is difficult to determine how impurity atoms interact with the metal particle and how the dopant atoms are incorporated into the NWs. It was observed that the introduction of a doping agent at any stage of the NW growth contributes to the entire NW being doped. This severely limits the longitudinal doping modulation and the realization of longitudinal NW structures with alternating doping characteristics [402]. The doping mechanism also contributes to the variation in the NW growth rate and structural profile.

V. Conclusion and Perspective

The ability to design PDs using high-quality semiconductor and oxide NWs based on bottom-up or self-assembly processes, and integrating them onto various substrates can lead to cost-effective, superior, and novel functionalities. In this review, we

presented a brief description of the different approaches to realize an integrated NW device. We show that both synthesis in-place (direct growth) and transfer printing on an arbitrary substrate offer high flexibility in the design and fabrication of NW-based PDs, which can be used in a wide range of technologies. However, for the NW integration process to be economically viable and attractive for CMOS applications, it must offer the possibility of direct growth and integration of non-Si-based NW devices onto large Si wafers.

Currently, issues such as: 1) lattice constant, material, and thermal mismatch; 2) lack of good control over atomic structures; 3) assembly into functional devices; 4) difficulty in forming ternary and quaternary NW alloys; 5) surface states; 6) persistent photocurrent ; 7) contact resistance and noise; 8) controlled doping for sharp homo- and heterojunctions; 9) nano-to-micro impedance matching; and 10) catalysts-induced contamination, make it difficult to grow and design NW devices on Si or any other substrates.

A successful NW detection and sensing device would require a meticulous control of surface states, defects, traps, orientation, polarization and light coupling, as well as good control on generating sharp axial or radial junctions in the NWs. There are obvious challenges in eventually realizing high-performance NW PDs. Most conventional semiconductor PDs operate at essentially 100% quantum efficiency, whereas NW PDs' efficiencies are much lower in values. Development of feasible techniques is now crucial to match the efficiency of NW PDs to that of their classical counterpart, and a combination of plasmonic techniques and NW heteroepitaxy may offer the potential to realize substrate-independent NW PDs with high efficiency and bandwidth.

The basic devices and laboratory demonstrations of the key elements of technology exist for NW PDs, and minimum physical breakthrough is required to implement the device in most systems. However, substantial technological work remains:

1) Controlling the physical properties, such as diameter, doping uniformity, orientations, identical surface, and contacts, is required to meet the strict requirements for practical systems with future generations of silicon photonics and CMOS.
2) Designing for impedance-matching techniques between NW PDs and conventional high-speed circuits.
3) The technology for integrating III–V and II–VI NWs with silicon ICs is still at an early stage, though there have been considerable key demonstrations in the past few years. It is likely that the first introductions of NW PDs will use hybrid approaches, such as transfer-printing or pick-and-place. Such hybrid approaches require no modifications to the current process for fabricating silicon ICs except to add processes for fabricated NW PDs. Long-term approaches will probably focus on monolithic integration via nanoheteroepitaxy, currently at the infancy as a research activity.
4) Novel methods will be required to ensure growth in-place under acceptable physical condition and CMOS compatibility. Investigations such as aging tests, including thermal shock, thermal cycling, high-temperature tests, and passivation mechanisms will be crucial for various NW devices.
5) As technology matures, techniques used in conventional devices such as resonant-cavity-enhanced PDs, edge-illuminated waveguide, and evanescently coupled distributed PDs, and avalanche photodetectors can be implemented in NW-based counterparts.

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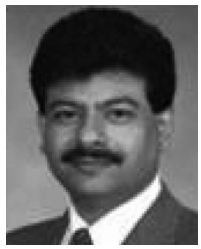

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