EEC 119B Spring 2014 Final Project:
System-On-Chip Module

Dept. of Electrical and Computer Engineering
University of California, Davis

Issued: March 14, 2014
Subject to Revision
Final Report Due: June 11, 2014, 6:00 PM

Reading: Rabaey [1].

Objective

The objective of this project is to create and verify through simulation an integrated circuit design targeted to a novel application. In addition to developing the design, project teams will evaluate transitioning the design to a product as either licensed intellectual property, as a standalone chip, or as a multi-chip set. The technical description and market analysis of the final design will be incorporated into a final project report.

Tool Setup

Use the Cadence tools setup that were used for the labs in 119A. Additional tool flows for synthesis, place and route are available and may be used at your discretion. Tutorials for these flows will be available on the class SmartSite.

Project Proposal and Abstract

Brainstorm among your teammates or others to decide on a particular application area for your system-on-chip design. Download and complete the *project proposal* document from the course SmartSite. The proposal is a preliminary document that must be reviewed by the instructional staff before your final project is approved. Expect the final project scope and specifications to be different from the original proposal in significant ways, especially to limit the size of the project to something that can be executed by a small team. Once the project is approved, prepare and submit the detailed *project plan* (see below).

Product Planning and Market Analysis

Part of the project includes an economic analysis which accounts for the costs and return on investment of creating a product around your system-on-chip module design. You will quantitatively evaluate three product models: (1) distributing the entire system-on-chip module as an intellectual property (IP) block so that it would be integrated in other chips sold by other chip vendors, as part of a larger system-on-chip (SoC), (2) selling the system-on-chip module as a standalone chip, which would be integrated into the application device. For example, if your module is designed for low-power image processing, it could be integrated into mobile phones by handset makers or bundled as part of the camera system-on-chip module by camera manufacturers. Finally (3), evaluate selling the module as a multi-chip set that could be integrated into a broader variety of products. The tradeoffs include lower costs and decreased time-to-market for Option 1, but higher profits for Option 2. For both options, you need to determine the sales price S_t ($/chip for Options 2 and 3, $/license or $/chip which includes the IP for Option 1). To find S_t, use the cost models from EEC 119A Lecture 8 supplemented with information you research. For example, you can use web resources to determine volume pricing of IC packages for Option 1. To give you an idea of current system component pricing, the camera system-on-chip modules in the iPhone 4S are estimated to cost $17.60 (this includes ICs, optics, packaging, and connectors) while the cost of the total bill of materials (BOM) is estimated to be $188. More detailed information on the iPhone 4S BOM is in the Resources section of the SmartSite, which you can use to get a sense of how much various IC components cost. You need to document in your final report in table form the following costs for each option:

1. Non-Recurring Engineering Costs (NRE's)
   (a) Engineering Design Cost C_E: Including labor, so you must estimate team size and development schedule, CAD tools, etc.
   (b) Prototype Manufacturing Cost C_{PT}: Obtain an online quote from the MOSIS IC prototype foundry service for the 180nm TSMC CMOS technology for a chip the size of your design. Use this cost for both options since the IP block would have to be tested in a standalone chip before the design can be marketed anyway.
2. Recurring Costs
   (a) Option 1: Assume 25% of the NRE's as recurring costs associated with maintaining documentation, providing customer support, porting the IP block to other process technologies.
   (b) Options 2 and 3: Include both the recurring total chip manufacturing costs and support costs. Assuming the following when computing total chip manufacturing cost C_t:
      i. Wafer Radius (r) = 10 cm (8 in. diameter wafers)
      ii. Wafer Cost (C_w) = $500
      iii. Die Fab Yield (Y_{df}): Calculate chip costs based on four yield values as a function of your design's area A. Use the Poisson and Murphy yield models assuming defect densities D of $10^{-3}/\text{mm}^2$ and $10^{-4}/\text{mm}^2$.

iv. Package Cost (C_{pa}): Find a standard package from the web (e.g., from Digi-Key) based on the number of I/O pins for your design. Assuming the highest possible quantities (i.e., the lowest price per package). This is an unrealistic assumption for some applications. For example, imager packages need transparent windows and so are higher cost, so you may be computing a lower bound on package cost with this estimate. Document whether this cost estimate is a lower or upper bound.

v. Test Cost (C_{te}) = \$0.10/pin (In general, the time and complexity of the testing is loosely proportional to the number of chip I/O's.)

vi. Packaged and Tested Yield ($Y_{pa}Y_{te}$) = 98%

Assume 20% of the total chip manufacturing cost as recurring costs due to overhead (documentation, field engineering support, sales and marketing, etc.).

For all three options, compute the cost assuming the system can be scaled to commercial size. For example, suppose your project involved designing an image processing module for a $3 \times 16 \times 16$ (256 pixels each for red, green, and blue) imager with a 4b ADC. Assuming a 5 megapixel imager (5MP) as used in the iPhone 4 with RGB pixels each with 8b resolution, you may need to scale your image buffer memory area by $\frac{5 \times 10^6}{256}$ and your ADC area by $2\times$. Relevant specifications for commercial products can be found using Internet resources. Document how you computed the scaled cost of your system-on-chip module using equations in your final report and presentation.

In addition to the product planning and cost analysis, you must also provide a brief market analysis for both options. Who would be your major customers? How many units can be sold? What are the geographically most important markets? When should a new and improved version of the product be launched? Use publicly available information from the business press and industry analysts such as Gartner Research to justify your market estimates. For example, in 2011 one of the design teams determined that testing for tuberculosis in South Asia and southern Africa would make the most economic sense for a mobile phone fluorescence microscopy imager module.

Project Plan

Your first deliverable will be a plan to execute your proposed project. This is a 3-4 page document plus a Gantt chart outlining project tasks, dependencies, and task durations. Your project plan must include the following sections:

1. Team: List the team members, choose a team name, and assign a team leader who is responsible for making final decisions regarding the system-on-chip module design.

2. System-On-Chip Module Design Task: Define and list subtasks, assign team members to each, and estimate duration of the subtasks.

3. Product Planning Task: Define and list subtasks, assign team members to each, and estimate duration of subtasks.

4. Milestones: Define and list milestones to be completed by each project status meeting and presentation (see below).

5. Schedule Risks: Define and list any unknowns which might negatively affect the proposed schedule and how much the schedule may be extended.

Project Meetings

Each team will be assigned a primary TA as a mentor to help oversee the design process. Regularly scheduled meetings (approximately every two-three weeks) will occur with each team, their primary TA, and the instructor to review progress and plan the next few weeks' activities. Each team member will give a brief oral report describing their individual contributions to the current progress of the team. Intermediate results, such as schematics, plots of preliminary simulations, or layouts must be shown at these meetings to enable the teaching staff to gauge progress.

Schedule

Important dates and deliverables for the design project are listed below:

- March 19, 2014: Project Plan and Gantt Chart
- Week 3 (April 14-18): Project Status Meeting
- April 28, 2014 (may move to April 21): Mid-Project Presentation
- Week 7 (May 12-16): Project Status Meeting
- May 30, 2014: System-On-Chip Module Design Completed (stretch goal)
  - System-on-chip module design will be verified against instructional staff/project team test bench. Power and performance will be determined by simulation of layout with extracted parasitic capacitances.
- June 4, 2014: System-On-Chip Module Design Completed (nominal goal)
- June 11, 2014: Final Project Presentations
  - Final Project Report due.

Project Presentations

Each team will make two presentations to the full class. The mid-project presentations will be done in lecture on April 21 or 28, 2014 and the final project presentations will be given during the final exam period scheduled for EEC 119B.

1. Mid-Project Presentations: Each team will have 10 minutes with 1-2 minutes each for questions. All team members must present. At the mid-project presentation, you must show the architecture of your system-on-chip module design including details such as the ADC architecture, size of your SRAM memory blocks, controller state diagram, etc. You should mark progress relative to your Gantt chart from your project plan and describe your approach to completing the project by the deadline.

2. Final Project Presentations: Each team will have 15 minutes with 2-3 minutes each for questions. All team members must present. At the final presentation, you must show the completed layout of your system-on-chip module and chip designs, provide a summary of the design with important figures of merit such as area, peak performance of the I^2C or other standard interface, and power consumption. You must also summarize your cost and market analysis. The presentation will serve as an oral summary of your written final report, which will include many more details about the design.

Report

You must hand in a **typewritten** report to receive credit for this project. Your report should be concise, but must include the following sections and sufficient supporting details such as plots, graphs, and tables. The list below is only a **guideline**. Add any material which you feel is important for the teaching staff to evaluate your work and each individual's contribution.

1. Executive Summary: Describe in a few paragraphs the objectives of the design including the key features of the system-on-chip module and the performance. Summarize the results of the project, including which units were completed and which were not (if any) and list any significant bugs which were not fixed. Also summarize the product planning and market analysis.

2. Architecture: This section documents the architecture of your system-on-chip module. Include a block diagram of your final design (which will likely be different than the one in your original project proposal). Describe your overall approach to design tradeoffs. Did you concentrate all the miscellaneous logic in a single controller or did you distribute the control functions among the other subunits? Also include a description of the individual blocks which should include information such as your architecture for the ADC and the SRAM organization (total memory size, partition into subarrays, etc.). Justify the design choices you made for each subunit. Include supporting details such as circuit schematics for important elements such as the comparator used in the ADC.

3. Functional Verification: Briefly document your approach to verifying the individual subunits. What were the testbenches that you used? Describe how you measured the simulated current and computed the average power for the system-on-chip module. Describe your strategy for generating your power characterization stimulus vectors. Someone reading this section should be able to easily duplicate your results by following the methodology described in this section.

4. Physical Design and Verification: Summarize your approach to completing the physical design. How did you floorplan your design? Did you use an automated layout flow (synthesis followed by place and route)? Did you use manual layout for some subunits? How did you place the I/O pads? Be sure to include a picture of the overall design layout with major functional units indicated in outline and report the total area for the design with and without the I/O pad ring.

5. Results and Discussion: Describe succinctly the delay, area, and power results produced by simulation. Include a summary table highlighting the important performance parameters. How could these parameters be further improved in future designs?

6. Product Planning and Market Analysis: Describe the results of your product planning and cost analysis as well as your market analysis. You must include any references to market data from the published literature which you used to justify your market size estimates. Make a product recommendation between the two options (licensed IP or standalone chip) and justify it.

7. Lessons Learned: Discuss the technical lessons, and share the insight that you gained. What would you do differently if you had to do this all over again? What advice do you have for students who will take this course next year? Also, discuss your non-technical lessons including management of human resources (the team), workload partitioning, scheduling, collaboration, etc. You may also include feedback to the instructor for improving the course in future offerings. Your feedback would be highly appreciated.

8. Contribution Breakdown: Clearly discuss the tasks that each member of the team worked on and/or had primary responsibility for. If a component is jointly developed by the team, give a rough breakdown of contribution percentage: for example, if two members were the primary developers of a component, each should indicate 50% contribution to development of that component. Design ideas/plans are sometimes developed by the entire team and not one or two individual members, in which case, each member should indicate equal contributions. Be sure to indicate work that was performed to research algorithms, test, debug, prepare reports and presentations, and complete the product planning/market study.

9. Broader Impact: Describe the outcome of your project in terms of impacting society. If your project was turned into a successful commercial product, how would it affect human health, affect the environment, or improve economic or living conditions for people using the product?

Peer Evaluation

At the end of the project, you will be submitting evaluations of the performance of your peers by filling out a questionnaire and distributing points based on your team members' contributions to the project. These peer evaluations will be used in part to determine your final grade in the class, so take them seriously.

References

[1] J. Rabaey, A. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits: A Design Perspective*, 2nd ed. Upper Saddle River, New Jersey: Prentice-Hall, Inc., 2003.

EEC 119B Spring 2014 Project Checklist and Summary

Team Name:
Team Members:
TA:

Deliverable	Checkoff	TA Initials	Date
Project Plan			
Gantt Chart			
Week 4 Project Status Meeting			
Week 7 Project Status Meeting			
Module Design Completed (Stretch Goal)			
Module Design Completed (Nominal Goal)			
Parameter	Value		
Module Architecture Block Diagram			
Transistor Count			
Area (core)			
Area (including pad ring)			
Power			
Other (TBD from Project Proposal)			