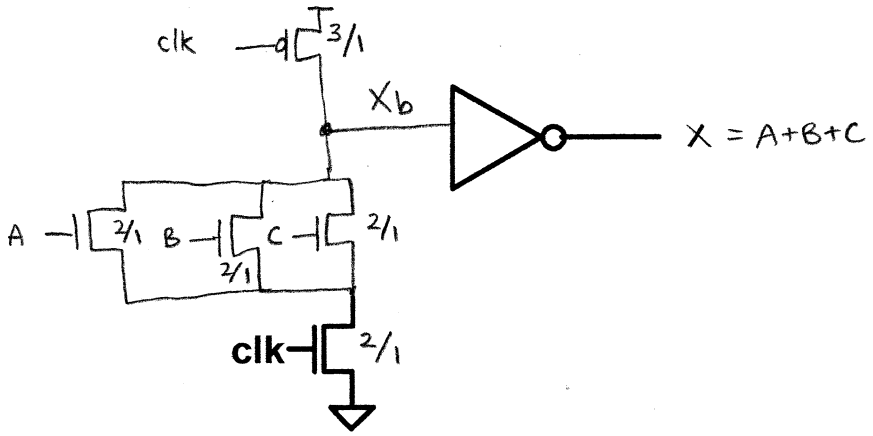
Quiz #4 **EEC118** **Spring 2011**

Name: Solutions Lab Section:_____

Problem 1 (7 points) Complete the following Domino-style dynamic logic three-input OR gate. Size the transistors such that the worst case precharge time (rise time for min. size inverter) equals the worst case evaluation time assuming V_{DD}=3.3V, V_{TN}=|V_{TP}|=1V, μ_N=3μ_P=300μA/V^2, γ=0, λ=0, W_{min}=1μm, L_{min}=1μm, while minimizing area. Label the inputs A, B, C, clk, the dynamic node Xb, and the output X.



Sizes 3pts.
topology 2pts.
labels 2pts.

Problem 2 (3 points) For the following 1 transistor DRAM cell, fill in the boxes labeling the corresponding wires with the appropriate signal names:

Q: data storage bit

BL: bit line

WL: word line