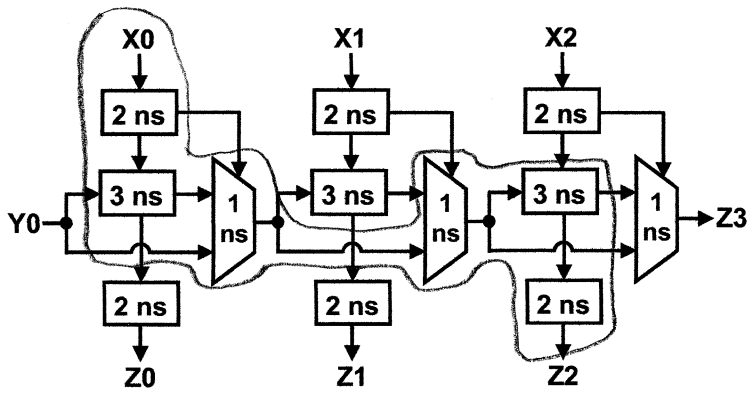
Quiz #3 **EEC118** **Spring 2011**

Name: Solutions Lab Section:_____

Problem 1 (3 points) For the carry bypass adder circuit below, circle the longest delay(s) (critical paths) from inputs to outputs. The delay number represents the delay from any input to any output for that block. What is the worst case delay?

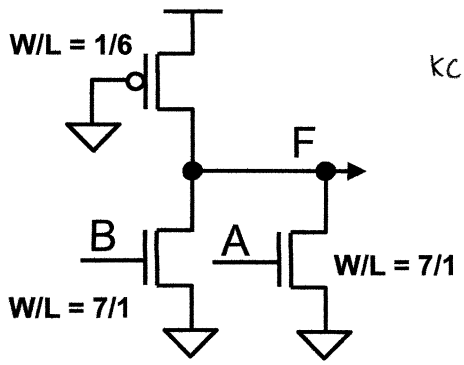


$t_{wc} = 2ns + 3ns + 1ns + 1ns + 3ns + 2ns$
$= \boxed{12ns}$

Problem 2 (2 points) Suppose the bypass paths (two-to-1 muxes) are taken out of the circuit. What is the worst case delay?

$t_{wc} = 2ns + 3ns + 3ns + 3ns + 2ns = \boxed{13ns}$

Problem 3 (5 points) For the circuit below, assume: $V_{DD} = 3V$, $V_{T,n} = 1V$, $V_{T,p} = -1V$, $\mu_p C_{ox} = (1/2) \times 10^{-4}\ A/V^2$, $\mu_n C_{ox} = 2 \times 10^{-4}\ A/V^2$, $\lambda = 0$. What logic function does the circuit implement? What is the worst case VOL for the circuit? State any reasonable assumptions you make.



$\boxed{F = \overline{A+B} \quad \text{NOR2}}$

Assume V_{OL} small $\Rightarrow$ PMOS sat., NMOS linear

KCL: $\mu_n C_{ox}\left(\frac{W}{L}\right)\left[(V_{DD} - V_{T,n})V_{OL} - \frac{V_{OL}^2}{2}\right] = \frac{\mu_p C_{ox} W}{2L}(-V_{DD} - V_{T,p})^2$

$\left(2\cdot 10^{-4}\frac{A}{V^2}\right)\left(\frac{7}{1}\right)\left[2V\cdot V_{OL} - \frac{V_{OL}^2}{2}\right] = \left(\frac{1}{2}\cdot 10^{-4}\frac{A}{V^2}\right)\frac{(-3V + 1V)^2}{2}\left(\frac{1}{6}\right)$

Assume V_{OL}^2 small,

$\boxed{V_{OL} = 5.95\,mV}$

Using quadratic formula:

$V_{OL} = \boxed{5.96\,mV}$, $\cancel{3.99V}$

$> V_{GS} - V_{T,n}$ so not linear

also $> V_{DD}$!