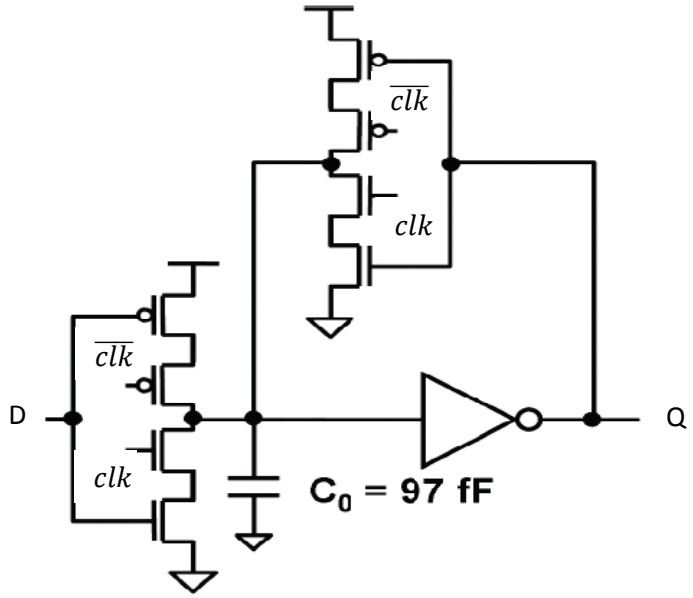
EEC 118 Solutions to Homework #5

Problem 1.1



We want the latch to be transparent when clk is positive, so we put clk at the gates of the NMOS's and clk_bar at the gates of the PMOS's. The feedback inverter makes it static instead of dynamic.

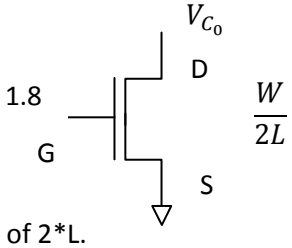
Problem 1.2

Since the output equals the input after some delay, we imagine the input D at V_{DD} and the output Q low before the clk signal goes high. We're given the t_{pLH} for the second inverter which is the delay for the output to go from GND to 0.5 V_{DD}. Assuming that t_{pLH2} is the time from when the input changes to it's 50% value till the output rises to the 50% value, the t_{pLH} from the input to the output is approximately$t_{HL1} + t_{pLH2}$ because we need the time it takes the voltage at the capacitor V_{C_0}or the input to the second inverter to become 0.5 V_{DD}. We don't have to calculate the full fall time for the first inverter.

Using the average current method, $\tau_{pHL1} = \frac{C_{load}\Delta V}{I_{avg}}$ where ΔV is 0.5V_{DD}.

$$I_{avg} = \frac{1}{2}\left[I\left(V_{in} = 1.8, V_{C_0} = 1.8\right) + I\left(V_{in} = 1.8, V_{C_0} = 0.9\right)\right]$$

Saturation since $V_{DS} \geq V_{GS} - V_{T,n}$ Linear since $V_{DS} < V_{GS} - V_{T,n}$



We can treat the two NMOS in series as one NMOS with an effective length of 2*L.

$$I_{avg} = \frac{k_n}{4}\left[\left(V_{GS} - V_{T,n}\right)^2 + 2\left(V_{GS} - V_{T,n}\right)V_{DS} - {V_{DS}}^2\right] = \frac{300\mu A}{4}\frac{0.45}{2 * 0.180}\left[1.2^2 + 2(1.2)(0.9) - 0.9^2\right]$$
$$= 262\ \mu A$$

$\tau_{HL} = \frac{97\ fF*0.9\ V}{262\ \mu A} = \underline{333\ \text{ps}}$ $\boxed{t_{pLH} = 333\ ps + 45\ ps = 378\ ps}$

You can also use the 2nd approximation using the saturation current, which gives $\tau_{HL} = 323$ ps and $\boxed{t_{pLH} = 323\ ps + 45\ ps = 368\ ps}$.

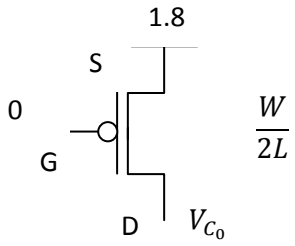
Problem 1.3

The same can be done as in the previous problem, but for the output falling from high to low and the input low before clock goes high. Therefore, we will be focus on the PMOS in the first inverter, and the second inverter has t_{pHL} = 45 ps.

$$I_{avg} = \frac{1}{2}\left[I\left(V_{in} = 0, V_{C_0} = 0\right) + I\left(V_{in} = 0, V_{C_0} = 0.9\right)\right]$$

Saturation since $|V_{DS}| \geq |V_{GS}| - |V_{T,p}|$

Linear since $|V_{DS}| < |V_{GS}| - |V_{T,p}|$



$$I_{avg} = \frac{k_p}{4}\left[\left(V_{GS} - V_{T,p}\right)^2 + 2\left(V_{GS} - V_{T,p}\right)V_{DS} - {V_{DS}}^2\right]$$

$$= \frac{100\mu A}{4}\frac{1.44}{2*0.180}[(-1.1)^2 + 2(-1.1)(-0.9) - (-0.9)^2] = 238\ \mu A$$

$\tau_{pLH1} = \frac{97\ fF*0.9\ V}{238\ \mu A} = 367$ ps $\boxed{t_{pHL} = 367\ ps + 45\ ps = 412\ \text{ps}}$

Using the second average current approximation, $\boxed{t_{pHL}}$ =360 ps + 45 ps = 405 ps

Problem 1.4

The Master stage latch in the flip-flop determines when a signal is "let in" or is the first of the two cascaded latches. In this case since the flip-flop is negative edge triggered, meaning that the output will hold the input value when the clock goes low, the master latch is active when the clock is high. The setup time is the time the input has to be stable before the active edge so that it can propagate to the input of the slave stage and be held. In this case, the longest possible propagation delay will determine the setup time. The longest propagation delay we see from the ideal clock pulse to the output changing to the 50% value is 412 ps. To be more conservative so that output reaches GND and since it's an ideal clock, it would most likely take another 45 ps resulting in a setup time of <u>457 ps.</u>