EEC 118: Solutions to Homework #3

Problem 1.1 Sizing

Solve for $\frac{W_n}{W_p}$, given $V_M = V_{in} = V_{out} = 2.2\ V$ and $t_r = 5$ ns

Since V_{DD}= 5V, and assuming $V_{OH} = 5$V and V_{OL} = 0 V, $V_{10\%}$ = 0.5 V and $V_{90\%}$ = 4.5 V

$$I_{avg} = \frac{1}{2}[I(V_{in} = \overset{0}{\cancel{V_{OL}}}, V_{out} = 0.5\ V) + I(V_{in} = \overset{0}{\cancel{V_{OL}}}, V_{out} = 4.5\ V)]$$

$|V_{DS}| > |V_{GS}| - |V_{th}|$?
4.5 > 5-1
Saturation for PMOS

$|V_{DS}| > |V_{GS}| - |V_{th}|$?
0.5 > 5-1
linear for PMOS

$$I_{avg} = \frac{1}{2}\left[\frac{1}{2}k_p\left(V_{GS} - V_{T,P}\right)^2 + \frac{1}{2}k_p\left[2\left(V_{GS} - V_{T,P}\right)V_{DS} - V_{DS}^2\right]\right]$$

$$= \frac{1}{4}k_p[16 + 2(-5+1)(-0.5) - (-0.5)^2] = \frac{W_p}{L_p} \times 98.75\ \mu A$$

$$\tau_{rise} = \frac{C*\Delta V}{I_{avg}} \quad \rightarrow \quad 5E-9 = \frac{2E-12\ F*4}{\frac{W_p}{L_p}\times 98.75\ \mu A} \rightarrow \boxed{W_p \cong 16.2\ \mu m}$$

$$V_M = \frac{V_{T,n} + \sqrt{\frac{1}{k_R}}(V_{DD} + V_{T,p})}{\left(1 + \sqrt{1/k_R}\right)} \quad \rightarrow \quad 2.2 = \frac{0.8 + \sqrt{\frac{1}{k_R}}(5-1)}{(1+\sqrt{1/k_R}} \quad \rightarrow \quad k_R = 1.65$$

$k_R = \frac{k_n}{k_p} = \frac{\mu_n C_{ox} W_n}{\mu_p C_{ox} W_p}$ assuming minimum lengths $\rightarrow$ $1.65 = \frac{5}{2}\frac{W_n}{16.2} \rightarrow \boxed{W_n = 10.69\ \mu m}$

Problem 1.2 Delay

$\tau_{pd} = ?\ \ \tau_{pd} = \frac{\tau_{PHL} + \tau_{PLH}}{2}$

From lecture #5, $\tau_{PHL} = \frac{C_{load}}{k_n(V_{DD} - V_{T,n})}\left[\frac{2V_{T,n}}{V_{DD} - V_{T,n}} + \ln\left(\frac{4(V_{DD} - V_{T,n}}{V_{DD}} - 1\right)\right]$

$$\tau_{PLH} = \frac{C_{load}}{k_p(V_{DD} - |V_{T,p}|)}\left[\frac{2|V_{T,p}|}{V_{DD} - |V_{T,p}|} + \ln\left(\frac{4(V_{DD} - |V_{T,p}|}{V_{DD}} - 1\right)\right]$$

$\tau_{PHL} = \frac{2E-12}{50*10^{-6}*10.69*4.2}\left[\frac{1.6}{4.2} + \ln(\frac{4*4.2}{5} - 1)\right]$= 1.104 ns

$\tau_{PLH} = \frac{2E-12}{20*10^{-6}*16.2*4}\left[\frac{2}{4} + \ln(\frac{4*4}{5} - 1)\right]$= 1.988 ns $\quad \boxed{\tau_{pd} = \frac{1.104+1.988}{2} = 1.546\ ns}$

Problem 1.3

If V_{DD} decreases from 5 V to 3.3 V, then

τ_p will increase.

V_M will decrease.

$V_M \approx$ 1.42 V

$\tau_{PLH} \approx$ 3.898 ns

$\tau_{PHL} \approx$ 2.038 ns

$\tau_{pd} \approx$ 2.965 ns

In the equations above we see that V_M and τ_{pd} depend on V_{DD}. Obviously, V_M will decrease because it scales with the supply voltage. Conceptually, τ_{pd} increases because although ΔV is smaller, the average current is a lot less. Remember, $\tau = (C * \Delta V)/I_{avg}$.

Problem 2.1 Sizing

τ_{PHL}< 0.825 ns $\quad C_{out} = 500 \text{ fF} + C_{db,n} + C_{db,p}$

$C_{db.n} = (100 + 9W_n)$ fF

$C_{db.p} = (80 + 7W_p)$ fF

$$0.825 \text{ E-9} = \frac{C_{out}}{(W_n/L_n)*50*10^{-6}*4.2} * 1.239 \quad \rightarrow \quad \frac{C_{out}}{W_n} = 1.398\text{E-13}$$

$$(680 + 9W_n + 7W_p) * 10^{-15} = W_n * 1.398 * 10^{-13} \rightarrow 680 + 9W_n + 7W_p = 139.8W_n$$

$$V_M = 2.4 = \frac{0.8+\sqrt{\frac{1}{k_R}}(5-1)}{1+\sqrt{1/k_R}} \quad \rightarrow \quad k_R = 1 \rightarrow \frac{W_n}{W_p} = \frac{2}{5} \quad \rightarrow \quad W_p = \frac{5}{2} * W_n$$

Plug into above equation

$$680 + 9W_n + \frac{35}{2}W_n = 139.8W_n \quad \rightarrow$$

W_n= 6 (assume in microns in problem)

W_p= 15 μm

Problem 2.2 Rise and Fall Times

There are many ways to calculate and approximate the inverter delay as well as different metrics as seen in class. Here, we use the first order approximation.

$\tau_{rise} = \frac{C*\Delta V}{I_{avg1}} = \frac{250*10^{-15}*4}{I_{avg1}}$ $\tau_{fall} = \frac{C*\Delta V}{I_{avg2}} = \frac{250*10^{-15}*4}{I_{avg2}}$

$I_{avg1} = \frac{1}{2}\left[\frac{1}{2}k_p\left(V_{GS} - V_{T,p}\right)^2 + \frac{1}{2}k_p\left[2\left(V_{GS} - V_{T,p}\right)V_{DSp} - {V_{DSp}}^2\right]\right] = 1.481 \text{ mA}$

$\tau_{rise} = \frac{250*10^{-15}*4}{1.481*10^{-3}} = \boxed{0.675 \text{ ns}}$

$I_{avg2} = \frac{1}{2}\left[\frac{1}{2}k_n\left(V_{GS} - V_{T,n}\right)^2 + \frac{1}{2}k_p\left[2\left(V_{GS} - V_{T,n}\right)V_{DSn} - {V_{DSn}}^2\right]\right] = 1.619 \text{ mA}$

Vout = 0.5

$\boxed{\tau_{fall} = 0.618 \text{ ns}}$

Problem 3.1 Rise and Fall Times

(1) Exact Method (differential equations)

τ_{fall} $C\frac{V_{out}}{dt} = -\frac{1}{2}k_n\left(V_{in} - V_{T,n}\right)^2$

nMOS in saturation for $4\ V \leq V_{out} \leq 4.5\ V$

$\frac{dV_{out}}{dt} = -2.4 * 10^9\ {}^{V}/_{s}$

$\int_{t=0}^{t=t_{sat}} dt = -\frac{1}{2.4*10^9}\int_{V_{out}=4.5}^{4} dV_{out}$

$t_{sat} = \frac{0.5}{2.4*10^9} = 0.2083\ ns$

nMOS in linear region for $0.5 \leq V_{out} \leq 4\ V$

$C\frac{V_{out}}{dt} = -\frac{1}{2}k_n\left[2\left(V_{in} - V_{T,n}\right)V_{out} - V_{out}^2\right]$

$\int_{t=t_{sat}}^{t=t_{delay}} dt = -6.\bar{6} * 10^{-9}\int_{4}^{0.5} \frac{dV_{out}}{8V_{out} - V_{out}^2}$

$t_{delay} - t_{sat} = 2.23\ ns$

$\boxed{t_{fall} = 2.23 + 0.2083 = 2.4383\ ns}$

τ_{rise} $C\frac{dV_{out}}{dt} = \frac{1}{2}k_p\left(V_{in} - V_{DD} - V_{T,p}\right)^2$

pMOS in sat'n for $0.5\ V \leq V_{out} \leq 1.2\ V$

$\frac{dV_{out}}{dt} = -2.406 * 10^9\ {}^{V}/_{s}$

$\int_{t=0}^{t=t_{sat}} dt = -\frac{1}{2.406*10^9}\int_{V_{out}=0.5}^{1.2} dV_{out}$

$t_{sat} = \frac{0.7}{2.406*10^9} = 0.2908\ ns$

pMOS linear for $1.2\ V \leq V_{out} \leq 4.5\ V$

$C\frac{V_{out}}{dt} = -\frac{1}{2}k_p\left[2\left(V_{GS} - V_{T,p}\right)V_{DS} - V_{DS}^2\right]$

$\int_{t=t_{sat}}^{t=t_{delay}} dt = 5.\bar{9} * 10^{-9}\int_{1.2}^{4.5} \frac{dV_{out}}{38 - 7.6V_{out} - (5 - V_{out})^2}$

$t_{delay} - t_{sat} = 2.059\ ns$

$\boxed{t_{rise} = 2.059 + 0.2908 = 2.3498\ ns}$

(2) Approximate method (average current)

$\tau_{fall} = \frac{C\Delta V}{I_{avg}} = \frac{1.5*10^{-12}*4}{I_{avg}}$ $\tau_{rise} = \frac{C\Delta V}{I_{avg}} = \frac{1.5*10^{-12}*4}{I_{avg}}$

$I_{avg} = \frac{1}{2}\left[k_n\left(V_{in} - V_{T,n}\right)^2 + \frac{1}{2}k_n\left[2\left(V_{in} - V_{T,n}\right)V_{out} - V_{out}^2\right]\right]$ =2.2 mA

$\boxed{\tau_{fall} = 2.7 \text{ ns}}$

$I_{avg} = \frac{1}{2}\left[k_p\left(V_{in} - V_{DD} - V_{T,p}\right)^2 + \frac{1}{2}k_p\left[2\left(V_{in} - V_{DD} - V_{T,p}\right)V_{DS,p} - V_{DS,p}^2\right]\right]$ =2.248 mA

$\boxed{\tau_{rise} = 2.668 \text{ ns}}$

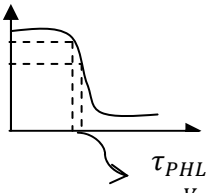
Problem 3.2 Frequency

$f = \frac{1}{2\tau_{pd}} \quad \rightarrow \quad \tau_{pd} = \tau_{PHL} + \tau_{PLH}$

$\tau_{PHL} = \frac{1.5*10^{-12}}{45*10^{-6}*10*(5-1)}\left[\frac{2}{4} + \ln\left(\frac{4*4}{5} - 1\right)\right] = 1.07$ ns

$\tau_{PLH} = \frac{1.5*10^{-12}}{25*10^{-6}*20*3.8}\left[\frac{2.4}{3.8} + \ln\left(\frac{4*3.8}{5} - 1\right)\right] = 2.11$ ns

$\tau_{pd} = 3.18$ ns $\quad \boxed{f = \frac{1}{6.36*10^{-9}} \cong 157 \text{ MHz}}$



τ_{PHL} only spans from $V_{DD} - V_{T,n}$ to $\frac{V_{DD}}{2}$, but the problem asks for the full logic swing. Thus, $f = \frac{1}{\tau_{rise}+\tau_{fall}} = \frac{1}{2(\tau_{PHL}+\tau_{PLH})}$

Problem 3.3 Power

$Power = C_{load} * V_{DD}^2 * f = 1.5 * 10^{-12} * 5^2 * 157 * 10^6 \cong \boxed{5.91 \text{ mW}}$

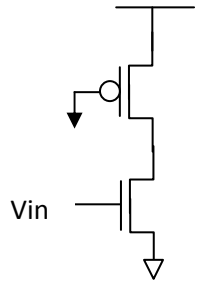
Problem 3.4 Redesign

$\tau_{PHL} = \frac{m}{\frac{W_n}{L_n}} \quad \rightarrow \quad 0.75\tau_{PHL} = 0.75\frac{m}{\frac{W_n}{L_n}} \quad \rightarrow 0.75\tau_{PHL} = \frac{m}{\frac{W_n}{L_n}*\frac{1}{0.75}}$

This means $\left(\frac{W_n}{L_n}\right)_{new} = \frac{10}{0.75} = \boxed{13.3}$

And same for $\left(\frac{W_p}{L_p}\right)$ $\rightarrow \left(\frac{W_p}{L_p}\right)_{new} = \frac{20}{0.75} = \boxed{26.6}$ V_M doesn't change because K_R doesn't

Problem 4.1 Sizing



$V_M = V_{in} = V_{out} = 1.4$ V

PMOS $|V_{DS}| = 1.9$ V $\quad |V_{DS}| > |V_{GS} - V_{T0}|$?

$|V_{GS}| = 3.3$ V $\quad 1.9\,! > 2.6, \therefore linear$

$|V_{T0}| = 0.7$ V

NMOS $V_{DS} = 1.4 \quad V_{DS} > |V_{GS} - V_{T0}|$ saturation

$V_{GS} = 1.4$

$I_{DN} = \frac{\mu_n C_{ox}}{2}\frac{W_n}{L}(1.4 - 0.6)^2 \quad I_{DP} = \frac{\mu_p C_{ox}}{2}\frac{W_p}{L}\left[2\left(3.3 — 0.7\right|\right)1.9 - 1.9^2$

$I_{DN} = I_{DP}$, $\boxed{\frac{W_n}{W_p} = 4.08}$ It is 4.38 times bigger than $\frac{W_n}{W_p}$. We need a bigger NMOS here.

Problem 4.2 Noise Margins

V_{OH} $V_{in} = 0 \rightarrow$ NMOS in cut-off,

$V_{GS,p} > V_{T0,p}$ conducts but no current then there is no voltage drop at $V_{DS,p} \rightarrow V_{out} = \underline{V_{OH} = 3.3\text{ V}}$

V_{OL} assume $V_{in} = V_{OH} = V_{DD} = 3.3$ V, then NMOS is linear bc $V_{DS,n} < (V_{GS,n} - V_{T0,n})$

PMOS is in saturation

Then $I_{DN} = \frac{\mu_n C_{ox}}{2}\frac{W_n}{L}[2(3.3 - 0.6)V_{OL} - V_{OL}^2]$ and $I_{DP} = \frac{\mu_p C_{ox}}{2}\frac{W_p}{L}(|-3.3| - |-0.7|)^2$

$I_{DN} = I_{DP} \rightarrow V_{OL}^2 - 5.4V_{OL} + 0.69 = 0 \quad \underline{V_{OL} = 0.13\,V}$

V_{IL} $V_{in} = V_{IL}$ then NMOS → $V_{DS} > (V_{GS} - V_{t0})$ saturation

PMOS → linear region

$\frac{\mu_n C_{ox}}{2}\frac{W_n}{L}(V_{IL} - 0.6)^2 = \frac{\mu_p C_{ox}}{2}\frac{W_p}{L}[2(3.3 - |-0.7|)(V_{out} - 3.3) - (V_{out} - 3.3)^2]$

$\frac{60}{25}\frac{W_n}{W_p}(V_{IL} - 0.6)^2 = -5.2(V_{out} - 3.3) - (V_{out} - 3.3)^2$

$9.79[2(V_{IL} - 0.6)] = -5.2\left(\frac{\partial V_{out}}{\partial V_{in}}\right)^{-1} - 2\left(\frac{\partial V_{out}}{\partial V_{in}}\right)^{-1}(V_{out} - 3.3), \quad \underline{V_{out} = 9.79V_{IL} - 5.175}$

$$9.79(V_{IL}-0.6)^2 = -5.2(9.79V_{IL}-5.175-3.3)-(9.79V_{IL}-5.175-3.3)^2$$

$$105.63V_{IL}^2 - 126.78V_{IL} + 31.28 = 0 \quad \underline{V_{IL} = 0.85\ \text{V}}$$

V_{IH} $V_{in}=V_{IH}$ then NMOS → $V_{DS}\ !> V_{GS}-V_t$ linear

PMOS → $V_{DS} > V_{GS}-V_t$ saturation

$$\frac{\mu_n C_{ox}}{2}\frac{W_n}{L}[2(V_{IH}-0.6)V_{out}-V_{out}^2] = \frac{\mu_p C_{ox}}{2}\frac{W_p}{L}(3.3-0.7)^2$$

$$2(V_{IH}-0.6)V_{out}-V_{out}^2 = \frac{25}{60}\frac{1}{4.08}6.76$$

$$2V_{out} + 2(V_{IH}-0.6)\left(\frac{\partial V_{out}}{\partial Vin}\right)^{-1} - 2V_{out}\left(\frac{\partial V_{out}}{\partial Vin}\right)^{-1} = 0 \qquad V_{out} = 0.5V_{IH} - 0.3$$

$$2(V_{IH}-0.6)(0.5V_{IH}-0.3)-(0.5V_{IH}-0.3)^2 = 0.69$$

$$0.75V_{IH}^2 - 0.9V_{IH} - 0.42 = 0 \qquad V_{IH} = 1.56\ \text{V}$$

$$\boxed{\begin{aligned} NM_L &= V_{IL} - V_{OL} = 0.72\ V \\ NM_H &= V_{OH} - V_{IH} = 1.74\ V \end{aligned}}$$

Problem 4.3 Overdrive

Want V_{OL}=0.6V PMOS: $V_{GS} = -3.3\ V, V_{DS} = -2.7\ V < V_{GS} - V_{T0}$ → saturation

NMOS: $V_{DS} = V_{OL} = 0.6$ V assume linear

$$I_{D,N} = I_{D,P} \qquad \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_n\left[2(V_{in}-V_{T,n})V_{OL}-V_{OL}^2\right] = \frac{\mu_p C_{ox}}{2}\left[V_{GS}-V_{T0,p}\right]^2$$

$$\frac{60\mu A/V^2}{2}(8)[2(V_{in}-0.6\ V)(0.6\ V)-0.6^2] = \frac{25\mu A/V^2}{2}(12)[-3.3+0.7]^2$$

$\boxed{V_{in} = 4.42\ V}$ $V_{GS} = V_{in}$, $4.42\ V - 0.6V = 3.82\ V$ $> V_{DS}$ yes, linear

Problem 5.1 Function

The highest voltage V_{out} can reach before NMOS cuts off is $\boxed{V_{DD} - V_{T,n} = V_{OH}}$

The lowest voltage V_{out} can reach before PMOS cuts off is $0\ V - V_{T,p}$ → $\boxed{V_{OL} = |V_{T,p}|}$

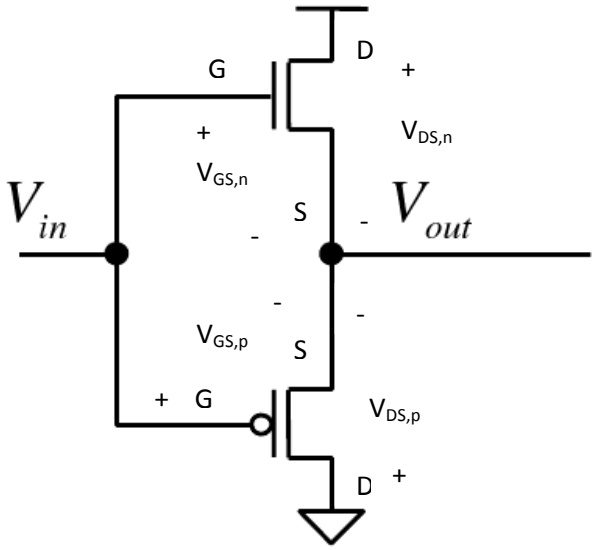
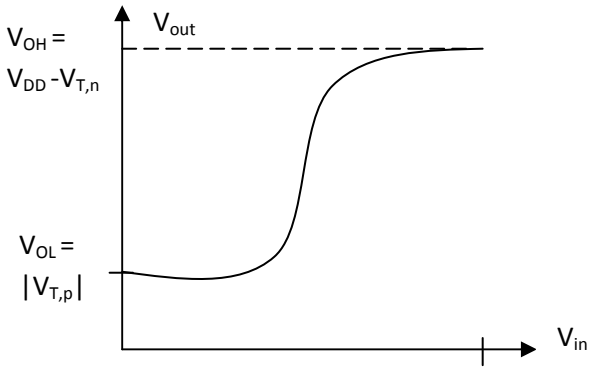
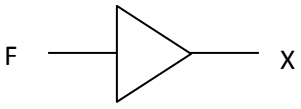


Figure 2: Circuit X.



Vin	Vout
0	0
1	1



X = F, buffer!

Problem 5.2 Switching Threshold

There is not enough information to calculate exactly, so make some plausible assumptions:

Assume $k_R = 1$ (just like ideal CMOS inverter)

$V_{T,n} = |V_{T,p}|$ (symmetric device thresholds)

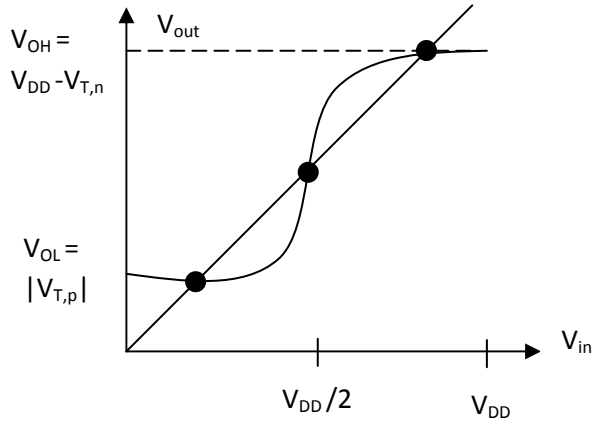
$V_{DD} > V_{T,n} + |V_{T,p}|$ (devices both on at same time under <u>some</u> Vin condtions)

Under these assumptions, the device currents for both NMOS and PMOS are <u>equal</u> for equal V_{GS} ($V_{GS,n} = V_{GS,p}$).

Since $V_{TH}=V_{in}=V_{out}$ → $V_{GS,p}=V_{GS,n}=0$ → NMOS, PMOS both in cutoff $I_{Dn,p}=0$

However, they have <u>finite impedance</u> due to <u>subthreshold</u> conduction; these will be equal, therefore: $\boxed{V_M = {}^{V_{DD}}/_2}$

Graphical solution:



Three points where VTC meets Vin=Vout line. Two of those points are where Vout=V_{OL} and Vout=V_{OH} → circuit is not switching. Therefore, V_M=V_{DD}/2

Problem 5.3 Switching Threshold

Suppose the input can swing between 0 V an V_{DD}:

$$\Delta V_{in} = V_{DD} - 0\,V = V_{DD}$$

The output can only swing from

$$\Delta V_{out} = V_{OH} - V_{OL} = V_{DD} - V_{T,n} - |V_{T,p}| < \Delta V_{in}$$

Problem 5.4 Discussion

Normally, we want logic gate output swings to be <u>larger</u> than input swings (this is called level restoration) so that input noise affects the output less. Therefore, this buffer is <u>not</u> suitable as a logic gate since $\Delta V_{out} < \Delta V_{in}$.