Problem 1.1 : Moore's Law for Microprocessors

Depending on starting assumptions and where you get the growth rate, answers may vary significantly.

Can use an exponential growth formula

$y = a(1+r)^X$

$a =$ starting amount

$r =$ growth or decay rate

$x =$ time intervals that have passed

Integration complexity assuming growth of 4x every 3 years as on p. 7 of Rabaey and starting with 400M transistors in year 2005

$y = 400*10^6(4)^{x/3}$

$@\,2010 \rightarrow x = 5,\ y \approx 4*10^9\,Transistors$

$@\,2015 \rightarrow x = 5,\ y \approx 4*10^{10}\,Transistors$

$@\,2020 \rightarrow x = 5,\ y \approx 4*10^{11}\,Transistors$

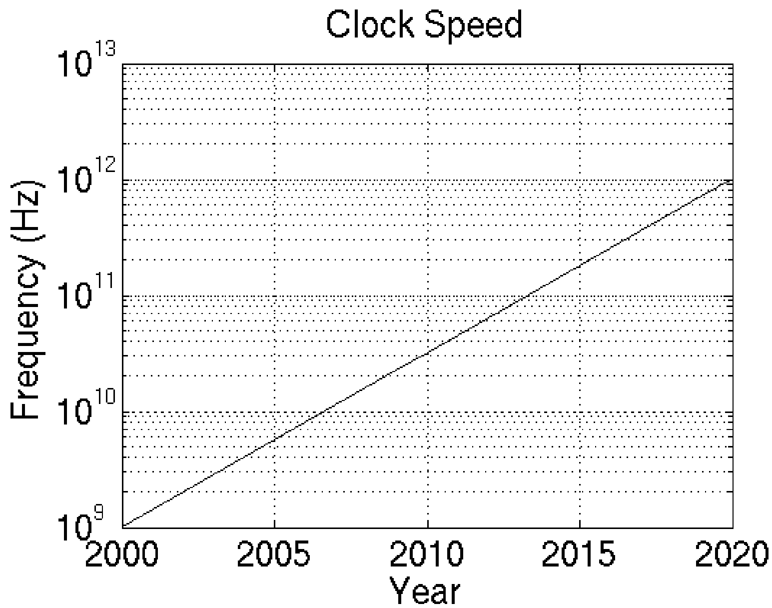
Frequency assuming growth of 2x every 2 years and starting with 1GHz in year 2000

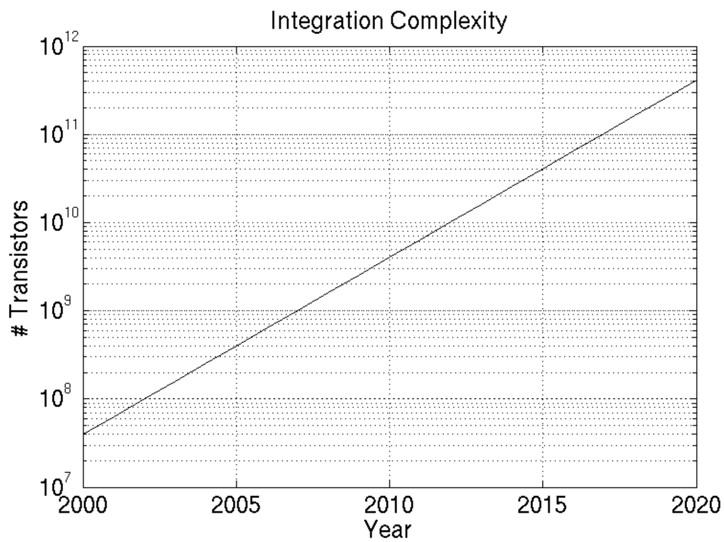
$y = 1*10^9(2)^{x/2}$

$@\,2010 \rightarrow x = 10,\ y \approx 3.2*10^{10}\,Hz$

$@\,2015 \rightarrow x = 15,\ y \approx 1.810*10^{11}\,Hz$

$@\,2020 \rightarrow x = 20,\ y \approx 1.024*10^{12}\,Hz$





Problem 1.2 : Moore's Law for DRAM

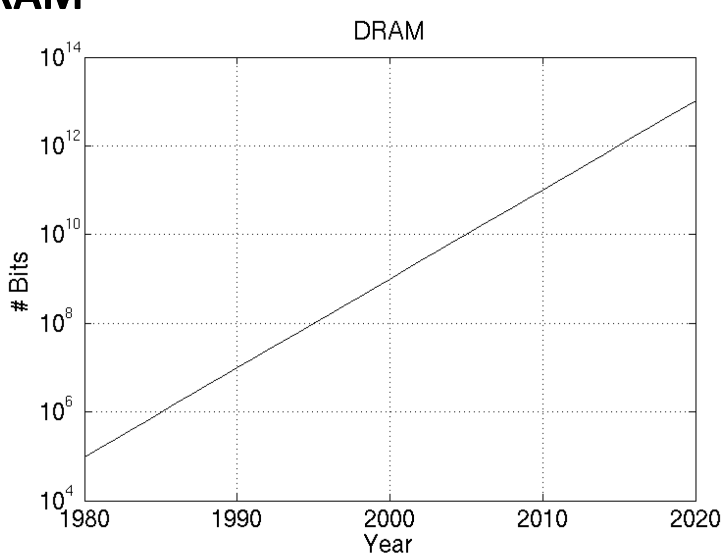
Number of DRAM bits assuming growth of 2x every 18 months as on p. 7 of Rabaey and starting with 1Gb in year 2000

$y = 1*10^9(2)^{x/1.5}$

$@\,2010 \rightarrow x = 10,\ y \approx 1*10^{10}\,bits$

$@\,2015 \rightarrow x = 15,\ y \approx 32*10^{10}\,bits$

$@\,2020 \rightarrow x = 20,\ y \approx 1*10^{11}\,bits$



Problem 2.1 : Quality Metrics

There is no "right" answer to this problem. What is considered a priority is almost entirely dependent on what the target application is, as well as how your company wishes to market its product(s).

All of these metrics can also influence each other. Pretend we are designing a processor to go into the next generation of cell phones. Power might be our #1 priority to enable the phone to run a long time without charging. We could lower the clock frequency (performance), remove support for some functions (robustness/functionality), or even add dedicated circuitry (cost) all of which are capable of reducing power. But as with all of engineering, nothing comes for free.

Problem 3.1 : Threshold Voltage

$$Cox = \frac{eox}{tox} = \frac{3.9*8.854*10^{-14}}{200*10^{-8}} = 1.72*10^{-7}\ F/cm^2$$

$$\phi_F = \frac{kT}{q}\log\left(\frac{N_i}{N_a}\right) \approx -0.3V \quad (\text{Eqn. not necessary, K \& L p.85})$$

$$\begin{aligned} Q_{B0} &= -\sqrt{2qN_A\varepsilon_{si}\left|-2\phi_F\right|} \\ &= -\sqrt{2(1.6*10^{-19})(2*10^{15})(11.7*8.854*10^{-14})|0.6|} \\ &= -2.02*10^{-8}\ C/cm^2 \qquad (\text{double check your units!}) \end{aligned}$$

$$\begin{aligned} V_{T0} &= \phi_{GC} - 2\phi_F - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}} \\ &= -0.85 + 0.6 - \frac{-2.02*10^{-8}}{1.72*10^{-7}} - \frac{(1.6*10^{-19})(2*10^{11})}{1.72*10^{-7}} \\ &\approx -0.32V \end{aligned}$$

Problem 3.2 : Channel Implant

Because the threshold in the previous problem was negative, dopants should be p-type. If we start with more holes, this will require a larger positive bias to generate strong inversion which is equivalent to having a more positive threshold (p.96-97 K&L).

$$Cox = \frac{eox}{tox} = 1.72*10^{-7}\ F/cm^2 \ (\text{From previous problem})$$

$$V_T = V_{T0} + \frac{qN_I}{Cox}$$

$$0.8 = -0.32 + \frac{1.6*10^{-19} N_I}{1.72*10^{-7}} \Rightarrow N_I \approx 1.2*10^{-12}\ dopants/cm^3$$

Problem 3.3 : Channel Length

The electrical channel length is shorter than the drawn channel length due to lateral diffusions of the source and drain underneath the drawn gate (p.92 Rabaey). An equation which models this difference is given below, where L_D indicates the drawn channel length, ΔL gives the total diffusion difference, and X_d gives the diffusion difference of one side of the channel.

$$\begin{aligned} L &= L_D - \Delta L \\ &= L_D - 2x_d \end{aligned}$$

Note that this effect is always on, and differs from pinching off of the channel.

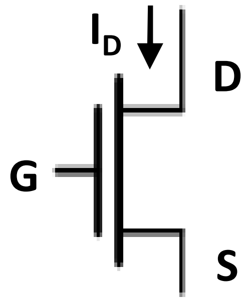
Problem 3.4 : Biasing $V_T = V_{T0} + \gamma\left(\sqrt{|(-2)\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}\right)$

$V_{SB} = 0$, so second term cancels and $V_{T0} = V_T$

1)

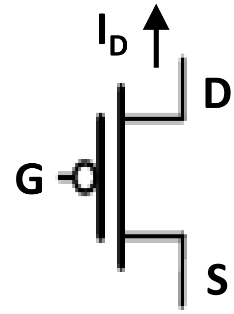
VGS = 1.8V
VDS = 1.8V

Saturation



VGS = -1.1V
VDS = -50mV

Triode/Linear



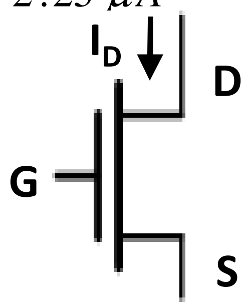
$$I_{D\_NMOS} = \frac{350 * 10^{-6} * 4}{2}(1.8-1)^2(1+0.05*1.8)$$
$$= 488\ \mu A$$

$$I_{D\_PMOS} = 150 * 10^{-6} * 4\left((-1.1-(-1))(-0.05) - \frac{(-0.05)^2}{2}\right)$$
$$= 2.25\ \mu A$$

2)

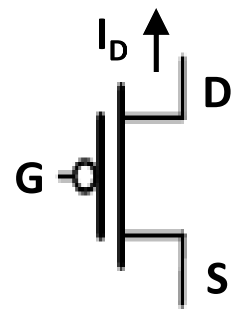
VGS = 0.9V
VDS = 1.8V

Cutoff



VGS = -2.5V
VDS = -1.0V

Triode/Linear



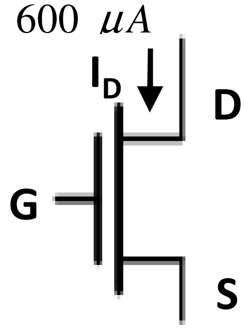
$$I_{D\_NMOS} = 0\ \mu A$$

$$I_{D\_PMOS} = 150 * 10^{-6} * 4\left((-2.5-(-1))(-1) - \frac{(-1)^2}{2}\right)$$
$$= 600\ \mu A$$

3)

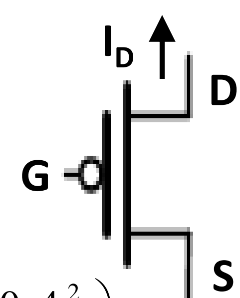
VGS = 1.5V
VDS = 0.4V

Triode/Linear



VGS = -1.8V
VDS = -1.6V

Saturation



$$I_{D\_NMOS} = 350 * 10^{-6} * 4\left((1.5-1)0.4 - \frac{0.4^2}{2}\right)$$
$$= 168\ \mu A$$

Note: Not stated in the problem, but lambda should be negative for PMOS, giving 207uA.

$$I_{D\_PMOS} = \frac{150 * 10^{-6} * 4}{2}((-1.8)-(-1))^2(1+0.05*(-1.6))$$
$$= 176\ \mu A$$