EEC 118 Spring 2009 Midterm

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This examination is closed book and closed notes. Some formulas which you may find useful are listed in the back of the exam. Calculators are allowed, however using the calculator's function memory to store course related material is NOT allowed and constitutes cheating on this exam.

For all problems, state any assumptions you make, show all work, and clearly mark your answers. Correct but unclear or ambiguous answers will not receive full credit.

Excerpts from the UC Davis Code of Academic Conduct state:

1. Each student should act with personal honesty at all times.
2. Each student should act with fairness to others in the class. This means, for example, that when taking an examination, students should not seek an unfair advantage over other classmates through cheating or other dishonest behavior.
3. Students should take group as well as individual responsibility for honorable behavior. This includes notifying the instructor or TA if you observe cheating.

I understand the honor code and agree to be bound by it.

Signature:
Name (printed):
Lab Section:

Grading:

Problem	Maximum	Score
1	8	
2	16	
3	15	
4	16	
Total	55	

1 Transistor Biasing

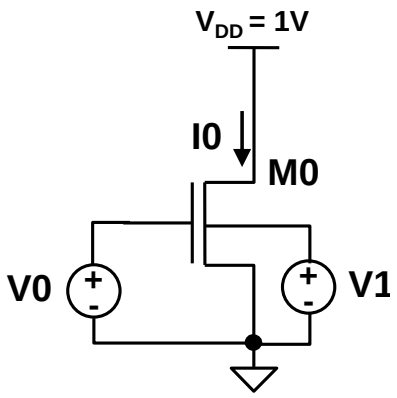

Figure 1: FET biasing circuit.

Problem 1.1 (**8 points**) Consider the NMOS bias circuit shown in Figure 1. Suppose we know that for the NMOS under bias, $V_{T0} = 1\text{V}$, $W/L = 4/1$, $\gamma = 0.35\text{V}^{1/2}$, $\lambda = 0\ \text{V}^{-1}$, $\mu C_{ox} = 350\ \mu\text{A/V}^2$, and $-2\Phi_F = 0.6\ \text{V}$. Given that $V0 = 3\text{V}$ and $V1 = -2\text{V}$, find the following:

- $V_{Tn} =$
- $I0 =$

Problem 1.1 (cont.)

2 Inverter

Assume all transistor W/L ratios are as shown in Figure 2 and the following transistor and supply voltage characteristics:

$V_{DD} = 5$ V	$\lambda = 0.02$ V^{-1}
$V_{T0,n} = 0.9$ V	$V_{T0,p} = -0.9$ V
$\gamma_n = 0.3$ V$^{1/2}$	$\gamma_p = 0.3$ V$^{1/2}$
$\mu_n C_{ox} = 250 \times 10^{-6}$ A/V^2	$\mu_p C_{ox} = 100 \times 10^{-6}$ A/V^2

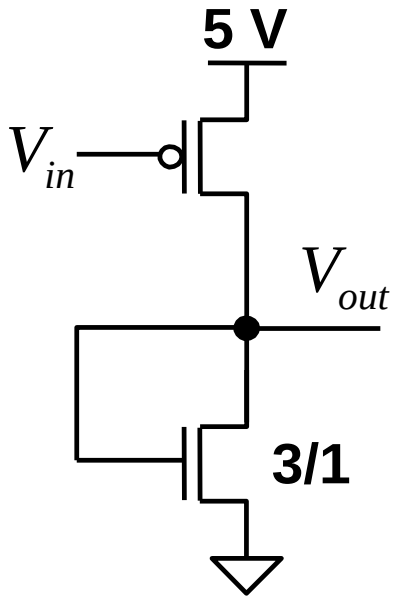

Figure 2: CMOS inverter.

Problem 2.1 (**2 points**) What is V_{OL} (approximately) for the inverter circuit in Figure 2? Justify your answer.

Problem 2.2 (**8 points**) Find W/L for the PMOS in Figure 2 such that $V_{OH} = 4.5$ V.

Problem 2.2 (cont.)

Problem 2.3 (**2 points**) Suppose that the only capacitances in the circuit of Figure 2 are the parasitic capacitances of the NMOS transistor. If the NMOS width W is doubled such that $W/L = 6/1$, what happens to the inverter fall time t_f (circle one)? Justify your answer.

- t_f almost doubles
- t_f is almost cut in half
- t_f stays about the same

Problem 2.4 (**2 points**) Under the same assumptions as Problem 2.3, if the NMOS width W is doubled such that $W/L = 6/1$, what happens to the inverter rise time t_r (circle one)? Justify your answer.

- t_r almost doubles
- t_r is almost cut in half
- t_r stays about the same

Problem 2.5 (**2 points**) Under the same assumptions as Problem 2.3, if the NMOS W/L is doubled to 6/1, what happens to V_{OH} as you designed in Problem 2.2 (circle one)? Justify your answer.

- V_{OH} increases
- V_{OH} decreases
- V_{OH} stays the same

A	B	C	F
0	X	X	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

Table 1: Truth table for function F.

3 Static CMOS Logic Design

Problem 3.1 (**2 points**) Consider the function F represented by truth Table 1. Write a Boolean expression for the logic function F.

Problem 3.2 (**6 points**) Design a single multiple input CMOS logic gate which implements F. You may assume that both true and complement versions of the input signals are available (i.e., A, $\overline{A}$, B, $\overline{B}$, C, $\overline{C}$)

Problem 3.3 (**6 points**) Assume a minimum-sized inverter has PMOS ratio $W_P/L = 4/1$ and NMOS ratio $W_N/L = 2/1$. Choose appropriate W/L ratios for the transistors in your circuit of Problem 3.2 such that the worst case rise and fall times are the same as a minimum-sized inverter. Indicate the sizes in your schematic above. Be sure to minimize the total area of the transistors.

Problem 3.4 (**1 point**) How many **other** implementations of logic function F can you think of which use the same number of transistors as your design?

4 Static CMOS Logic Analysis

For this problem, assume the transistor characteristics as shown in Table 2.

Parameter	NMOS	PMOS
V_{T0}	1.0 V	-0.9 V
μC_{ox}	300 μA/V^2	100 μA/V^2
γ	0	0
λ	0.0 V^{-1}	0.0 V^{-1}
V_{DD}	3.3 V	

Table 2: Problem 4 Transistor Parameters.

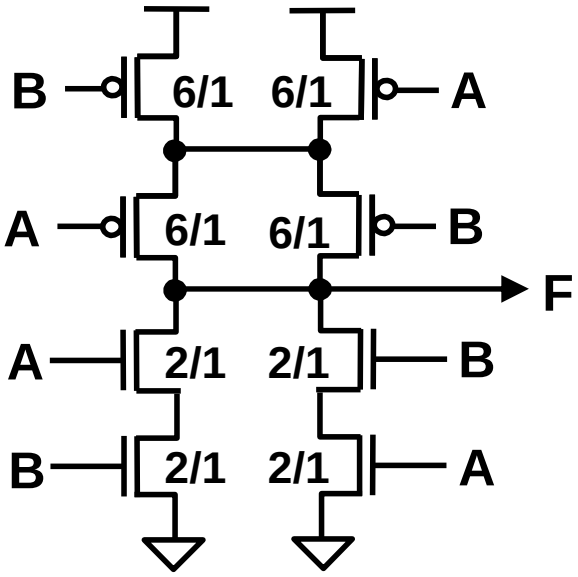

Figure 3: CMOS logic gate. All dimensions in microns.

Problem 4.1 (**1 point**) Write a Boolean algebra expression for the function F computed by the static CMOS logic gate shown in Figure 3.

Problem 4.2 (**2 points**) For the circuit shown in Figure 3 and assuming the only relevant capacitance is at output F, what set of input values gives the worst case rise time? Justify your answer.

Problem 4.3 (**2 points**) What set of input values gives the worst case fall time? Justify your answer.

Problem 4.4 (**7 points**) Assume the capacitance at output F is 100 fF. Find the worst case fall time t_f using the switch RC model. Compute an average "ON" resistance using two resistance values, one at the beginning of the output falling transition and one at the end of the output falling transition, as specified in the definition of t_f.

Problem 4.4 (cont.)

Problem 4.5 (**4 points**) Draw the schematic for a static CMOS logic gate which computes the same function as the circuit in Figure 4.1 but uses only four transistors. You do **not** need to find W/L for the transistors in your circuit.

Miscellaneous Formulas

MOSFET Threshold Voltage

$$V_T = V_{T0} + \gamma \cdot \left(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|} \right)$$

$$\gamma = \frac{\sqrt{2q \cdot N_A \cdot \epsilon_{Si}}}{C_{ox}}$$

CMOS Inverter Switching Threshold

$$V_{TH} = \frac{V_{T0,n} + \sqrt{\frac{1}{k_R}} \cdot (V_{DD} - |V_{T0,p}|)}{\left(1 + \sqrt{\frac{1}{k_R}}\right)}$$

CMOS Inverter Propagation Delay Times

$$\tau_{PHL} = \frac{C_{load}}{k_n(V_{DD} - V_{T,n})} \left[\frac{2V_{T,n}}{V_{DD} - V_{T,n}} + \ln\left(\frac{4(V_{DD} - V_{T,n})}{V_{DD}} - 1 \right) \right]$$

$$\tau_{PLH} = \frac{C_{load}}{k_p(V_{DD} - |V_{T,p}|)} \left[\frac{2|V_{T,p}|}{V_{DD} - |V_{T,p}|} + \ln\left(\frac{4(V_{DD} - |V_{T,p}|)}{V_{DD}} - 1 \right) \right]$$

Switch Model Propagation Delay Times

$$t_{PHL} = 0.69 R_n C_L$$

$$t_{PLH} = 0.69 R_p C_L$$

$$t_f = 2.2 R_n C_L$$

$$t_r = 2.2 R_p C_L$$

Junction Capacitances

$$C_{j0} = \sqrt{\frac{\epsilon_{Si} \cdot q}{2}} \left(\frac{N_A N_D}{N_A + N_D} \right) \frac{1}{\phi_0}$$

$$C_j(V) = \frac{AC_{j0}}{\left(1 - \frac{V}{\phi_0}\right)^m}$$

$$C_{eq} = AC_{j0}K_{eq}$$