EEC 118 Lecture #10: Dynamic Logic

Rajeevan Amirtharajah
University of California, Davis

Jeff Parkhurst
Intel Corporation

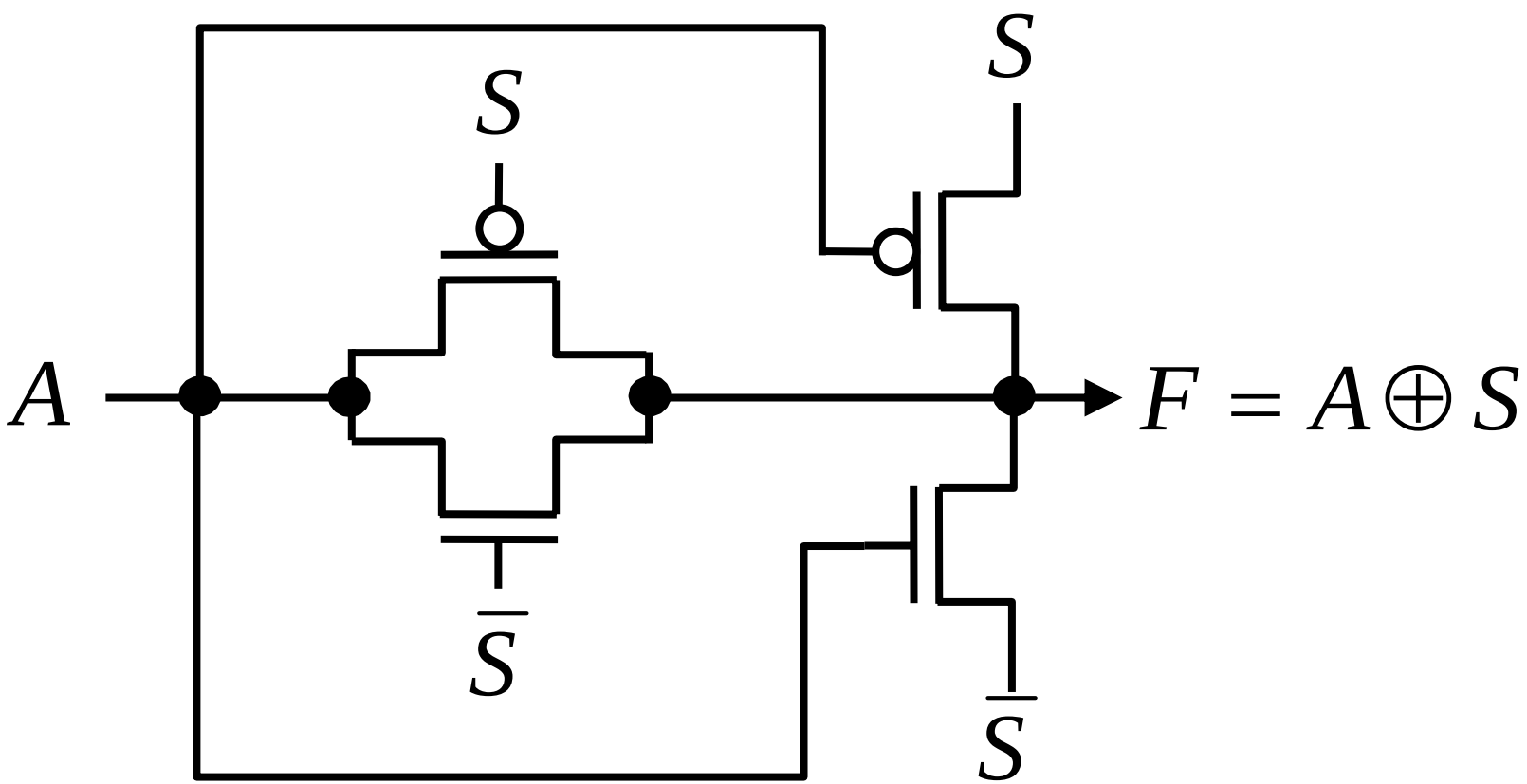
Announcements

- **Complete Lab 4 this week**

Outline

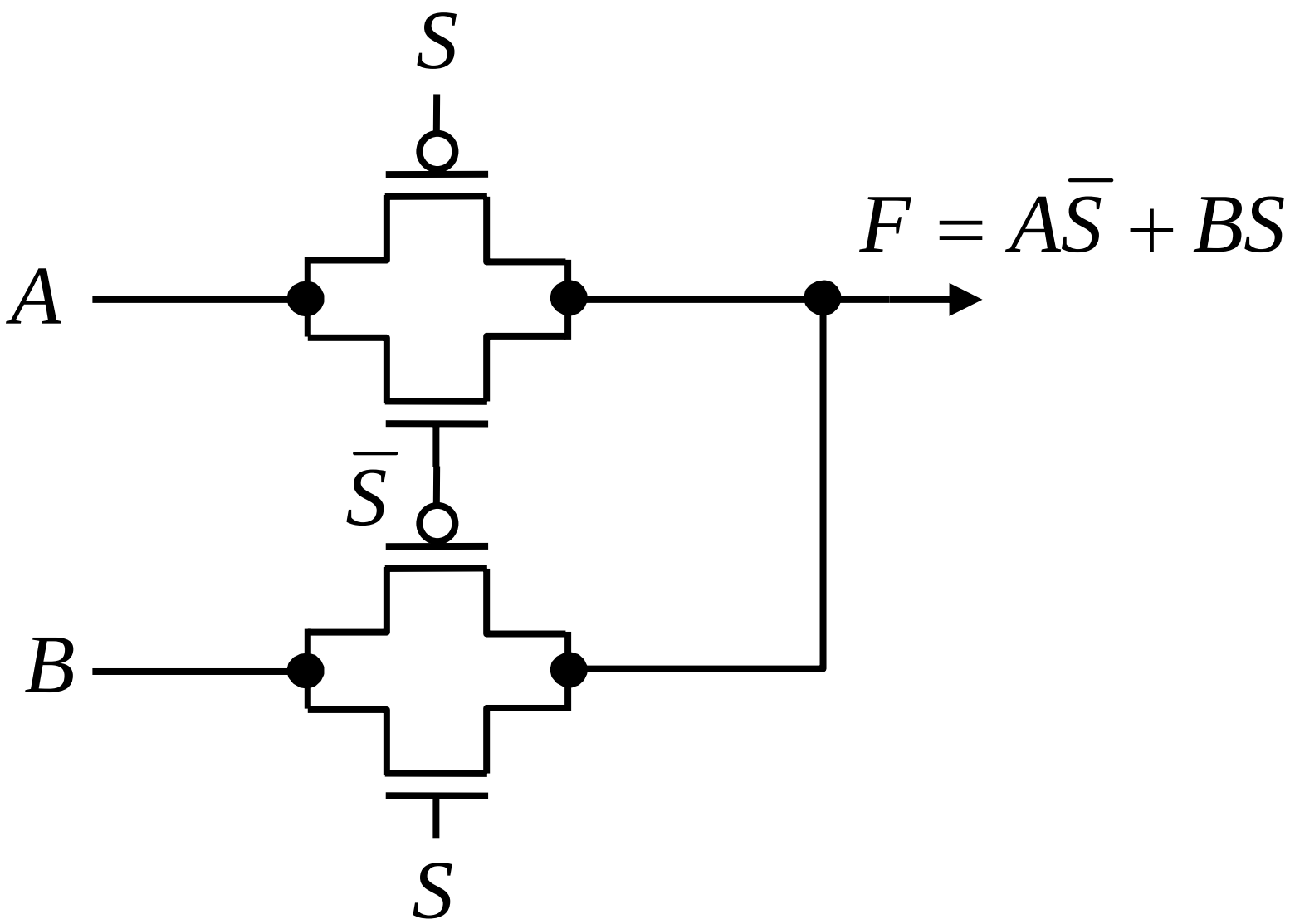
- **Today: Alternative MOS Logic Styles**
- **Dynamic MOS Logic Circuits: Rabaey 6.3 (Kang & Leblebici, 9.4-9.6)**

Review: Transmission Gate XOR



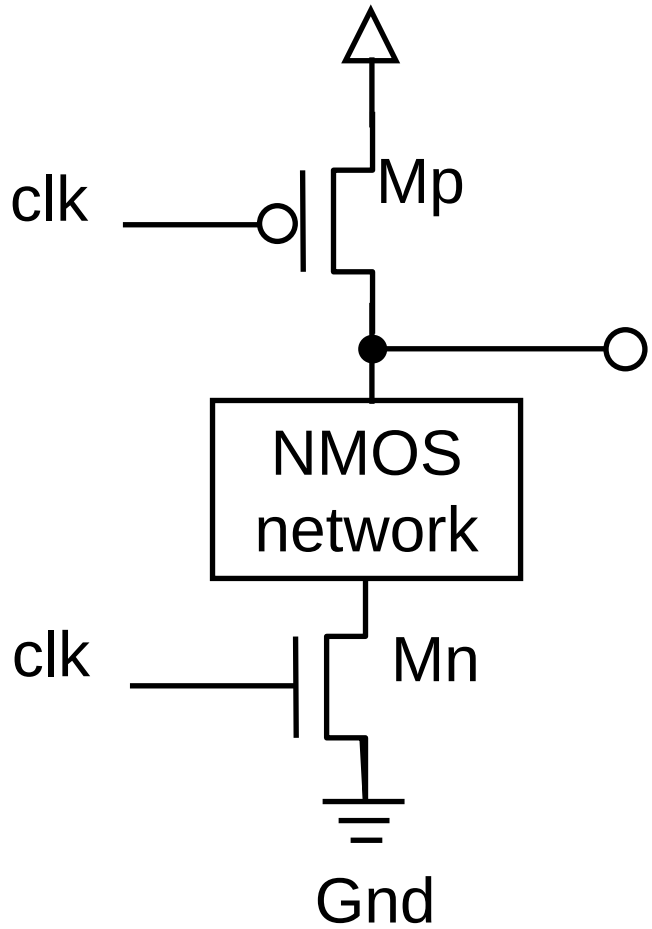
- **If S = 0, F = A and when S = 1, F = ~A**

Review: Transmission Gate Multiplexer



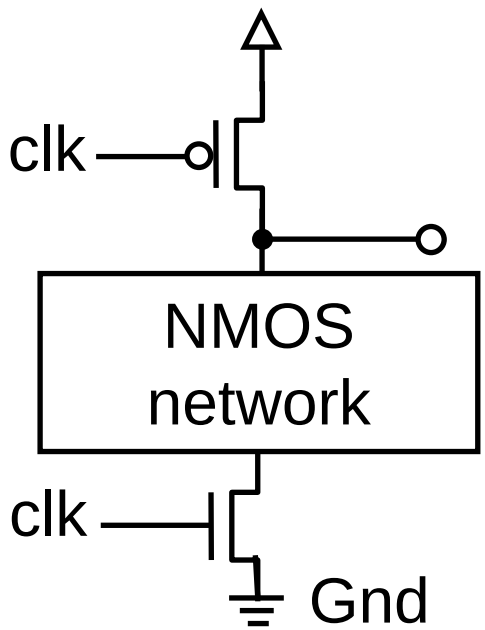
Dynamic CMOS

- **Operation**
  - Clk low during Pre-charge
    - Mp is on while Mn is off
    - Output charged to Vdd
  - Clk high during evaluate
    - Mn is on while Mp is off
    - Output pulled down according to PDN function
- **PDN design same as static CMOS**



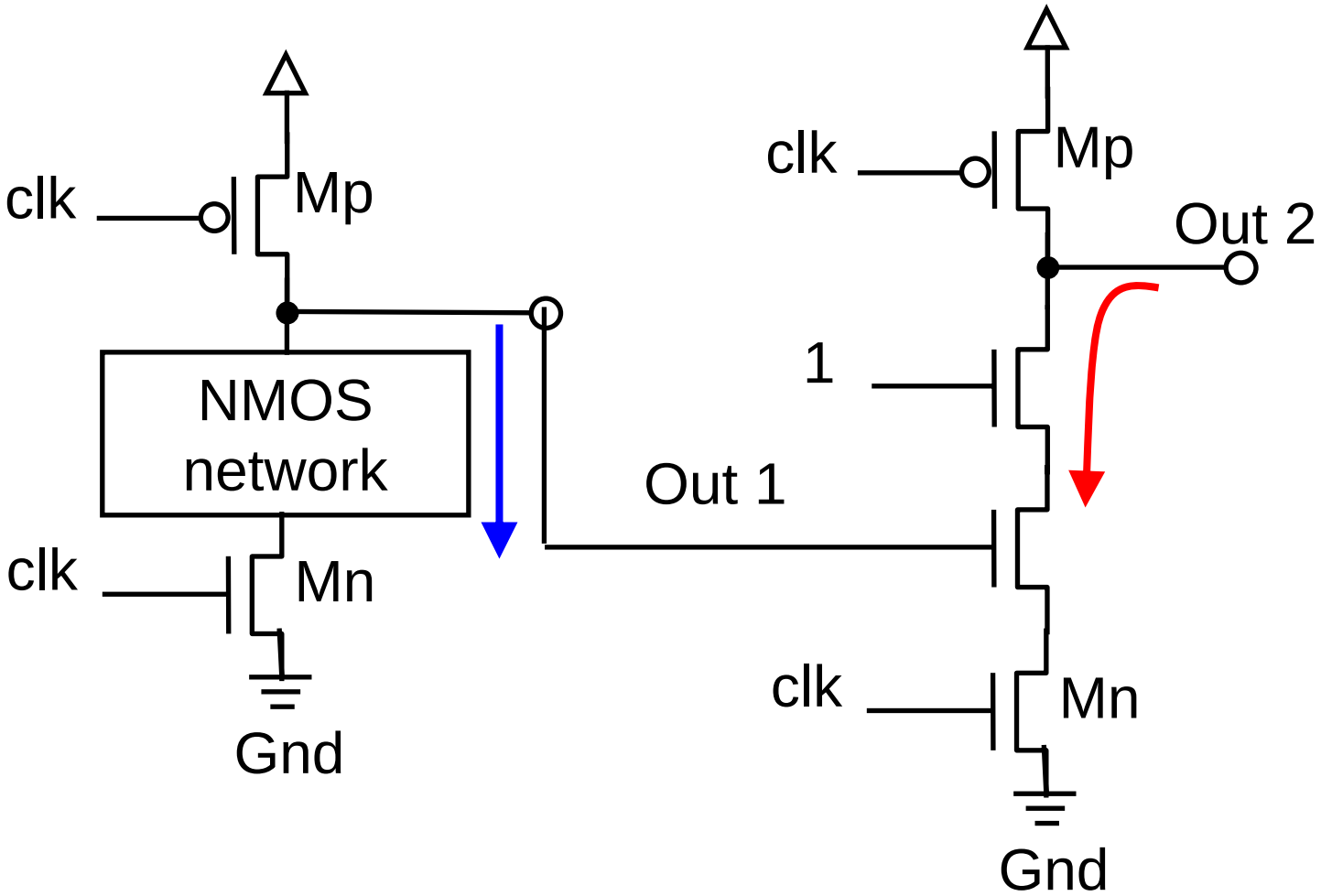
Dynamic CMOS Tradeoffs

- **Advantages:**
  - Faster – why?
    - Reduced input load
    - No switching contention
  - Less layout area



- **Disadvantages:**
  - Multiple stage issues
  - Charge leakage
  - Charge sharing
  - Capacitive coupling
  - Cannot be cascaded
  - Complicated timing/clocking
  - Higher power
  - Lower noise margins
  - Does not scale well with process

Multiple Stage Issue: Output Discharge Race



- **During pre-charge stage, inputs to second gate are all high: Out 2 could discharge before Out 1 discharges**

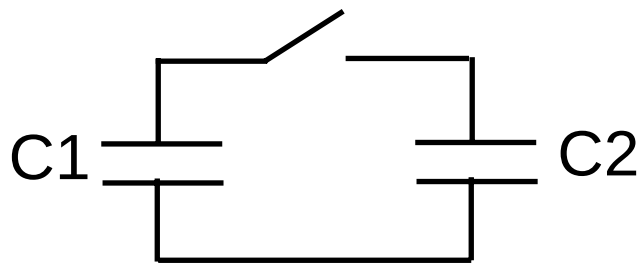
Cascading Multiple Stages

- **During pre-charge stage, inputs to second gate are all high**
  - At the beginning of evaluate stage, Out 2 is discharged.
  - Out 1 goes through its evaluation stage concurrently and goes low
    - Hence out 2 was supposed to be high, but already discharged.
    - Dynamic logic driven by the same clock cannot *be cascaded directly*

Charge Sharing

- **Output is floating after clk = ‘1’ if inputs are ‘0’**
- **If upper transistors in a stack switch, the intermediate and output node voltages will be equalized, possibly leading to a drop in the output voltage = noise**
- **Final output (initial charge distributed over both capacitors):**

$$V=(C_1V_1+C_2V_2)/(C_1+C_2)$$



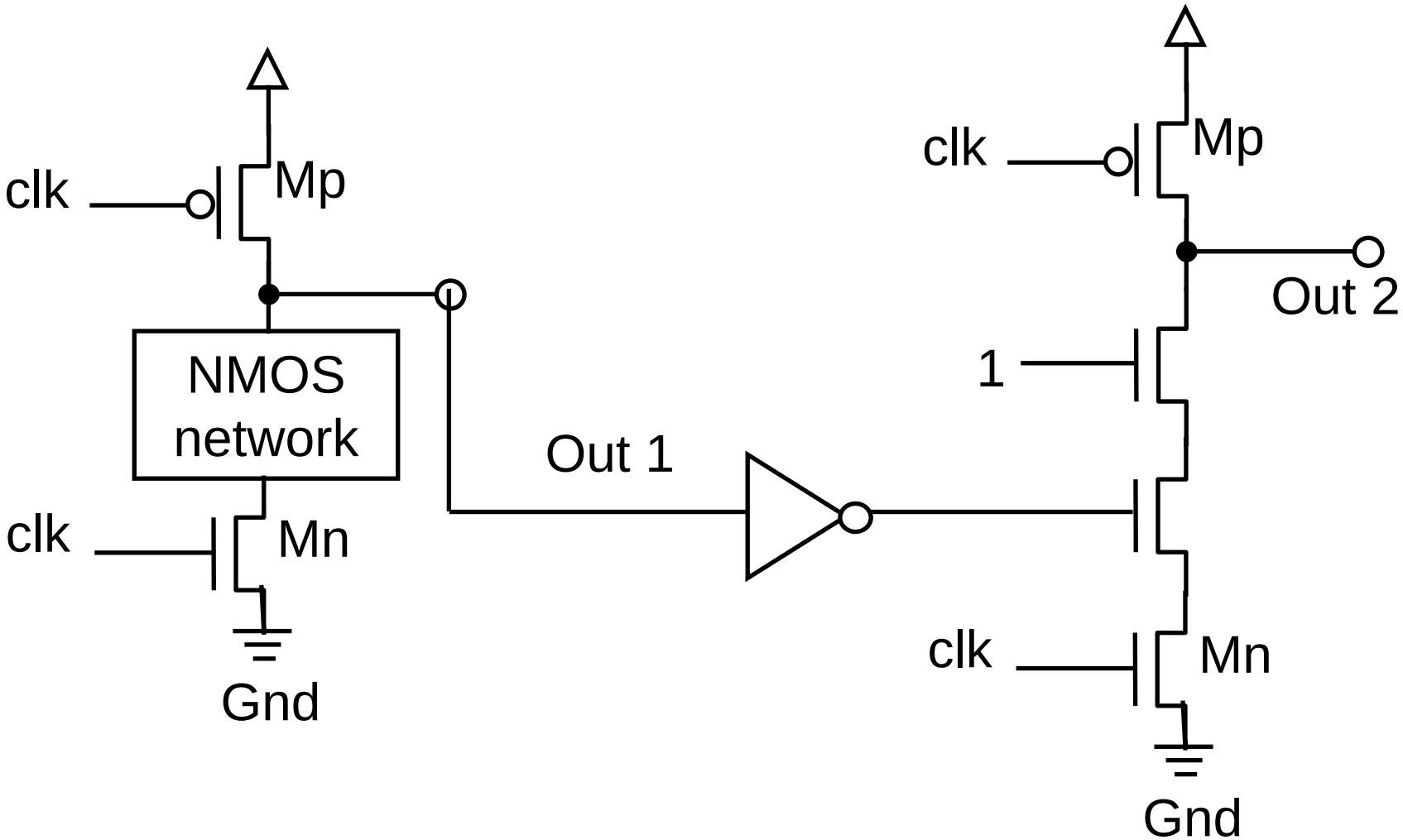
Charge Leakage & Capacitive Coupling

- **Output is floating after clk = ‘1’ if inputs are ‘0’**
- **Since the current is not 0 when transistors are in cutoff, current can leak charge away from the output when all inputs are ‘0’**
- **Changes in input signals couple to the output and intermediate nodes, also resulting in voltage drops**

Noise Solutions

- **Charge sharing:**
  - Ensure the output capacitance is large enough such that the voltage drop is minimal
  - Precharge internal stack nodes to V_{DD}
  - Pre-discharging internal stack nodes can increase performance, but worsens noise
- **Charge leakage/sharing and capacitive coupling:**
  - Add a keeper PMOS (weak P pullup) – increased evaluation contention

Domino Logic



Domino Logic

- **Add an inverter between dynamic gates**
  - Inverter drives the gate's fanout – increased performance
- **Sometimes the inverter is replaced with a more complex static CMOS gate**
  - Incorporates more logic per stage to improve speed
- **Static CMOS gate improves overall circuit dynamic noise margins**

Cascading Domino

- **For gates with all inputs coming from other domino gates, the bottom NMOS transistor can be eliminated**
  - Why? All inputs will be ‘0’ during precharge and can only transition from ‘0’ to ‘1’ during evaluate due to inverter between stages…
  - Results in increased performance due to decreased stack height
  - Precharge now depends on input precharge time

Dynamic Logic Power

- **Power depends upon switching activity**
  - Switching activity depends upon the probability of a '1' input

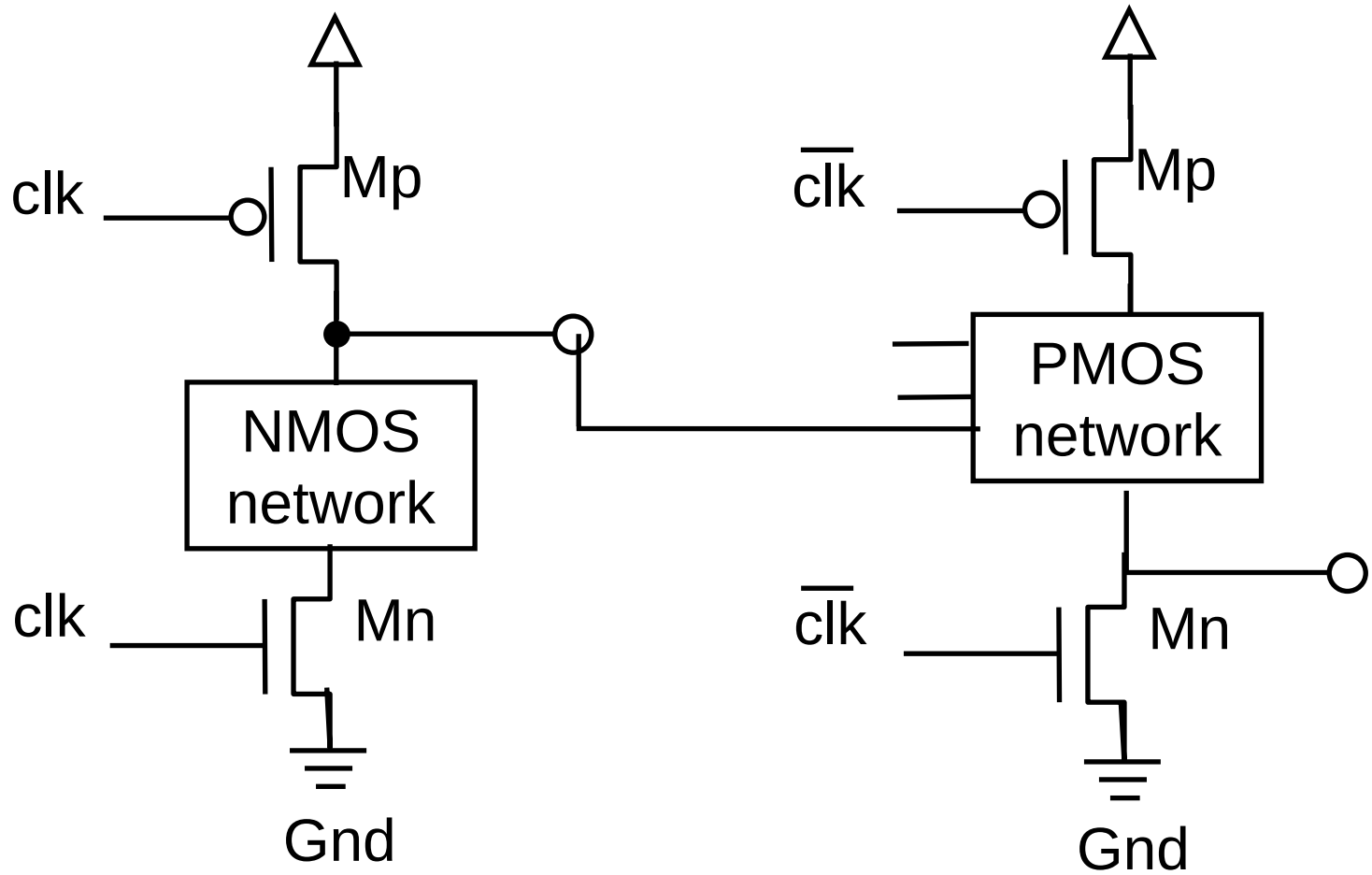
$$P_{avg} = \frac{1}{T} C_{load} V_{DD}^2 = C_{load} V_{DD}^2 f$$

  - Effective capacitance C_{load} is doubled when the gate evaluates because the gate must later precharge
  - Frequency must be multiplied by the probability that an evaluation will occur
- **Power is usually higher for domino logic except when it replaces prior logic with very high activity factors**

Bottom Line

- **Tradeoff between performance and power exists**
- **Many things can go wrong from a design standpoint (high risk)**
  - Charge sharing, noise, leakage currents, race conditions
- **Debugging challenge, especially in deep submicron**
  - Leakage currents put lower bound on clock frequency for testing
- **Best to use dynamic logic only when necessary**
  - High performance circuits such as microprocessor critical paths

NORA Logic Gate



NORA Logic

- **Solves problem of cascading dynamic gates, but is vulnerable to noise**
  - Alternate P-dynamic and N-dynamic stages
  - Both clk and $\overline{\text{clk}}$ required
  - Lose some of the speed benefits due to added PUNs

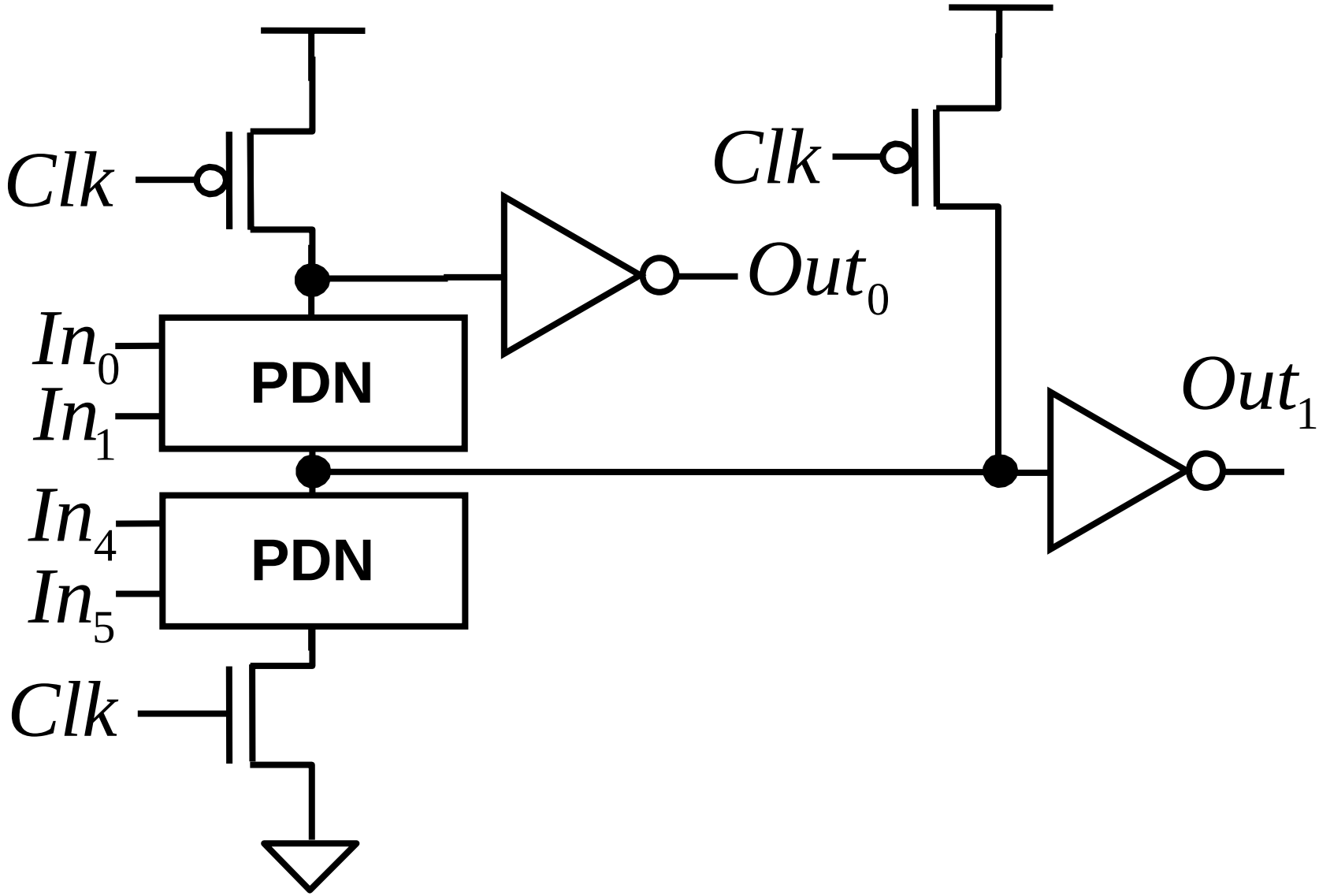
Zipper Logic

- **Like NORA logic…but,**
  - PMOS precharge and NMOS pre-discharge weakly on during evaluation stage…

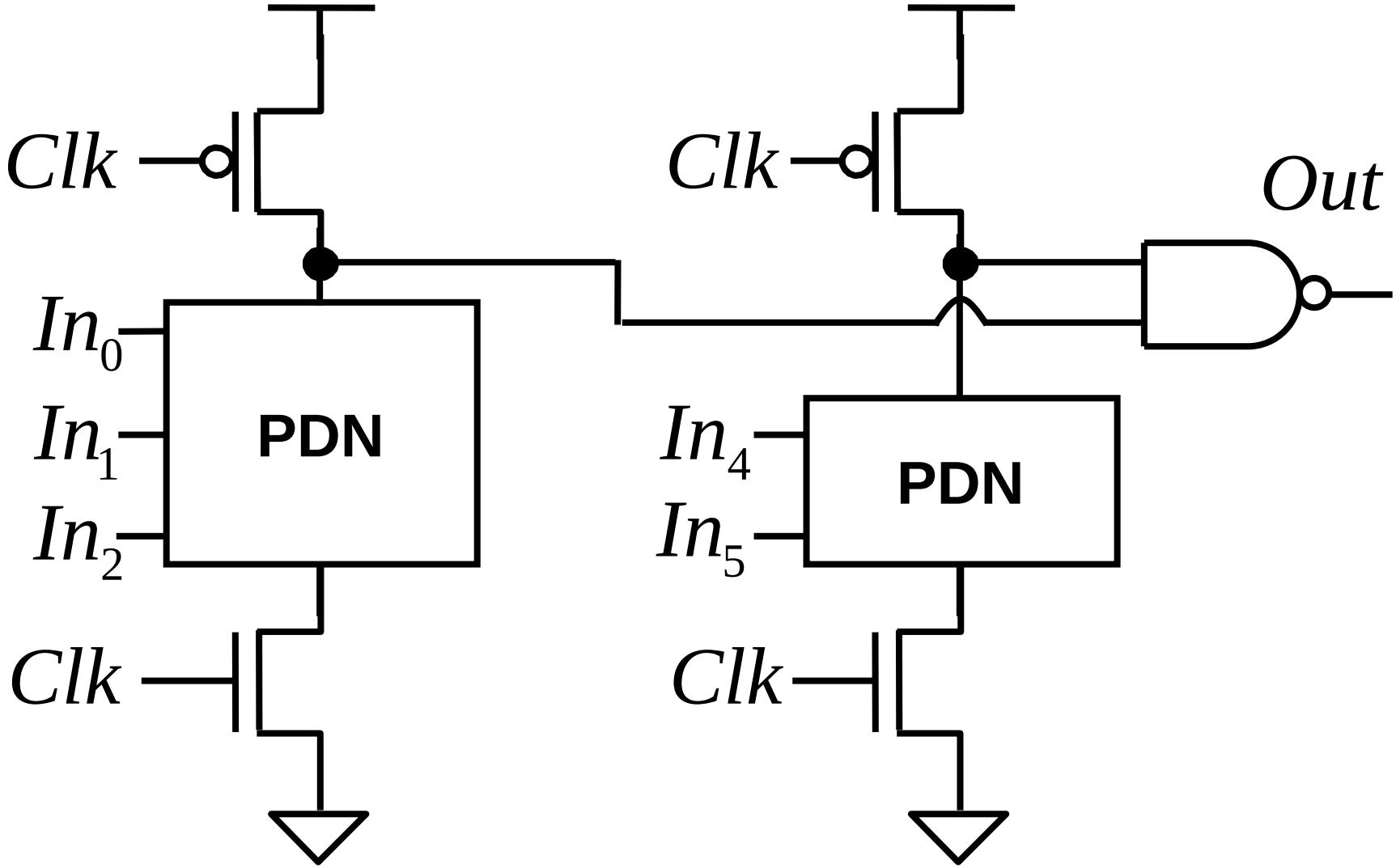
Variations on the Domino Theme

- **Multiple-Output Domino**
  - Exploit situation when certain outputs are subsets of other outputs to reduce area
  - Precharge intermediate nodes in PDN and follow with inverters to drive other N-block dynamic gates
- **Compound Domino**
  - Use complex static CMOS gates (NANDs, NORs) on outputs of multiple dynamic gates in parallel
  - Replaces large fanin domino gates with lower fanin gates
  - Capacitive coupling from static gate outputs to dynamic gate outputs an issue

Multiple Output Domino CMOS Logic



Compound Domino CMOS Logic



Next Topic: Arithmetic

- **Computing arithmetic functions with CMOS logic**
  - Half adder and full adder circuits
  - Circuit architectures for addition
  - Array multipliers